Optimized Design and Simulation of Ring Counter using 45nm Technology

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Abstract *— In the era of technical world, sequential circuits are playing their vital role in the designing of digital system. Sequential circuit design with low power and high speed at smaller chip size has become the prime concern for researcher and day by day growth in VLSI technologies also sustain the flow for achieving the desired goals. A counter is a sequential circuit having various applications in the field of embedded system, pattern generations, signal synthesis, Digital to Analog conversion etc. In this paper, an optimized designing mechanism has been deployed to design a high speed, cost effective and low power 4-bit ring counter which can also be extended to higher order ring counter designs. In this work, performance of the proposed ring counter is enhanced by using a negative edge triggered master slave D flip flop which have 14 MOS transistors in its design as compare to conventional counter. The proposed paper has accomplished the design goals by reducing the 68.5% transistor count, 29.85% power consumption and got the 95% higher speed.*

Keywords *— Ring Counter; Master slave D flip flop; negative Edge trigged; VLSI power dissipation; Transistor count;CMOS gates.*

I. INTRODUCTION

In digital circuits, Counter plays very significant role. Counters are digital circuits which follow a particular pattern sequence in response to the number of times an event happened. So every time whenever a clock take place, present state of counter changes to next state. This creates its wide applications in digital control systems, embedded systems, processors, memories, frequency synthesizer, digital timing circuits etc.[1]. A counter consists of set of flip flop which stores bits '0' and '1' and results in counter state pattern. The capabilities of a counter can be represented by modulus which represent the maximum number of states in a counter.

In sequential circuits, ring counter has made its place in controlling application based on its unique counting sequence. It uses a shift register in which set of flip flop are cascaded to circulate a bit '1' through all the flip flops. Therefore, inputs of flip flops are derived from the output of previous flip flop. and in the case of first flip flop, the output of last stage is given back to first stage. Initially, first stage is required to be set by external input 'preset' and other flip flops are cleared. So for 4-bit ring counter, we start with 1000 binary pattern and then 1 circulate as 0100, 0010, 0001 and then again to 1000 binary pattern in next 4 input clock pulses [2].

The growth in manufacturing capabilities of VLSI industries has evolved the technical world. A CMOS inverter is basic cell in VLSI design as shown in Fig. 1. Transistor count is increasing day by day which leads to reduce the chip size, power consumption and increase its speed further reduced to its cost [3]. But quest of mobility, tiny product size, and more battery back-up is creating a vacancy for more enhancements in VLSI design parameters. So selection of better technology and less number of CMOS logic gates make design more power efficient and effective for digital designing. In this paper, design of ring counter is proposed using master slave D flip flop and a comparison of this circuit has been done with its conventional design in terms of speed and power dissipation. For better design, negative edge trigged clock circuit is employed in the d-flip flop. In this work, Cadence EDA tool is used for the designing of proposed counter. The work in this paper proceed as:

Section II explain the designing aspects of the CMOS circuit implementation. Section III describes the Ring counter circuit design. Section IV presents the proposed schematic design of counter. Section V discusses the simulations and the results of proposed work and in the section VI, the paper is concluded.

II. DESIGNING ASPECTS

In VLSI circuit design, main target is to reduce the power consumption for CMOS circuits. In VLSI applications, the use of continuously increasing clock frequency is the main cause of increasing the power consumption in CMOS circuit design even the circuit operates at low supply voltage. In CMOS design, Power consumption has a static component resulting from consisting of threshold conduction through inactive transistors, leakage of inactive device, contention current and gate tunneling current etc. [4] The sub-threshold current in inactive device is:

$$I_{ds} = I_{dso} e^{\frac{V_{gs}-V_t}{nV_T}} \left(1 - e^{-\frac{V_{ds}}{V_T}}\right) \quad (1)$$

Charging and discharging of load capacitance increases the dynamic power and CMOS circuit

switching take place when the short current flows through it also increases power dissipation [8]. When the PMOS transistor is in ON state then provided finite nonzero load capacitance gets charged and by providing current to NMOS transistor from the ground, it gets self-charged and activated. The charging and discharging of load capacitance leads to the power dissipation expression as given below:

$$P = 0.5\ C_L\ (V_{dd})^2\ f_{clk}\ E_{sw} \quad (2)$$

Here, f_{clk} is clock frequency, C_L is load capacitance, E_{sw} is average switching activity and V_{dd} is supply voltage. Speed of the operation increases in digital circuits when clock frequency is increased. In high switching frequency of CMOS devices resulting in higher power dissipation [5].

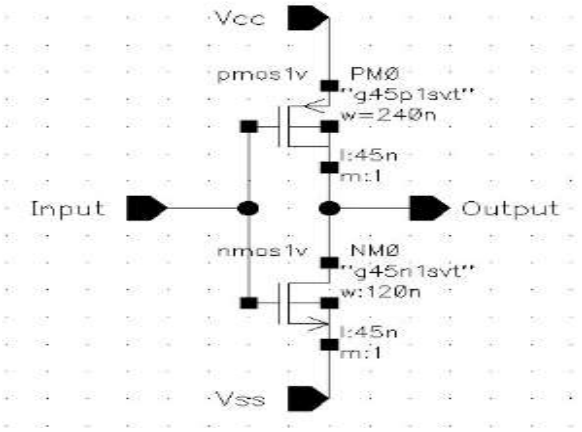

Fig. 1. Schematic diagram of CMOS Inverter

The power dissipation of a digital system is generally contributed by the sequential circuits. According to logic level sequential circuit synchronously changes its present state with clock period. During positive or negative edge transitions of clock, the states of circuits waveform changes. The main factor for power dissipation is the clock transition occur low to high and high to low state. In CMOS design, during the transition of clock, both NMOS and PMOS transistors conducts for a small duration of time due to having very some value of fall and rise time. A current is flow through the circuit from V_{dd} to ground due to an electrical path created. This current is referred to as Short circuit current or thorough current which appear as a spike during clock transition [5]. This short circuit current is the large part of dynamic power loss which is:

$$P_{sc} = I_{sc}\ .V_{dd}\ .ts\ .\ E_{sw} \quad (3)$$

Here, t_s is switching delay and I_{sc} is the switching current [5]. The above discussed both phenomenon are used to calculate the power dissipation in sequential circuits which depends upon the clock switching frequency. It has been seen in sequential circuits that clock signal is responsible for 15 to 45 % of total power dissipation [6].

III. RING COUNTER DESIGN

Ring counter is a synchronous circuit having basic element as flip flop. A flip flop can store data on the rising edge of clock pulse or falling edge respectively called as positive edge and negative edge flip flop. A master slave D flip flop has 8 NAND gates and an inverter as shown in fig. 2. First stage constitutes master that operates directly on external

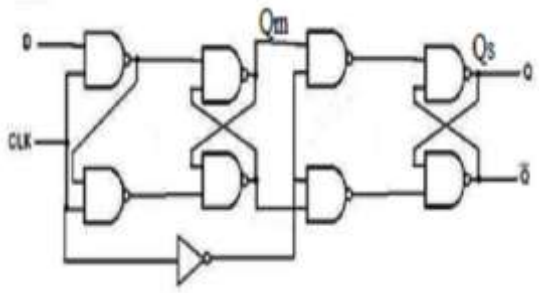

Fig. 2. Conventional master slave D flip flop [1]

clock pulse. Slave, which is the second stage, is applied with inverted form of external clock. When external clock is at high level master is active and it follows the D input. At the same time slave is not functional and thereby holds its previous state. When clock does transition from level 1 to level 0 master passes its output to slave, which is active now and hence stores the passed value. Master is deactivated for the negative clock level and is unaffected by the changes of its input. Transistor level schematic of negative edge triggered D-flip flop is shown in fig.3.

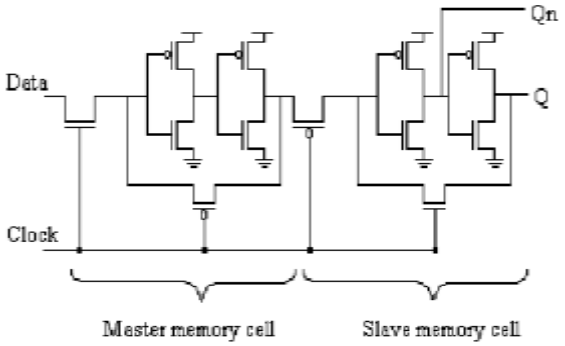

Fig. 3. Negative edge triggered master slave D flip flop [9]

A ring counter comprises of a circular shift register where the output of the last flip flop is fed to the input of the first flip flop. It circulates a single one bit around the ring. In a 4-bit register ring counter, with initial flip flop values of 1000, the subsequent patterns are: 1000, 0100, 0010, 0001, 1000. Here one of the flip flops has to be preloaded with bit 1 in order to operate as per ring counter logic.

Ring counter stage is evaluated at every triggering edge of clock. If n flip flops are used in the design of a ring counter, its modulus count is n. Modulus count refers to the number of states present in the counter state flow. The block diagram of a 4-bit ring counter is shown in the fig. 4.

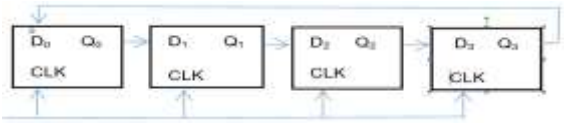

Fig. 4. Block diagram of 4-bit Ring Counter

In a 4 bit ring counter the modulus count is 4. Four D flip flops are cascaded with the output of one given as the input to the next and output of the last is given as input to the first. The flip flops are provided with the same clock pulse justifying the synchronous nature of the ring counter. As soon as the clock pulse is first applied to the flip flops one of the flip flops is set at logic 1. This 1 would circulate in the flip flops as per the counting sequence shown in table I. [7]

TABLE I. State table of 4-bit Ring Counter

Clock	Q_3	Q_2	Q_1	Q_0
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	0	0	0	1
8	1	0	0	0

Ring counters are used to create complicated finite state in logic designing of FPGAs and ASICs. Ring counters are employed for encoding input pulses to decimal, octal and other forms.

IV. PROPOSED SCHEMATIC DESIGN

The designing of proposed Ring counter has been performed in Cadence EDA tool. Its Virtuoso schematic editor is used for transistor level schematic designing using 45nm technology and Multimode simulator is used for the design simulation. The NMOS and PMOS transistor of specification given in table II are picked from component Library and its proposed design has been implemented. Firstly, an inverter cell is designed and then it is used along with NMOS and PMOS transistor to create D-flip flop in master slave mode as shown in Fig.5. Further D-flip flops are cascaded to design shift register Ring counter.

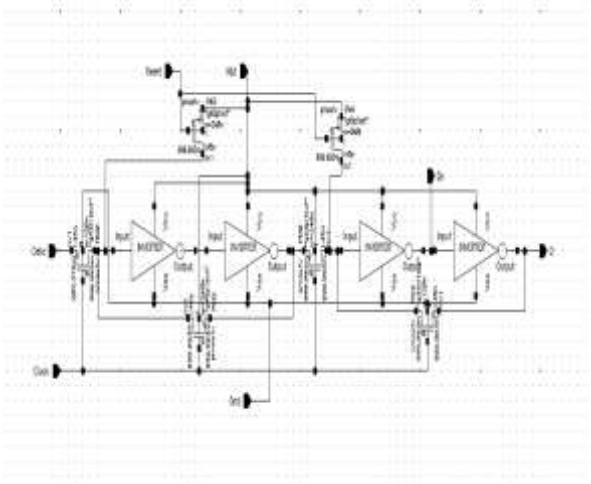

Fig. 5. Proposed Master slave D flip flop design

In the proposed design, transistor count is tried to reduce. Here 14 transistors are employed to design master slave D-flip flop. This flip flop design is used as instance in ring counter designing.

TABLE II. NMOS and PMOS specifications

Parameter	PMOS transistor	NMOS transistor
Width	240 nm	120 nm
Length	45 nm	45 nm
S/D metal	400 nm	400 nm
Finger width	240 nm	120 nm
Fingers	1	1
Threshold	800 nm	800 nm

Subsequently, proposed Ring counter of 4 bit is implemented using master slave D flip-flop as shown in fig. 7. In this design, flip-flop cells are cascaded such that output of a flip-flop derived the input of next flip flop. The output of most significant flip flop derived the input of least significant flip flop. For making a synchronized ring counter, same clock is also associated in the design along with reset circuit. Reset circuit is designed such a way that it can start the counter from the initial state 1000 whenever required.

In this paper, a conventional 4-bit Ring counter by means of master slave D flip flop is also implemented for the comparative study as shown in Fig. 8. The same specification of NMOS and PMOS are used in the designing of conventional D flip flop as given in table 2. This master slave D flip flop is designed using single inverter and eight NAND gates as shown in fig. 6.

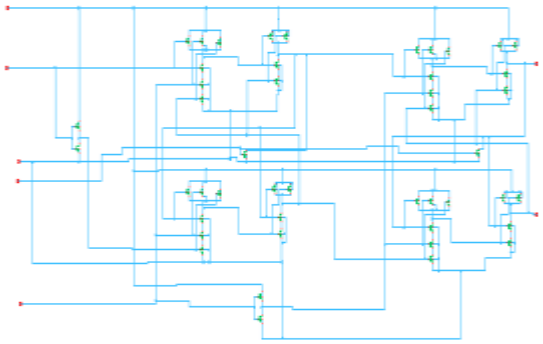

Fig. 6. Conventional master slave D flip flop

V. Result Simulations and Discussions

The proposed and conventional designs of Ring counter are simulated for 200 ns and analyzed using 45 nm technology at 1V voltage rating in Cadence tool. Fig. 9 and fig. 10 demonstrate the transient response for the simulation of proposed and conventional design respectively. The output sequence as shown in Table 1 can be easily analyzed that bit 1 is circulating in all the flip flops of ring counter which can be verified in its transient response also. Here Q_3 and Q_0 are the most significant bit and least significant bit respectively in the design. The clock inputs of the both design are running at10ns clock signal frequency. Similarly count sequence of the conventional Ring counter can be verified from Table 1. The delay and power dissipation of the two design are then calculated with the help of their transient responses. The simulation result also provide the transistor count in the design.

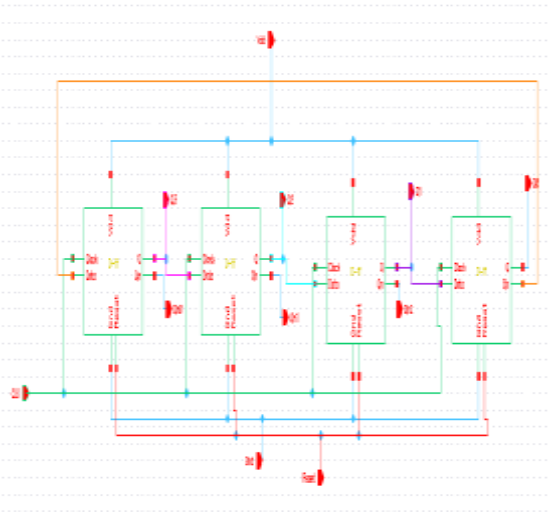

Fig. 7. Proposed 4 bit Ring Counter

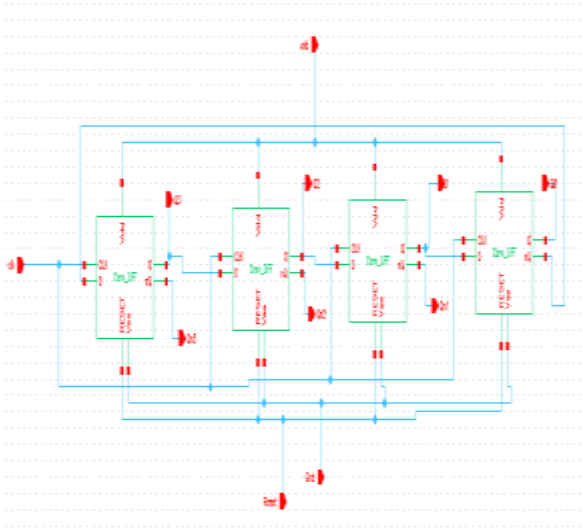

Fig. 8. 4-bit conventional Ring Counter

Performance and comparative analysis of the proposed Ring counter design with respect to the conventional design, in terms of power dissipation, delay and transistor count is done in Table III. All the parameters are then graphically compared with the help of bar charts in Fig. 11.

Table 2. Performance and cost analysis

Design	Power Dissipation (pw)	Delay (ns)	Transistor count
Conventional Ring Counter	313.43	120.125	186
Proposed Ring Counter	219.85	5.216	58

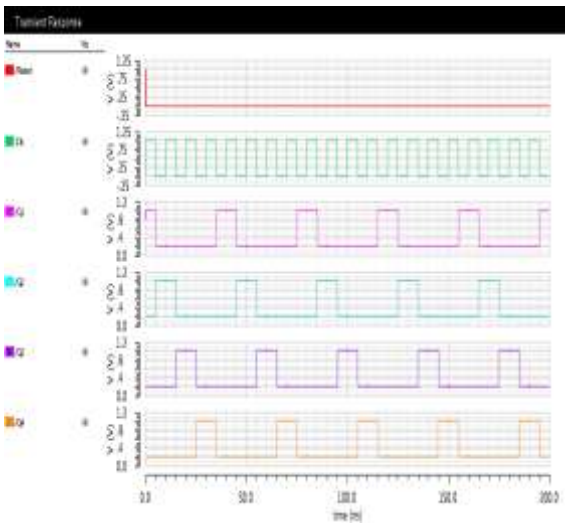

Fig. 9. Transient response of proposed 4 bit Ring Counter

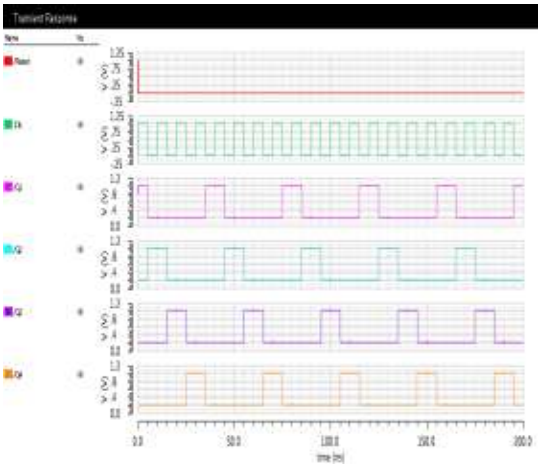

Fig. 10. Transient response of conventional 4 bit Ring counter

From the Table 2 and bar charts, it can be analyzed that the power consumption in 4-bit Ring counter using proposed design and conventional design is 219.85 pw and 313.43 pw respectively. This illustrates 29.85% reduction in power consumption which makes the proposed design suitable to be used in the applications where low power consumption is imperative. The propagation delay using proposed design and conventional design are 5.216 ns and 120.125 ns respectively which results in 95% reduction in case of proposed design compared to conventional design. So the proposed design is much suitable in the applications where the counter response required to be of very high speed. In case of proposed design, the transistor count reduces to 58 from 186 as is in conventional design which reflects a 68.5% reduction. This reduction in transistors count would lead to cost effective design because of its less chip area requirement.

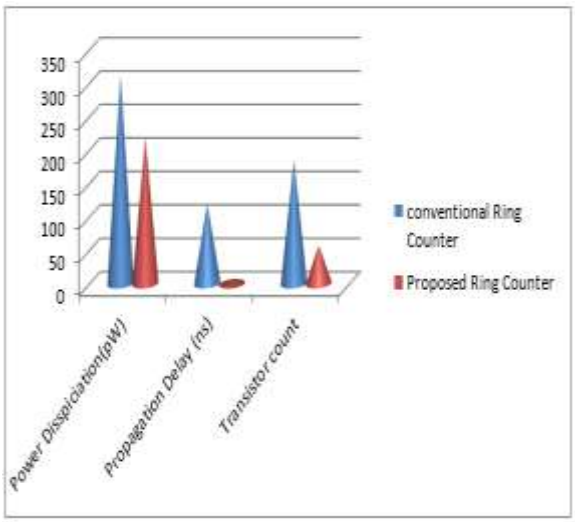

Fig. 11. Comparative analysis in terms of Power dissipation, Propogation delay and Transistor count

Hence the proposed counter design is suited for the applications in area efficient, power efficient and energy efficient VLSI designs. The proposed Ring counter design may further be finds its use in the efficient designing of embedded circuits like processors, DACs, digital memories, frequency synthesizer, digital timing circuits etc.

VI. Conclusion

In this paper, an optimized 4-bit Ring counter is designed using master slave D flip flop. It is made efficient in terms of less power dissipation, reduced transistor count and high speed operation. The parameters of proposed counter are compared with conventional design and found it better in its performance. The proposed design show the superior performance in its speed as the propagation delay in proposed counter is found 5.216 ns as compare to 120.125 ns delay in conventional counter.The proposed design has 219.85 pw power dissipation where conventional design has 313.43 pw power dissipation. The proposed design also show better results in its cost analysis as it requires only 58 transistors in its design as compared to 186 transistor count of conventional counter. So the results of this study concluded that the proposed counter is more optimized as compare to its conventional counter design.

VII. References

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