Performance Evaluation in Adiabatic Logic Circuits for Low Power VLSI Design

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Abstract:- *As the in semiconductor industries progress by following Moore's law faithfully from last five decades, and integrating more transistors along with functional circuits on a single chip periodically with every coming process technology. However, this progress help in rapid run towards tiny, circuit design high speed and economical VLSI (Very Large Scale of Integration) circuits has added to excessive power dissipation of numerous circuits used today. In this research paper we have study the different topologies of adiabatic logic such as ECRL, 2N-2N2P and PFAL. The main objective of this paper is to calculate the power consumption, Delay and PDP of the existing adiabatic logic families, and thus compare for the effectiveness in terms of lower power dissipation. All simulations were performed by using HSPICE Simulator at 65nm technology having 10MHz frequency at supply voltage is 1V, for proper validation and verification of the results W/L ratio of all the circuit is kept constant.*

Keywords - *C-CMOS, ECRL, 2N-2N2P, Power, Delay.*

I. INTRODUCTION

With the advancement of the MOS technology, which increased more number of transistors per die with better performance is the main operating feature for the chip manufacturers. Integrating large number of transistors per die area helps in manufacturing to accommodate more components in a single package of the chip and hence decreased not just the size but also has made it inexpensive with lesser delay []1-3]. The huge development in semiconductor industry increases the competition which forced the manufacturers to reduce the size transistors per chip immensely for the economic benefit of semiconductor industry and run towards these goals is increasing exponentially, which also increased the power dissipation consequently [4]. Leakage power consumption of power is dominating factor in chip designing, which reduces the battery life and high on chip temperature in various portable electronics devices, hence, reduces the operating life of IC (Integrated circuits). However, this power consumption is not just a matter of portable electronics, more power consuming IC's also dissipate more heat, which requires more costly cooling solutions e.g. liquid cooling cabinets for desktop computers, resulting into higher overall cost of the device with IC [8] Thus high performance of the circuit which minimize the power consumption is the main requirement for further development of semiconductor industries.

Active and Standby leakage percentage of a microprocessor chip by Intel [5]. In order to maintain overall performance of the chip in DSM technology along with high driving capability with lower supply voltage, this reduces the V_{TH} of the transistor. However, reduction of Threshold Voltage (V_{TH}) results in the exponential increase in as sub threshold Leakage Current (I_{SUB}) as we know that V_{TH} is exponentially proportional to I_{SUB} [6-7]. Sub threshold leakage is the main part of power consumption below 90nm technology. When transistor is in cut OFF region then current flow from drain terminal to source terminal without affecting the channel length of the transistor which increase the leakage current.

Adiabatic Switching

The principle behind adiabatic switching is that, the transitions should be sufficiently slow so that heat is not emitted significantly. This slow transition is achieved when DC power supply is replaced with an AC power clock which can be achieved by a resonance LC driver, an oscillator, a clock generator etc[8] . As we know that, a constant charging current source corresponds to a linear voltage ramp. If the constant current source delivers the charge Q (= CV_{dd}) during the time period T, the energy dissipated in the channel resistance R is given by-

$$E_{diss} = I^2RT = \left(\frac{CV_{dd}}{T}\right)^2 RT = \left(\frac{RC}{T}\right) CV_{dd}^2 \quad (3)$$

From the equation, as the T is increased linearly, power dissipation will decrease linearly. If T is made sufficiently larger than RC, the energy dissipation

will be nearly zero. This is the principle of adiabatic switching.

II. ADIABATIC LOGIC FAMILY

The use of AC power clock as opposed to DC supply makes the adiabatic circuits capable of recovering the stored energy of node capacitors back to the power source, and thus avoiding dynamic power loss almost completely, theoretically. The use of adiabatic logic principle in designing of low power circuits, is growing, and proving to be a better selection in comparison to other conventional circuits. Adiabatic operation usually consists of four phases, with a phase difference of one quarter of a complete period, in each phase. The four phases of operation are Wait [9], Evaluate, Hold and Recovery [Fig. 2] respectively. In the WAIT phase the power clock stays at low (zero) value, maintaining the output at low level, the evaluation logic generates pre-evaluated results. Now, since the power clock is at low level, the pre-evaluated inputs shall not affect the state of the gate. In the EVALUATE phase, power supply ramps up from zero to Vdd gradually, and the outputs will be evaluated based on the results of pre-evaluation logic. In the HOLD phase, power clock stays at high level, which provides a constant input signal for the next stage in pipelining of adiabatic circuits, and maintain the outputs valid for the entire phase. Meanwhile inputs ramp down to low value. In the RECOVERY phase of operation, power supply ramps down to logic zero and the energy of circuit nodes is recovered and transferred back to the AC power source instead of being dissipated as heat [10].

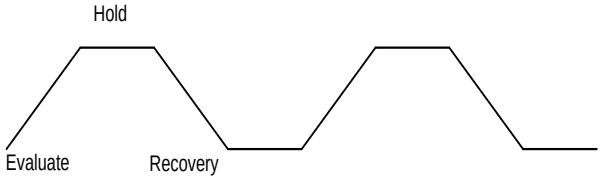

Fig.1. Four Phased Trapezoidal Power Clock

2.1 Efficient Charge Recovery Logic (ECRL)

Basic Efficient Charge Recovery Logic (ECRL) [5] circuit, as shown in Fig. 3, uses two PMOS transistors in cross-coupled fashion, and two NMOS transistors in the functional blocks of ECRL logic circuit. An AC power clock (pck) is used in place of a constant DC supply. Let us first consider, input '**In**' is at high level and '**Inb**' is at low level. At the beginning of a cycle, when power clock 'pck' rises from zero to high level , '**Out**' remains at low level because the high level at '**In**' turns the F - NMOS logic high. '**Outb**' follows the power clock 'pck' through M1. Now when 'pck' reaches to Vdd, the outputs hold valid logic values. In self controlling technique no external signals are applied while in external leakage controlling technique external sleep signal are applied which switches OFF the sleep transistor to reduces the leakage power. The basic idea behind all the proposed techniques is to provide stacking effect of the transistor which mitigates leakage power from V_{dd} to GND. After deep studies of all types of leakage current the validation and verification of results some benchmark circuit are used and test on some other type of circuits like SRAM, Domino circuits, this give the hole detail of leakage current in DSM technology, and for mitigation of leakage current some techniques are also explained [11].

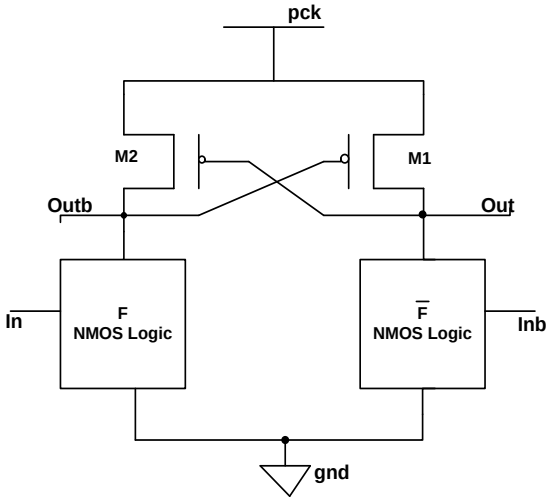

Fig .2. Efficient Charge Recovery Logic (ECRL)

2.2. 2N-2N2P Logic

2N-2N2P Logic is a variation of ECRL Logic family with the difference that two new cross coupled NMOS transistors added parallel to the two existing NMOS transistors. The generalized 2N-2N2P logic diagram is shown in Fig. 4. As the operation is concerned, it is identical to that of ECRL logic family. This new family is derived in order to reduce the effect of coupling in the circuit. Also, the two added NMOS transistors have the advantage of eliminating the floating nodes for a large part of the recovery phase. The added NMOS transistors, however, prevent the circuits form achieving significant power reduction as the ECRL logic family [10-12].

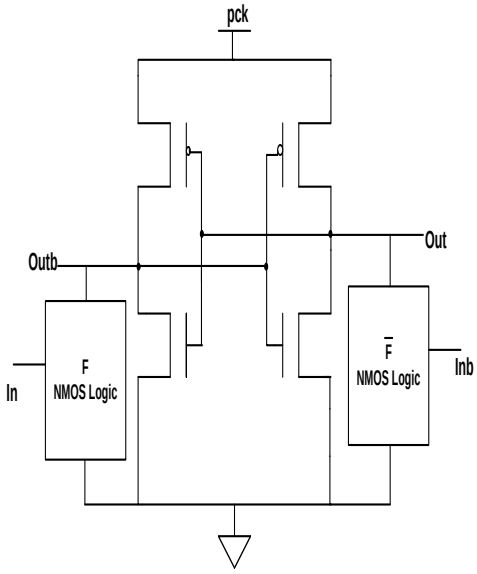

Fig .3. 2N-2N2P Basic Logic circuit

2.3. Positive Feedback Adiabatic Logic (PFAL)

The Positive Feedback Adiabatic Logic (PFAL), of all the three adiabatic logic families, achieves the lowest power. Generalized PFAL logic diagram is shown in Fig. 5. The latch is similar to that of 2N-2N2P logic family with two PMOS transistors and two NMOS transistors in cross coupled fashion. The NMOS logic functional blocks are connected in parallel with the PMOS pull up transistors of the latch, forming the transmission gates. The fact that the functional blocks are in parallel with the pull up transistors, equivalent resistance is smaller during the charging process of capacitance [13-15].

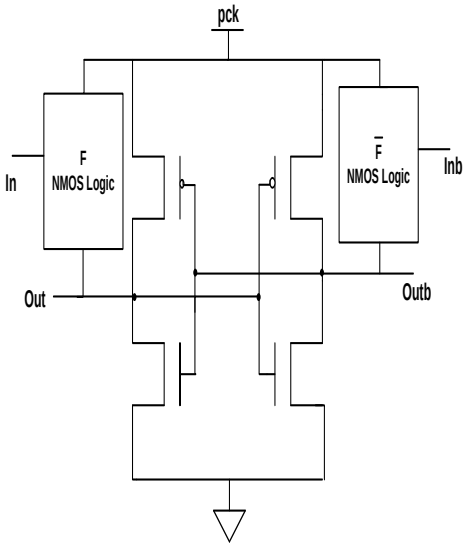

Fig.4. PFAL Basic logic circuit

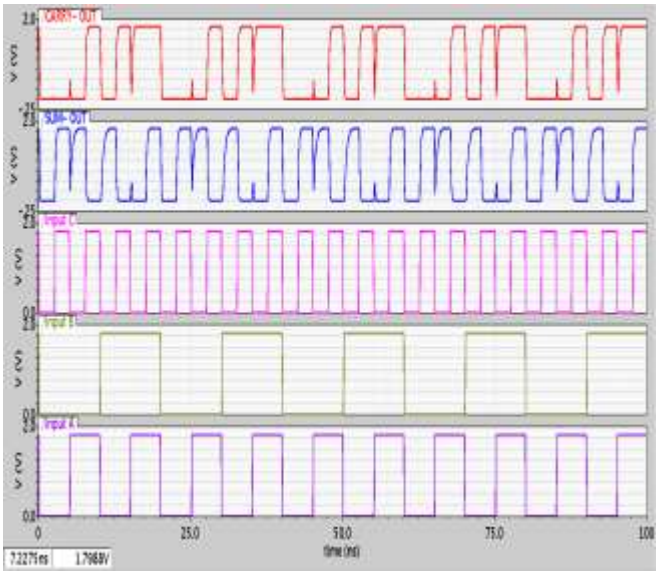

Fig 6. Output Waveform of Proposed Circuit

II. SIMULATION AND RESULTS

All the simulations are done using HSPICE Simulator at '65nm' technology. In Table 1, the design parameters utilized for simulation of circuits have been listed. Different graphs showing the comparison of average power dissipation for the 2n-2N2P, ECRL, PFAL and DCDB-PFAL logic circuits have been plotted. shows comparison of lowest power dissipation achieved using proposed DCDB-PFAL circuits over other ECRL, 2N-2N2P and PFAL adiabatic logic circuits. While shows average power comparison for 2:1 MUX circuit using proposed logic circuit at different values of Vdc over the existing PFAL logic circuit.

It can be seen from the graphs plotted that with the dc voltage varying between 0.1V to 0.3V, power first decreases up till around 0.25V and then increases gradually. The DCDB-PFAL INVERTER consumes up to 91% lesser power over 2N-2N2P INVERTER, 89% lesser power over ECRL Inverter and 48% lesser power as compared to PFAL INVERTER. NAND gate achieves a power reduction of up to 86% over 2N-2N2P logic, 83% over ECRL logic and 43 % lesser power as compared to PFAL NAND gate. NOR gate consumes up to 85% less power than 2N-2N2P logic, 81% less power than ECRL logic and 39% lesser power as compared to PFAL NOR gate. And XOR gate achieves a power reduction of up to 71% over 2N-2N2P logic, 63% over ECRL logic and up to 29% lesser power over PFAL XOR gate. Finally, the 2:1 MUX implemented using proposed DCDB-PFAL logic consumes up to 35% lesser power as compared to existing PFAL logic.

Table.1. The supply voltages used at different technologies.

Tech	45nm	65nm	90nm	120nm	180nm
V_{dd}	.90v	1.00v	1.20v	1.50v	1.80v

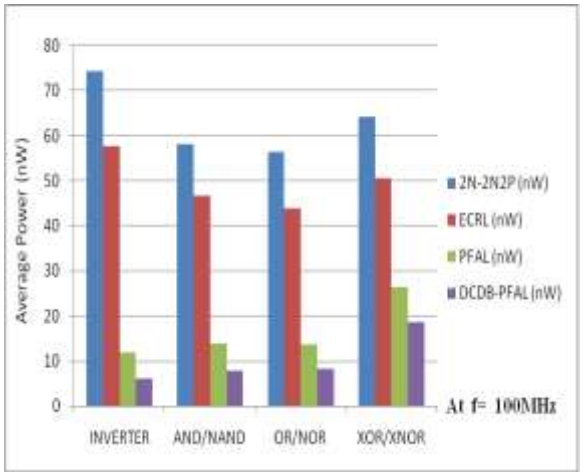

Fig.7. Graph showing average power dissipation for different logic gates using proposed DCDB-PFAL, ECRL, 2N-2N2P, PFAL at 100MHz

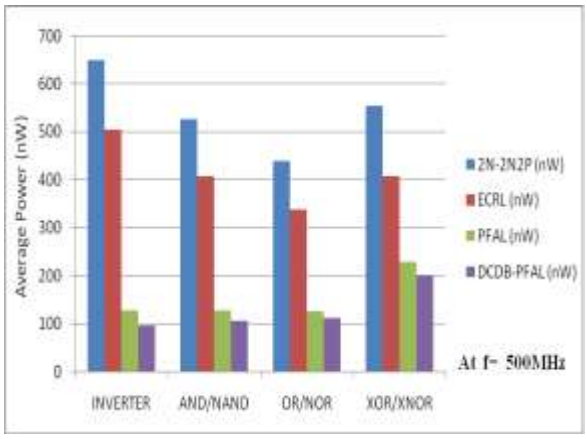

Fig.8. Graph showing average power dissipation for different logic gates using proposed DCDB-PFAL, ECRL, 2N-2N2P, PFAL at 500MHz

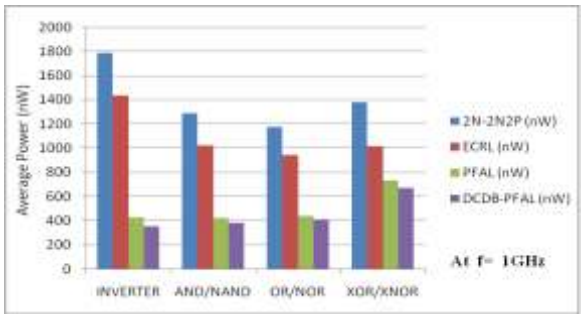

Fig.95. Graph showing average power dissipation for different logic gates using proposed DCDB-PFAL, ECRL, 2N-2N2P, PFAL at 1GHz

IV. CONCLUSION

The prime area of over research is to mitigate leakage power in DSM technology. The leakage power is calculated by measuring I_{SUB} and I_{GATE} current of the transistor which flow when circuit is in ideal condition. In this dissertation we have propose a novel technique of leakage reduction at circuit level. In this technique a external controlling sleep transistor are inserted between PUN and PDN for increasing the resistance of the circuit, which help in mitigation of leakage power. And from the simulations carried out in this paper we have seen that the proposed DCDB-PFAL logic circuits it offers significant power reduction over all other logic families and achieves even better performance and much lower power dissipation than PFAL logic family. Similarly saving of leakage power in ECFRL is 40.19% for Low Vth and 22.75% for High V_{th}, in PFAL 96.91% for Low V_{th} and 96.01% for High V_{th} at 11111 input vectors as compared to NAND gate. The proper validation and verification of results are shown.

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