Leakage Power Reduction Techniques for Nanoscale CMOS VLSI Systems and Effect of Technology Scaling on Leakage Power

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Abstract*—The rise in technology has demanded the use of more and more components on chip. This rise has led to rise in power dissipation and a major challenge for circuit designers**.Due to scaling, the reduction of threshold voltage in CMOS circuits increases the sub threshold leakage current which leads to the static power dissipation. It has been observed that leakage power is the major contributor for power dissipation and directly affecting the battery life of circuits.In order to restrain thisleakage power, a comprehensive study and analysis of various leakage power reduction techniques have been presented in this paper. Also the effect of technology scaling on the leakage power is analysed. MICROWIND tool is used for this approach to analyse the power dissipation at different technologies such as 50nm, 90nm, 120nm and 180nm at a given power supply.*

Keywords—*leakage power, low powerconsumption, LECTOR, Technology scaling.*

I. INTRODUCTION

The scaling of feature size in CMOS technology has been done to meet performance, production and power requirements. The main reason for the scaling of CMOS devices is rapid growth of portable electronic devices. As battery life is the key factor,various studies were performed and leakage power was observed. Leakage power occurs when the devices are in standby mode. As a result, leakage power has been the major area of concern. Leakage power directly depends on leakage current which is dependent on various factors such as operating conditions, circuit family and environmental conditions. The three main components in MOS transistor leakage are gate, sub threshold and junction tunnelling leakage. Sub threshold leakage is the current between the source and drain of a MOSFET when transistor is in sub threshold region or weak inversion region i.e., for gate to source voltage below the threshold voltage. The importance of sub threshold conduction is that the supply voltage has continually scaled down, both to reduce the dynamic power consumption of integrated circuits (the power that is consumed when the transistor is switching from an on-state to an off-state, which depends on the square of the supply voltage), and to keep electric fields inside small devices low, to maintain device reliability. This makes us the study of leakage power an important topic. So several techniques areimplemented to reduce the leakage powerin CMOS VLSI circuits such as Inverter, and NAND.

II. BACKGROUND

i. Sources of Power Consumption in CMOS:

Power in digital circuits, can be analysed according to its peak and average (total) powers. In this paper we have used average power, as peak power, is more related to reliability and performance of the device. The total power consumption in CMOS circuits is due to two types of power: dynamic power and static power. Dynamic power is generated when clock is given as input to logic gates. As capacitance is associated with the gate during this process, power dissipation is caused due to charging and discharging of the gate. Static power is the power that is dissipated when the circuit is idle state. Static power consumption is caused by the leakage currents, while the gates are idle. Leakage currents affect the circuit both during active and idle mode of operations. The leakage power will eventually exceed the active power if no leakage reduction scheme is used.

ii. Effect of Technology Scaling:

In 1975, Gordon Moore noticed that the number of transistors per square inch on integrated circuits had doubled every year since their invention. Moore's law predicts that this trend will continue in the future and the number of transistors since then have doubled approximately every 18 months. In every new process technology most of the device dimensions are scaled to allow higher device density. The important effect of the scaling is the reduction of capacitances, which reduces power and delay. There are two major types of scaling methods for MOSFET devices. One is called Constant Field Scaling (CFS) and the other is Constant Voltage Scaling (CVS). In CFS, all the dimensions of the transistors as well as the supply voltage are scaled down by a factor of S and the doping densities are increased by the same factor to preserve the internal electric field. In CVS, the same scaling down occurs as that of CFS, but, the supply voltage remains unchanged.To maintain the charge-field relationship, the doping densities are increased by a factor of S^2. It

can easily be observed that in case of CFS, the power consumption is reduced by a factor of S^2.

iii. Leakage Power

The two main components that constitute the power dissipation in a CMOS integrated circuit are static power anddynamic power.

Total Power dissipation= $P_{static} + P_{dynamic}$

Static power is the power dissipated when the transistor is not in the switching mode and is generally determined by the formula,

$$P_{static} = I_{static} V_{dd}$$

where V_{dd} is the supply voltage and I_{static} is the total current flowing through the device. In the earlier days, CMOS technology has been advantageous for its low static power. As devices are scaled, gate oxide thicknesses is decreased and probability of tunnelling is increased, which reults in very large leakage currents. This sub threshold leakage current is governed by thermodynamics, more specifically the Boltzmann distribution. Dynamic power is the sum of transient power consumption ($P_{transient}$) and capacitive load power (P_{cap}) consumption. $P_{transient}$ represents the amount of power consumed when the device changes its logic states, 1 to 0 or 0 to 1. Capacitive load power consumption from its name,represents the power used to charge the load capacitance. Putting these together we find that

$P_{dynamic} = P_{cap} + P_{transient} = (C_L + C) (V_{dd})2f N3$

where V_{dd} is the supply voltage and I_{static} is the total current flowing through the device. In the earlier days, CMOS technology has been advantageous for its low static power. As devices are scaled, gate oxide thicknesses decreased, resulting in very large leakage currents. This sub threshold leakage current is governed by thermodynamics, more specifically the Boltzmann distribution. Dynamic power is the sum of transient power consumption ($P_{transient}$) and capacitive load power (P_{cap}) consumption. $P_{transient}$ represents the amount of power consumed when the device changes its logic states, 1 to 0 or vice versa. Capacitive load power consumption as its name suggests,represents the power used to charge the load capacitance. Together we find that

$P_{dynamic} = P_{cap} + P_{transient} = (C_L + C) (V_{dd})2f N3$

where C_L is the load capacitance, C is the internal capacitance of the IC, f is the frequency of operation, and N is the number of bits that are switching. This showsthat as performance increases, due toincrease of speed and frequency of the IC, the dynamic power also increases. Also we know that dynamic power is data dependent and is closely related to the number of transistors that change states. A more hidden component of dynamic power is the loss due to dynamic hazards.

III. MOS LEAKAGE MECHANISM

Sub threshold leakage

Sub threshold leakage or sub threshold drain current is the current between the source and drain of a MOSFET when the transistor is in sub threshold region, when the gate-to source voltages are below the threshold voltage.

Reduction in threshold voltage results in the increase in subthreshold leakage current. One of challenge with technology scaling is the rapid increase in subthreshold leakage power due to V_t reduction. In such a system it becomes crucial to identify techniques to reduce this leakage power component. The development of digital integrated circuits is challenged by higher power consumption [6]. Leakage current has become a primary concern for low-power, highperformance digital CMOS circuits. The exponential increase in the leakage component of the total chip power can be attributed to threshold voltage scaling, which is essential to maintain high performance in active mode, since supply voltages are scaled. Numerous design techniques have been proposed to reduce standby leakage in digital circuits. Leakage power has become a serious concern in nanometer CMOS technologies, and power-gating will be considered to give a solution to the problem with a small drawback in performance. The importance of sub threshold leakage is increasing because the supply voltage is continuously scaling down, to reduce the dynamic power consumption of integrated circuits which in turn is increasing static power dissipation. So it has become a challenge to circuit engineers to reduce leakage power which has become a major source of power dissipation.

In the current paper, we study, analyse and compare various leakage reduction techniques[1], [9] and also study the effect of scaling on the leakage power.

IV. LEAKAGE POWER REDUCTION TECHNIQUES

i. Forced Stack

The Forced stack is a leakage reduction technique which works both in active and stand-by mode. It is based on the fact that two off-state transistors connected in series cause significantly less leakage than a single device[1], [7]. The leakage current of the stack is very small than the leakage of a single device with double channel length. But, in modern deep sub-micron circuits, the threshold voltage may decrease for longer channels due to the reverse short channel effect. Therefore, leakage reduction is not very effective.

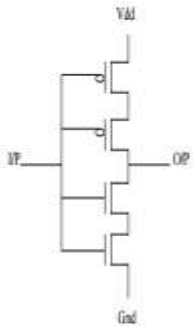

Fig 1: Forced Stack technique

ii. Sleep Transistor

This method provides good reduction in leakage power, but it is a state destructive technique. State -destructive techniques cut off transistor (pull-up or pull-down or both) networks from supply voltage or ground using sleep transistors [8]. These types of techniques are also called gated V_{dd} and gated-GND (We usually use gated clock for dynamic power reduction). The sleep transistors will be turned offwhen the logic circuits are not in use. Because of isolation of the logic networks using sleep transistors, the sleep transistor technique dramatically reduces leakage power during sleep mode. High threshold voltage is used for sleep transistor. Both dynamic and leakage power reductions can be achieved through threshold voltage adjustment.

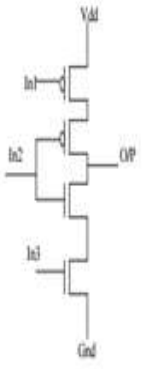

Fig2: Inverter using Sleep transistor

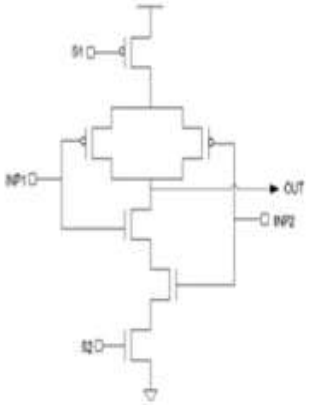

Fig3: NAND using Sleep transistor

iii. Sleepy Keeper

This technique uses the sleep transistors with two additional transistors to save state during sleep mode. Dual threshold voltages can also be applied in the sleepy keeper approach to reduce subthreshold leakage current [6]. But in Sleepy keeper approach, an additional singleNMOS transistor placed in parallel to pull-up sleep transistor connects VDD to the pull-up network. When in sleep mode, this NMOS transistor is the only source of VDD to the pull-up network since the sleep transistor is off. Similarly, to maintain a value of '0' in sleep mode, given that the '0' value has already been calculated, the sleepy keeper approach uses this output value of '0' and a PMOS transistor connected toGND to keep output value equal to '0' when in sleep mode.

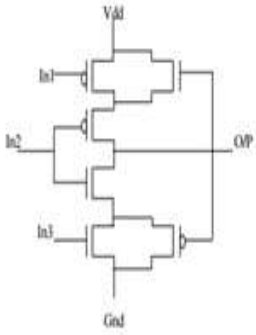

Fig4: Inverter using SleepySleepykeeper[6]

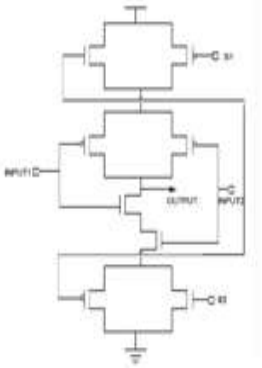

Fig5: NAND using keeper

iv. LECTOR Technique

In this technique, between the pull-up and pull-down networks, we introduce two leakage control transistors within the circuit-a PMOS in pull-up and an NMOS in pull-down in which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. This arrangement will ensure that one of the LCT will always operate in its near cutoff region [7],[8]. The basic idea behind the LECTOR technique for the leakage power reduction is the effective stacking of transistors in the path from supply voltage to ground.

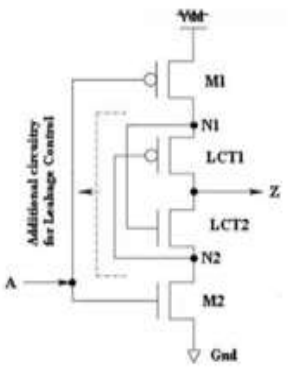

Fig6: LECTOR based Inverter[8]

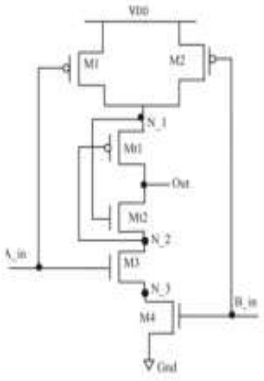

Fig 7: LECTOR based NAND

V. SIMULATION RESULTS

We use microwind tool to design and simulate the circuits such as Inverter, NAND and Adder at layout level using various leakage reduction techniques and compare the results with respect to various parameters such as Static power, Dynamic power, Delay and Area at various technologies such as 180nm, 120nm, 90nm and 50nm and summarize the results.

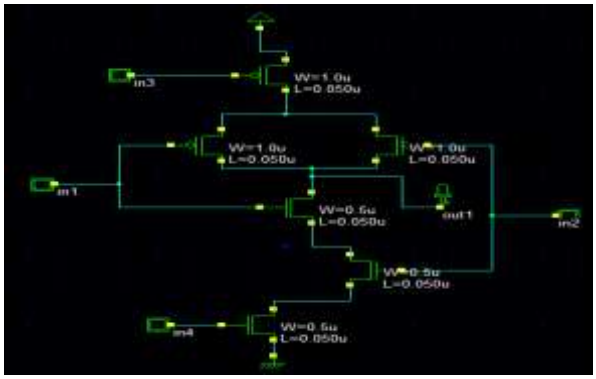

Fig 8: Schematic of 50nm Sleep transistor NAND

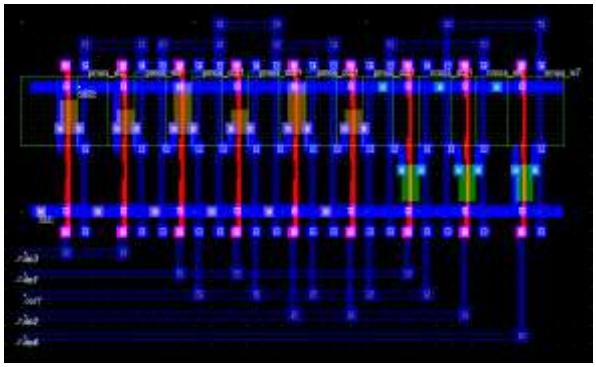

Fig 9: Layout of 50nm Sleep transistor NAND

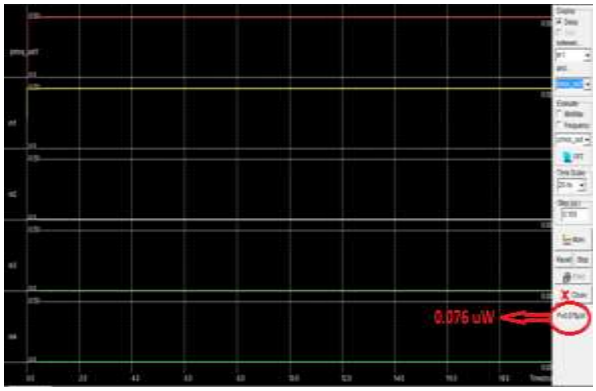

Fig 10: Static power of 50nm Sleep transistor NAND

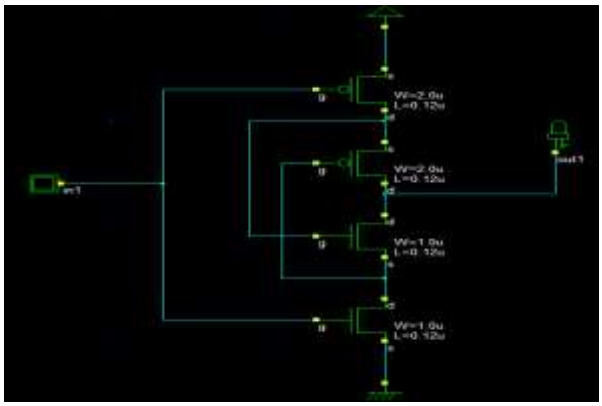

Fig 11: Schematic of LECTOR [2] based Inverter

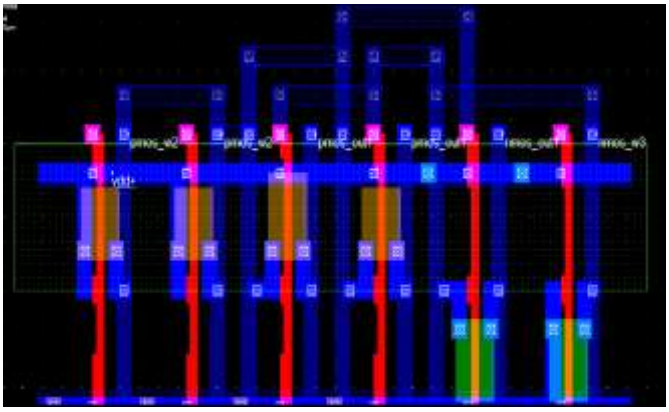

Fig 12: Layout of LECTOR based Inverter

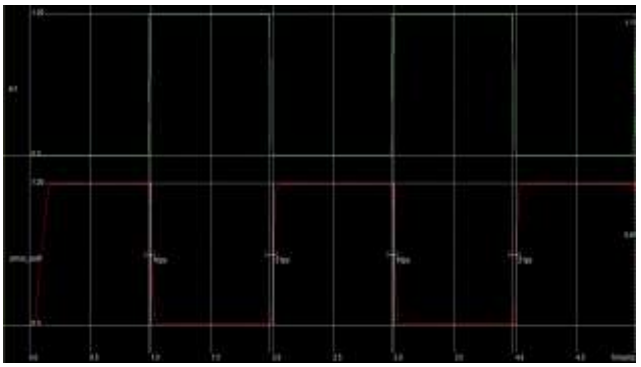

Fig 13: Simulation output of LECTOR based Inverter

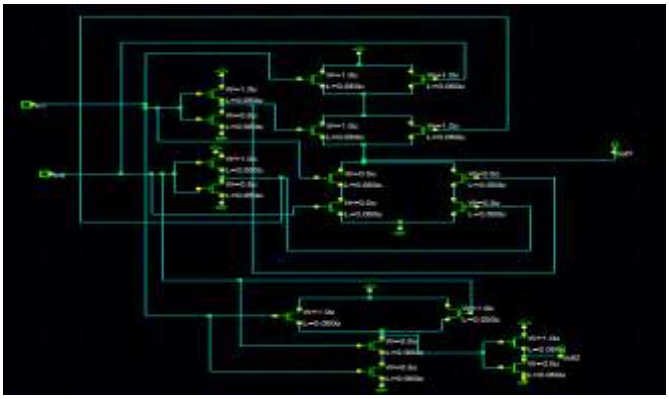

Fig14: Schematic of 50nm Adder

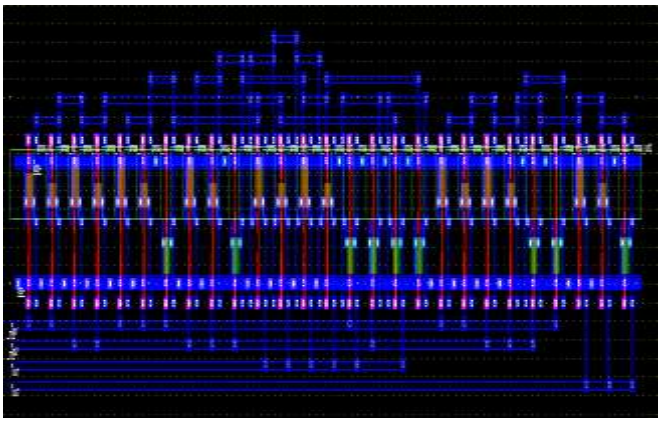

Fig15: Layout of 50nm Adder

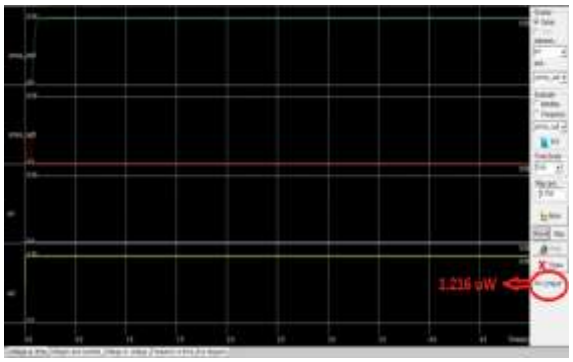

Fig16: Static power of 50nm Adder

TABLE 1

COMPARISON OF ALL THE LEAKAGE POWERREDUCTION TECHNIQUES FOR INVERTERIN 50NM TECHNOLOGY

Technique	Static Power (uW)	Dynamic power (uW)	Total Power (uW)	Area (um^2)	Delay (ns)
Basic inverter	0.117	0.243	0.36	8.6	0.29
Forced stack	0.041	0.209	0.25	17.3	0.51
Sleep transistor	0.049	0.114	0.16	21.7	0.51
Sleepy keeper	0.057	0.137	0.194	36	1.16
Sleepy stack	0.054	0.231	0.285	31.7	0.58
LECTOR	0.035	0.107	0.142	26.3	0.340

TABLE 2

COMPARISON OF STATIC POWER FOR DIFFERENT LEAKAGE POWER TECHNIQUES FOR INVERTER IN VARIOUS TECHNOLOGIES

Technique	180 nm	120 nm	90 nm	50 nm
Basic inverter	3.721	0.484	0.386	0.117
Forced stack	6.902	1.119	0.226	0.041
Sleep transistor	1.859	0.289	0.232	0.049
Sleepy keeper	2.64	0.371	0.299	0.057
Sleepy stack	2.275	0.37	0.303	0.054
LECTOR	1.023	0.187	0.106	0.035

TABLE 3

COMPARISON OF ALL THE LEAKAGE POWER REDUCTION TECHNIQUES FOR NAND CIRCUIT IN 50NM TECHNOLOGY

Technique	Static power (uW)	Dynamic power (uW)	Total power (uW)	Area (um^2)	Delay (ns)
Basic NAND	0.14	0.259	0.399	18.8	0.24
Sleep transistor	0.076	0.176	0.33	33.9	0.44
Sleepy keeper	0.092	0.238	0.272	33.9	0.89
Sleepy stack	0.149	0.409	0.558	70	1.83
LECTOR	0.051	0.136	0.187	27.4	0.44

TABLE 4

COMPARISON OF STATIC POWER FOR DIFFERENT LEAKAGE POWER TECHNIQUES FOR NAND IN VARIOUS TECHNOLOGIES.

Technique	180 nm	120 nm	90 nm	50 nm
Basic NAND	7.959	0.303	0.252	0.14
Sleep transistor	3.328	0.511	0.406	0.076
Sleepy keeper	4.31	0.637	0.565	0.092
Sleepy stack	6.518	1.002	0.874	0.149
LECTOR	2.789	0.368	0.115	0.051

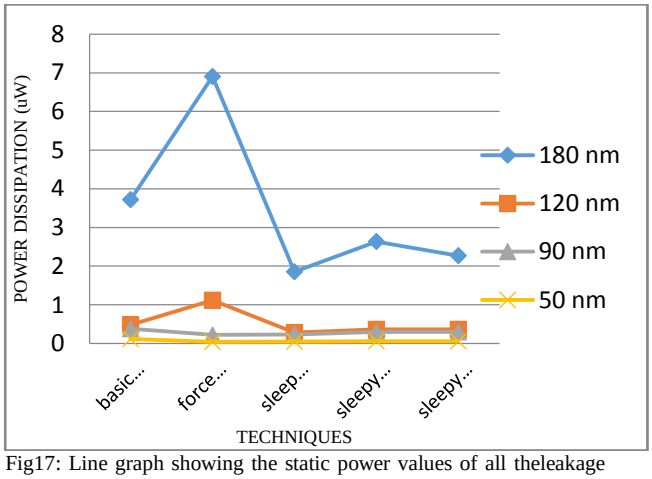

Fig17: Line graph showing the static power values of all theleakage power reduction techniques on Inverter in various technologies.

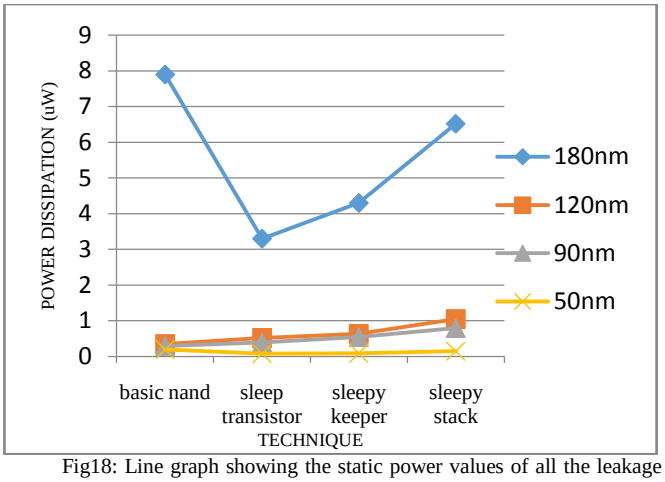

Fig18: Line graph showing the static power values of all the leakage power reduction techniques on NAND in various technologies.

TABLE 5

COMPARISON OF STATIC POWER IN HALFADDER IN VARIOUS TECHNOLOGIES

Technology	Static power (uW)	Dynamic Power (uW)	Total power (uW)	Area (um^2)	Delay (ns)
180nm	46.608	108	154.608	982.1	0.760
120nm	7.139	17.309	24.448	335.7	0.55
90nm	5.715	12.926	18.641	233.1	0.55
50nm	1.216	2.237	3.453	110.2	0.55

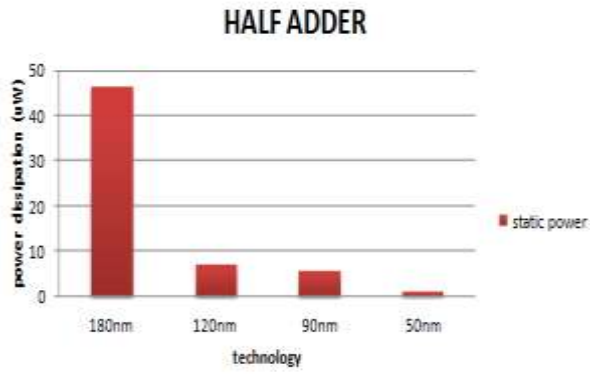

Fig19: Line graph showing the static power values of Half Adder in various technologies

Power-Delay-Product (PDP) is the important parameter to assess the quality and performance of logic circuits. It represents the energy consumed for switching event. It is preferred to have the least value of PDP for the logic circuits.We also compare the Power-Delay Product of Inverter and NAND circuits for different techniques and find that LECTOR circuit gives less PDP.

TABLE 6

PDP OF INVERTER AND NAND CIRCUITS

Technique	PDP(Inverter) (J)	PDP(NAND) (J)
Base case	$3.39e^{-17}$	$3.36e^{-16}$
Forced stack	$2.09e^{-17}$	$3.34e^{-16}$
Sleep transistor	$2.49e^{-16}$	$3.97e^{-16}$
Sleepy keeper	$6.61e^{-16}$	$8.18e^{-16}$
Sleepy stack	$3.13e^{-16}$	$2.72e^{-16}$
LECTOR	$1.19e^{-16}$	$2.24e^{-16}$

VI. CONCLUSION

Sub-threshold leakage power consumption is a great challenge in nanometer scale CMOS technology. Although there are many techniques proposed previously, there is no perfect solution for reducing power consumption. In this project we have analysed various techniques and have compared them with different technologies for different CMOS VLSI circuits. MICROWIND tool is used to design and simulate the circuits at layout level for different technologies and compare the results at different technologies.

By analysing and comparing all these techniques in various technologies on circuits such as inverter, NAND and Adder, we have found that LECTOR circuit has less leakage power, low PDP and also power dissipation decreases as the technology is scaled down to 50nm. The current work is implemented on combinational circuits. This work can be extended further for sequential circuits and also for technology scaling upto 14nm.

REFERENCES

[1] Pushpa Saini and Rajesh Mehra, "Leakage Power Reduction in CMOS VLSI Circuits", International Journal of Computer Applications(0975-8887) Volume 55-No.8,, October 2012.

[2] Narender Hanchate, and Nagarajan Ranganathan, "LECTOR:a technique for leakage reduction in CMOS circuits," IEEE Trans. Very Large Scale Integration (VLSI) Systems, Vol.12, no.2, pp.196-205, February 2004.

[3] Smita Singhal, Nidhi Gau, Anu Mehra and Pradeep Kumar,"Analysis and Comparison of Leakage Power Reduction Techniques in CMOS circuits", 2015 2nd International Conference on Signal Processing and Integrated Networks (SPIN)

[4] Subrat Mahalik, M. Bhanu Teja, "Leakage Power Reduction in CMOS VLSI", International Journal of Engineering Research and Technology (IJERT) ISSN: 2278-0181IJERTV3IS051384 www.ijert.org, Vol. 3 Issue 5, May – 2014.

[5] D.vijayalakshmi, Dr P.C Kishore Raja, "Leakage Power Reduction Techniques in CMOS VLSI Circuits – A Survey", ISSN: 2455-2631, May 2016 IJSDR | Volume 1, Issue 5

[6] Rudraksh Gatkal, Swapnil G.Mali, "Low Power CMOS Inverter in Nanometer Technology", International Conference on Communication and Signal Processing, April 6-8, 2016, India, 978-1-5090-0396-9/16.

[7] https://link.springer.com/chapter/10.1007%2F1-4020-5081-X_4

[8] Vinay Kumar Madasu, B.Kedharnath, "Leakage Power Reduction by using Sleep methods", International of Engineering and Computer Science,ISSN:2319-7242, Volume 2 Issue 9 September 2013 Page No. 2842-2847.

[9] Md.Tauseef, Sudeep Sharma, Rita Jain, "A Survey on Leakage Reduction on Logic Gate in Deep Submicron Technology", International Journal of Engineering Trends and Technology, ISSN:2231-5381, Volume 35 Number 5-May 2016.