

# Comparative Study Of Different Multiplier Architectures

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**Abstract**— This paper presents a comparative analysis of three different multiplier architectures. The three multipliers architecture are array multiplier, a column bypass multiplier, and a array multiplier using Reversal Logic schemes. The multipliers are implemented on Spartan 6 FPGA. The architectures are compared in terms of critical path delay, power dissipation and area. The different multipliers are compared in terms of dynamic power consumption due to the scaling effects on leakage current. Each of the three multipliers has its own trade-offs between power and delay.

**Keywords**— Low Power, Multiplier, Switching Delay, bypassing techniques, reversible logic.

## I. Introduction

Multiplication is one of the most basic function in a various VLSI applications. The multipliers are used in various application like as ,Arithmetic and logic unit in different processors, Digital signal processors (DSP), FIR filters, Math processors, floating point units [3]. Various types of multipliers are available in the literature survey , depending on the requirements different companies are using the various types of multipliers according to their requirement. On the basis of required application, the modified multiplier architecture can be chosen.

It is well known that Multipliers consume maximum power in DSP computations [2]. Hence, it is very important factor for modern DSP systems to design low-power multipliers to reduce the power dissipation. In low-power multiplier design, many researcher experiments & find out results on the reduction of the switching activities [3] have been published. Besides that, a simple and straightforward approach [4] for low-power multiplier is to design a low-power Full Adder to reduce the power dissipation in an array multiplier. The other designs are proposed to reduce the power dissipation in a multiplication operation by interchanging dynamic operands [5] or using partially guarded computation [6]. Furthermore, the minimize of the power dissipation can also be achieved through the architectural modification via row bypassing [7] or column bypassing [8] techniques. Based on the concept of theory row and column bypassing techniques for the reduction of the power dissipation, a low-power 2- dimensional bypassing-based multiplier [9] and a low-power row-and- column bypassing-based multiplier [10] are further proposed. However, the introduction of the extra bypassing circuits

decreases the ability of minimize the power dissipation based on bypass extra bits to next steps..

## II RELATED WORK

The multiplication method for an N bit multiplicand by M bit multiplier is shown below:

$$Y = Y_{n-1} Y_{n-2} \dots Y_2 Y_1 Y_0 \text{ Multiplicand}$$

$$X = X_{n-1} X_{n-2} \dots X_2 X_1 X_0 \text{ Multiplier}$$

Generally process of mathematical,

$$Y = Y_{n-1} Y_{n-2} \dots Y_2 Y_1 Y_0$$

$$X = X_{n-1} X_{n-2} \dots X_2 X_1 X_0$$

=====

$$Y_{n-1}X_0 \ Y_{n-2}X_0 \ Y_{n-3}X_0 \ \dots \ Y_1X_0 \ Y_0X_0$$

$$Y_{n-1}X_1 \ Y_{n-2}X_1 \ Y_{n-3}X_1 \ \dots \ Y_1X_1 \ Y_0X_1$$

$$Y_{n-1}X_2 \ Y_{n-2}X_2 \ Y_{n-3}X_2 \ \dots \ Y_1X_2 \ Y_0X_2$$

.....

$$Y_{n-1}X_{n-2} \ Y_{n-2}X_{n-2} \ Y_{n-3}X_{n-2} \ \dots \ Y_1X_{n-2} \ Y_0X_{n-2}$$

$$Y_{n-1}X_{n-1} \ Y_{n-2}X_{n-1} \ Y_{n-3}X_{n-1} \ \dots \ Y_1X_{n-1} \ Y_0X_{n-1}$$

Example

$$1101 \quad 4\text{-bits}$$

$$1101 \quad 4\text{-bits}$$

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$$1101$$

$$0000$$

$$1101$$

$$1101$$

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$$10101001$$

Generally AND & OR gates are used to generate the Partial Products, PP, If the multiplicand is N-bits and the Multiplier is M-bits then there is N\* M partial product. The way that the partial products are generated or

summed up is the difference between the different architectures of various multipliers.

For CMOS circuits design, the power dissipation can be divided in two category like as static power dissipation and dynamic power dissipation. In general, static consumption is from the leakage current and dynamic consumption is from the switching transient current. For static power dissipation, the consumption is proportional to the number of the used transistors. For dynamic power dissipation, the consumption is provided from the charging and discharging of load capacitance. The average dynamic dissipation of a CMOS gate is

$$P_{avg} = \frac{1}{2} C f V_{dd} N$$

Where C is the load capacitance, f is the clock frequency, VDD is the power supply voltage and N is the number of switching activity in a clock cycle. Hence, it is very important for modern DSP circuit application to develop low-power multipliers to minimum the power dissipation. In this paper we present a technique to reduce power dissipation in digital multipliers, concentrating on the switching activity. There have been proposed a lot of techniques to reduce the switching activity of a logic circuit design.

To reduce the power dissipation of an array multiplier, the simplest approach is to design a full adder (FA) that consumes less power. The other method is to reduce the switching activities by architectural modification via row or column bypassing techniques [5]. The bypassing techniques disables the operation in some rows or columns to minimize the power dissipation. For the parallel multiplier, the array implementation is the Braun's design. The components used in the Braun's design are full adder as well as AND gate.

### III. Simple Array Multiplier

In design of Simple Braun type multiplier, Each partial product is generated by taking into account the Multiplicand and one bit of multiplier each time. The Impending addition is carried out by high-speed carry-save algorithm and the final product is obtained employing any fast adder – the number of partial products depends upon the number of multiplier bits. Tabular form of 4x4 Array multiplier is shown in Fig. 1 4x4 Array multiplier.

The structure of the full adder can be realized using FPGA. Each products can be generated in parallel with the AND gates. Each partial product can be added with the sum of partial product which has previously produced by using the row of adders. The carry out will be shifted one bit to the left or right and then it will be added to the sum which is generated by the first adder and the newly generated partial product. The shifting would carry out with the help of Carry Save Adder (CSA) and the Ripple carry adder should be used

for the final stage of the output [11].

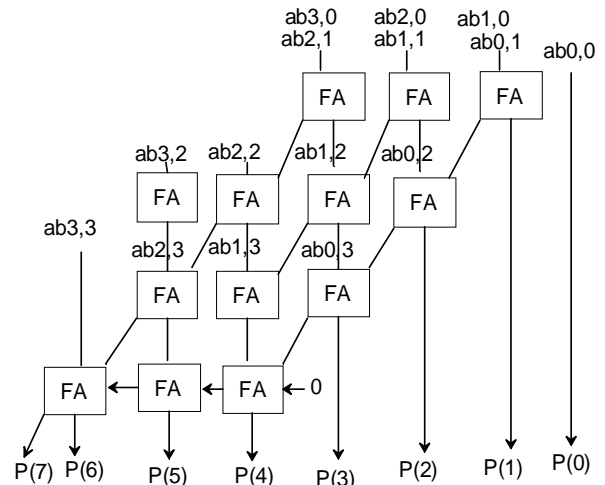


Fig 1 Array multiplier

### IV. Column Bypass Multiplier

We propose a multiplier design in which columns of adders simply are bypassed. In this process, the mathematical operations in a column can be disabled if the corresponding bit in the multiplicand is 0.

A low-power column-bypassing multiplier, the addition multiplication operations in the  $(i+1)$ -th column can be bypassed if the bit,  $a_i$ , in the multiplicand is 0, i. e., all partial products  $a_i b_j$ ,  $0 \leq j \leq n-1$ , are zero. In the multiplier design, the modified Full Adder is simpler. Each modified Full Adder in the Carry Save Adder array is only attached by two tri-state buffers and one 2-to-1 multiplexer. As the bit,  $a_i$ , in the multiplicand multiplier, the addition mathematical calculation in the  $(i+1)$ -th column can be bypassed if the bit,  $a_i$ , in the multiplicand is zero, i. e., So all partial products  $a_i b_j$ ,  $0 \leq j \leq n-1$ , are zero. In the multiplier design, the modified Full Adder is simpler. Each modified Full Adder in the Carry Save Adder array is only attached by two tri-state buffers and one two-to-one multiplexer. As the bit,  $a_i$ , in the multiplicand is zero, their inputs in the  $(i+1)$ -th column will be disabled or reduce and the carry output in the column must be set to be 0 to produce the correct output. Hence, the modification protecting process can be achieved by adding an AND gate at the outputs of the last row [11].

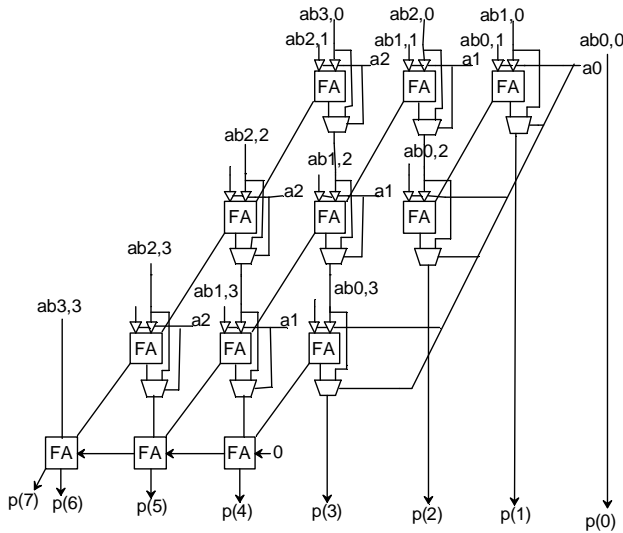


Fig 2 Column bypass multiplier

V. Reversible Scheme Multiplier

In design of Reversible logic, has used as one of the most application approaches for the power optimization with its application in low power requirement of VLSI circuit design. They are also the fundamental requirement for the emerging field operation of the Quantum computing having with applications in the domains like Nano- technology.

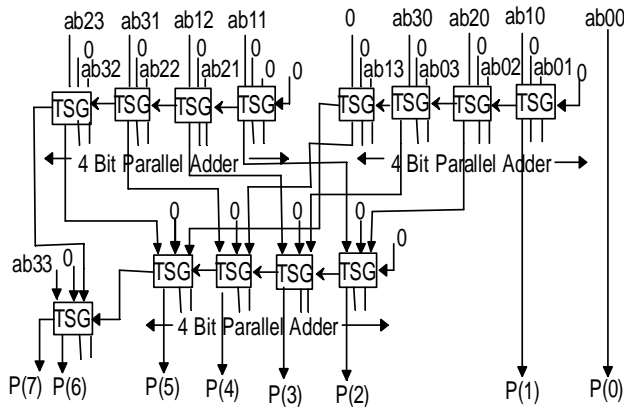


Fig 3 Reversible Multiplier

Modification Reversible logic circuits design have theoretically zero internal power dissipation because they do not lose information, the classical set of gates such as AND, OR, and EXOR are not reversible.

TSG gate is used in place of Full Adder , capable of implementing all Boolean functions and can also work singly as a reversible Full Adder . Figure shows the modification of the proposed gate as a reversible Full adder.

Figure shows the modification of the proposed gate as a reversible Full adder

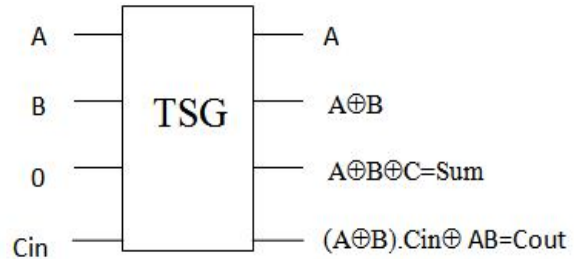


Fig.4 Reversible Full Adder

Researchers worked on new concepts at everyday , generate new concepts & technology which is faster, smaller and more simpler than its predecessor is being developed. The modification in varies clock frequency to achieve greater high speed and increasing in number of transistors & logic family packed onto a chip to achieve complexity of a conventional system results in increased power consumption. Almost all the millions of gates used to perform logical & mathematical operations in a normal computer are irreversible. That is, every time a logical operation is performed some information about the input is erased or lost and is dissipated as heat.

Digital signal processing, VLSI circuits , Communication channel paths. Implementing the reversible logic has the advantages of reducing no. of gate counts, garbage outputs as well as constant inputs. In replacing to normal gates, reversible logic gates have the same number of inputs and outputs signal, each of their output function is equal to 1 for exactly half its input assignments and their fan-out is always equal to 1.

VI. EXPERIMENTAL RESULTS

A. Analysis On Area Overhead of Slices:-

In all type of multiplier designs, to give us an idea of the area & space that will be used, the number of transistors & slices used in the circuit is counted since this directly affects the area. The results are shown in Table 1.

Table 1. Area overhead of different multiplier (4x4)

S.N.	Multiplier	No. of Slices Uses
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1	Simple Multiplier	14
2	Bypass Column Multiplier	15
3	Reversible Gate Multiplier	16

**B. Analysis Power Dissipation**

The main fact of design of multiplier is power, the average dynamic power of each test case were measured and tabulated in Table 2.

Table 2. Power dissipation in different multiplier (4x4) (mW)

S. N.	Multiplier	Dynamic	Quiescent	Total
1	Simple Multiplier	9.14	13.76	22.90
2	Bypass Column Multiplier	7.86	13.76	21.62
3	Reversible Gate Multiplier	8.26	13.76	22.02

**C. Propagation Delay & Switching activity**

For design of multipliers ,have mathematical operations depend on calculation of switching activity . Which the propagation delay, the critical path delay is measured which occurs in the middle of the array. The test cases used travel along this path.

The delay measured for each of the multiplier architecture is shown in Table 3.

Table 3 Delay in different multiplier (4x4) (ns)

S.N.	Multiplier	Power Delay (nS)
1	Simple Multiplier	1 . 443
2	Bypass Column Multiplier	2 . 201
3	Reversible Gate Multiplier	3 . 359

**VII. CONCLUSION**

According to calculations of switching process , analysis of area overhead in transistors, the extra transistors also consume more power in the bypassing-based multipliers. In general, the more the number of additional transistors in the bypassing-based multiplier design, the minimize the ability of the power reduction for low-power design. Besides that, the ability of the power reduction in the Simlpe Full adder-based designs, column bypassing designs and Reversible based designs

depends on the bit patterns of the tested examples. The experimental results show that the column-bypassing design actually consume less power in comparison to the extra bypassing logic circuits and Reversible designs.

The multiplier with Simple braun has less delay compared to the array bypass multiplier, reversible but the Slices count is much higher and the added power from additional logic offsets the power saved. This also happens to the low-cost low-power bypassing based multiplier is performs better in both power and delay compared to Simple & reversible. The low power bypass multiplier performs best in terms of power reduction but worst at propagation delay among the tested multiplier is high. So above discussion in different multipliers in comparison in case of low power Bypass column multiplier better.

**VIII. FUTURE WORK**

In comparison of different Multipliers, Bypass multiplier is better but problem in power delay that can be realises in other multiplier such as row & column bypass, 2 D dimensional multiplier & in used of high speed adder in place of simple full adders methods.

However, since number of logic elements available is large in most of the todays. FPGA this is not considered as a negative point, since power reduction is a prime goal.

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