High Speed CMOS Comparator Design with 5mV Resolution

Raghava Garipelly
Assistant Professor, Dept. of ECE,
Sree Chaitanya College of Engineering,
Karimnagar, A.P, INDIA.

Abstract: **A high speed CMOS comparator with low power and high precision is proposed. The topology is very well capable of distinguishing DC voltage difference of around 5mV, which means a high precision circuit. The proposed circuit operates at a supply voltage of 2V. The circuit is designed to operate at 600MHz. The circuit can be used in high speed ADC devices.**

The proposed circuit is developed on CADENCE gpdk-180 Spectre simulator.

Keywords: **CMOS, resolution, low power, ADC, high speed, level shifting feedback circuit.**

I. BACK GROUND

Now a day's many types of signal processing techniques have indeed moved to the digital domain, though analog circuits have proved fundamentally necessary in many of today's complex, high performance systems. Let us consider some applications where it is very difficult or even impossible to replace analog functions with their digital counterparts regardless of advances in technology.

Processing of Natural Signals:

i. Naturally occurring signals are analog-at least at a microscopic level. A high quality microphone picking up the sound of an orchestra generates a voltage whose amplitude may vary from a few microvolts to hundreds of millivolts.

ii. The photocell in a video camera produces a current that is as low as a few electrons per microsecond.

Since all of these signals must eventually undergo extensive processing in the digital domain, we observe that each of these systems consists of an analog-to-digital converter (ADC) and a digital signal processor (DSP) [Figure 1]. The design of ADCs for high speed, high precision and low power dissipation is one of many difficult challenges in analog design.

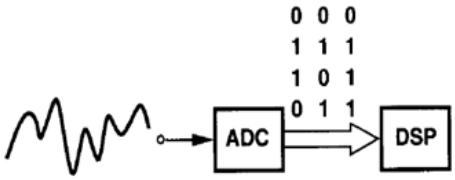

Figure 1: Digitization of a natural signal

II. INTRODUCTION

The recent advancements in technology prove that we are completely working in the digital world, but we know that all the signals in nature are analog. So, it is necessary to have a device, which can convert all the analog signals into digital. For this purpose, we use an Analog-to-Digital Converter (ADC). The basic component in ADC device is a comparator. Lots of comparators have been proposed earlier. The basic comparator consists of three blocks as shown in Figure.2 below.

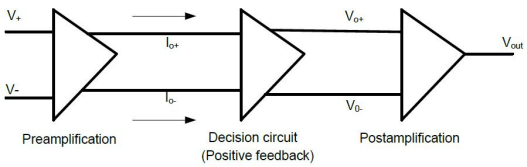

Figure 2: Block diagram of Comparator

Among the circuits proposed in literature, some are concerned with speed [4], some may be emphasizing on low power and high resolution, and some on offset cancellation. In our work, we studied the various proposed literatures and designed an improved one with a view to reduce the comparator size and make it adaptable for high speed. Here, we have come up with a circuit with 5mV

resolution and a supply voltage of 2 V, keeping track with an input clock frequency of 600 MHz. In this process, we have omitted the post amplifier, which is an essential component in the conventional comparator. So, the circuit area is squashed. For proper load drive, we have connected a level shifting feedback circuit.

Bang-Sup Song [2] proposed a comparator circuit with only preamplifier and decision stage, but did not provide any experimental results to analyze the circuit performance. Amalan Nag [1] proposed a comparator with 200 MHz speed and with offset cancellation. We had taken his idea and continued our project by focusing on the speed of the circuit.

Allstot [3] also thought of and simulated a novel comparator circuit which has cascading stages and ended up with a minimum power supply requirement of 3.5 V. The resolution may be higher but achieved at the expense of bulky cascading stages.

III. CIRCUIT DESCRIPTION

A. Conventional Circuit Operation

The block diagram of the basic comparator is shown in Figure 2. This design consists of three stages; the first stage is the preamplifier, followed by a positive feedback or decision stage, and an output buffer. The preamplifier stage amplifies the input signal to improve the comparator sensitivity i.e. it increases the input signal by which the comparator can make a decision and isolates the input of the comparator from switching noise which comes from the decision stage. This is used to determine which of the input signals is large. The output buffer amplifies this information and gives a digital output signal.

a) Pre-amplification

For the preamplifier stage, the circuit is as shown in Figure 3. The circuit is a differential amplifier with active loads. The size of M1 and M2 are set by considering the differential amplifier's transconductance and the input capacitance. The transconductance sets the gain of the stages, while the input capacitance of the comparator is determined by the size M1 and M2. We have concentrated on speed in this design, and hence no high impedance nodes are used in the circuit, other than the input and output nodes. Using the size given in the schematic, we can relate the input voltage to the output currents by

$$io+= \frac{g_m}{s} (vo+ - vo-) + \frac{I_{ss}}{s} = Iss - io- \qquad (i)$$

where gm1 = gm2 = gm

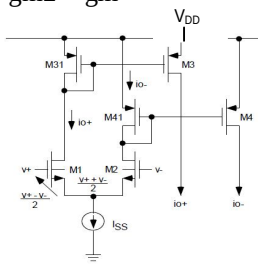

Figure 3: Pre-Amplifier

b) Decision Circuit

The decision circuit is the heart of the comparator and it should be capable of discriminating signals around 10 mV. The circuit used in our design is shown in Figure 4. The circuit uses positive feedback from the cross gate connection of M6 and M7 to increase the gain of the decision element.

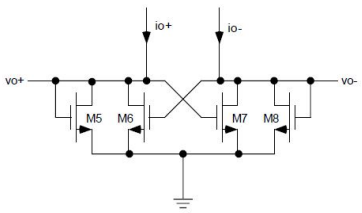

Figure 4: Decision Circuit

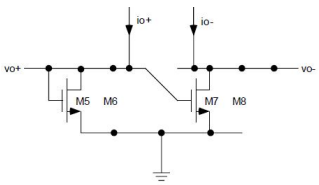

Figure 5: Equivalent Circuit when $v_{o+} > v_{o-}$

Let us begin by assuming that io+ is much larger than io- so that M5 and M7 are ON and M6 and M8 are OFF as in Figure 5. We will also assume that β5 = β8 = βA and β6 = β7= βB. Under these circumstances, vo- is approximately 0 V and vo+ is

$$Vo+ = \sqrt{\frac{2Io+}{\beta A}} + VTHN \qquad (ii)$$

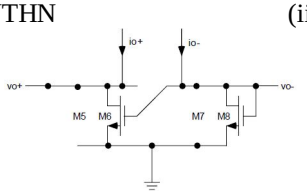

Figure 6: Equivalent Circuit when $v_{o+} < v_{o-}$

If we start to increase io- and decrease io+, the output changes, i.e. switching takes place when the drain source voltage of M7 is equal to VTHN of M6. At this point, M6 starts to take current away from M5. This decreases the drain source voltage of M5 and thus starts to turn M7 OFF as shown in Figure 6. If we assume that the maximum value of vo+ or vo- is equal to 2 VTHN, then M6 and M7 operate, under steady state conditions, in either cut-off or the triode regions. Under these circumstances, the voltage across M7 reaches VTHN, and thus M7 enters the saturation region, when the current through M7 is

io- = (vo+ - vTHN)2 = .io+ (iii)

This is the point, at which switching takes place: i.e. M7 shuts OFF and M6 turns ON. If βA = βB, then switching takes place when the currents io+ and io- are equal. Unequal β's causes the comparator to exhibit hysteresis. A similar analysis for increasing io+ and decreasing io- yields a switching point of io+ = . io- (iv)

Relating these equations to Eq: (i) yields the switching point voltages

vSPH = vo+ - vo- = for βA >= βB (v)

and vSPL = -vSPH

c) Output Buffer

The final component in our comparator design is the output buffer or post-amplifier, which is shown in Figure 7. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal i.e. either a 0(-VDD) or 1(VDD).

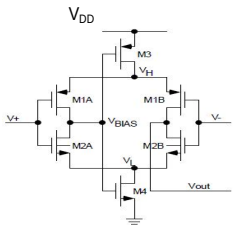

Figure 7: Post-Amplifier/Output-Buffer / Load

The output buffer should accept a differential input signal and not have slew rate limitations. The output buffer used in conventional comparator design is shown in Figure 7. This is a self biasing differential amplifier. An inverter was added at the output of the amplifier as an additional gain stage, to isolate any load capacitance from the self biasing differential amplifier. Figure.8 shows the conventional comparator with three stages. A dc sweep of this configuration is shown in Figure 10. The input vo+ is swept from 0 to 2V, while vo- is held at 1V.

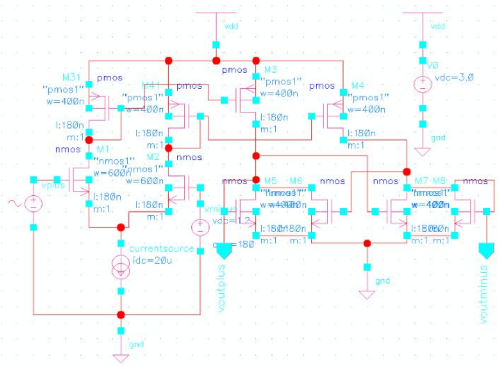

Figure 8: Conventional CMOS comparator circuit design using CADENCE GPDK-180nm

B. Proposed Design

The gates of M14 and M15 are connected to the gates of M6 and M7. So, ultimately increase in VIN will provide large amount of current to flow through M13, which will increase VD of M13 by many fold. So, to compensate the large current flow through M8, the gate of M8 has to increase keeping track with the rising source voltage. Since gate voltage of M8 is same as vo+, the feedback actually reduces response time, and at the same time forcing the higher vo+ to saturate at supply voltage VDD and saturating vo- at almost ground level.

In the proposed circuit Figure 9, we have kept the sizes of all the MOSFETs in decision stage equal, in order to avoid the following problems: First, when we keep the W/L of M8 and M11 as low as possible, these MOSFETs respond only when the gate voltages are increased. But, the incoming currents (from M6 & M7) will be bypassed through M9 and M10. Then the two binary outputs will not be much effected, because they are directly connected to the drains and gates of M8 and M11. This proposal is not desirable. We can go for the reverse case, in which is keeping the W/L of M9 and M10 lower than that of M8 and M11. This proposal will fail when we talk about resolution. Here, the resolution will be increased as an increase in W/L of M8 and M11 will reduce their sinking capability. Next, we tried to keep W/L ratios of M8 and M9 lower than the other two MOSFETs. But in this case, as there is a feedback path in decision stage the circuit may

not respond properly even when the VIN reaches VREF. This idea may give desired results but with slow response, which is also called Delay. So the final decision is to keep equal W/L ratios for all of the transistors at decision stage.

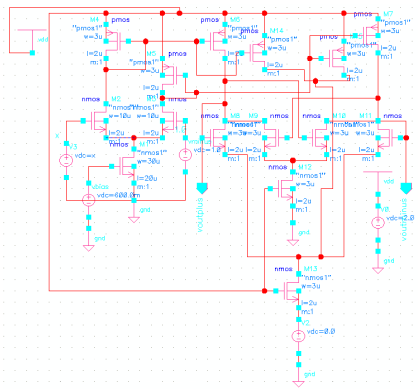

Figure 9: Proposed Circuit

IV. CIRCUIT SIMULATION AND RESULTS

The simulation is done in Spectra CADANCE gpdk-180nm Technology. Figure 10 shows the DC response of the conventional comparator circuit. Figure 11 shows the DC response of the proposed circuit, in which the output is also shown; we get single output because we added a post-amplifier circuit after the proposed circuit. Figure 12 and 13 shows the transient response of the proposed design from which we can understand that the circuit is capable of distinguishing even 5mV of difference between vin and vref and we can say that the circuit achieved the desired speed i.e. 600MHz. We can calculate the speed from the figure by calculating the timing parameters.

Figure 14 shows the power graph of the circuit. From this graph we can calculate the static and dynamic powers of the circuit. The static power is 5.618mW and the dynamic power is 1.216mW. Figure 15 shows the Delay contribution of the circuit. We have calculated the delay contribution of our design, as it has to be embedded in another design, like an ADC. The proposed design takes a delay of 521.1ps to transfer the input to the output. Figure 16 shows the symbol of the proposed design. By using this symbol, one can directly use it in their designs without implementing the overall MOSFETs structure. The DC response of the conventional Comparator circuit is shown in Figure 10.

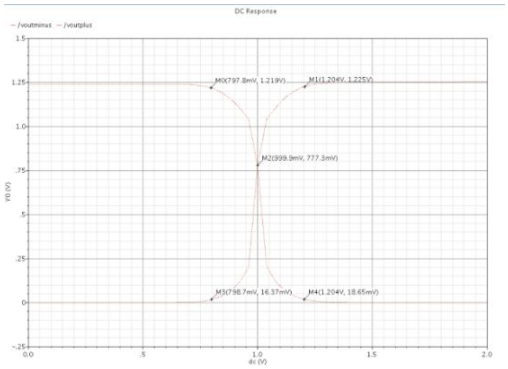

Figure 10: DC Response of the conventional CMOS comparator design

The results of the proposed circuit are show in the following Figures 11-15, and Figure 16 shows the Symbolic structure of our design.

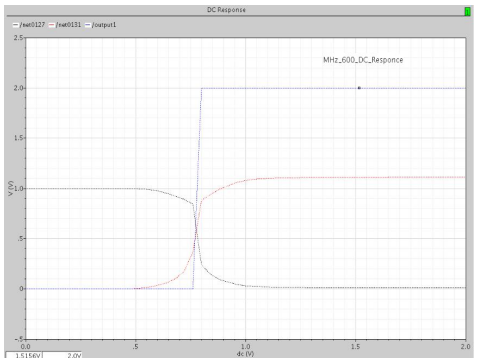

Figure 11: DC response of the Design

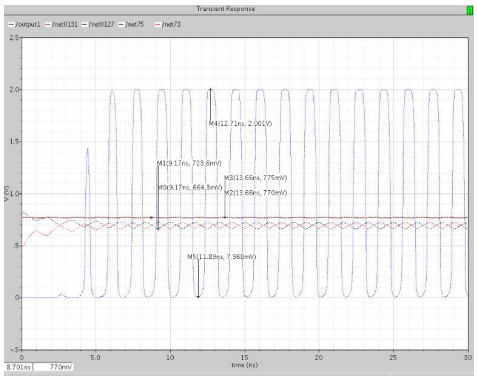

Figure 12: Transient response of the Design

Figure 13: Transient response of the Design

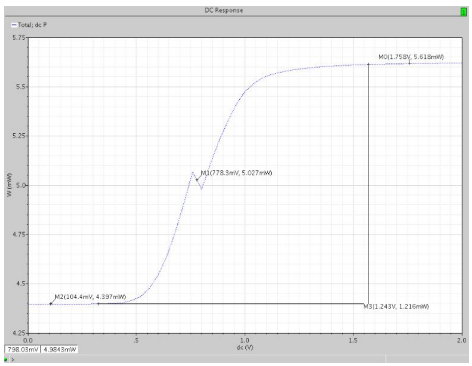

Figure 14: Power Graph of the Design

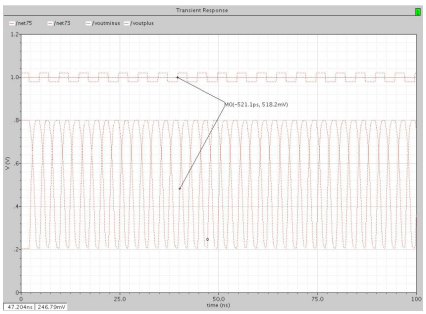

Figure 15: Delay contribution of the Design

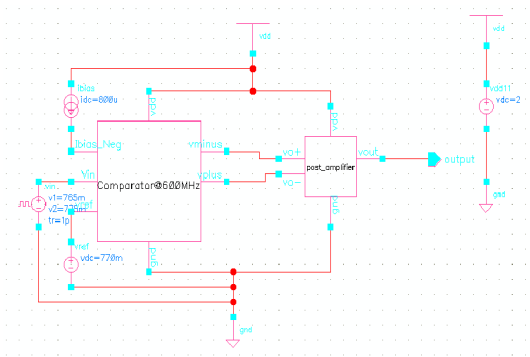

Figure 16: Symbolic structure of the Design

V. CONCLUSION

The proposed circuit is tested and verified in various aspects. The speed, resolution, supply voltage and clock frequency are considered. The circuit is able to resolve small difference in voltage as low as 5 mV when operating at 2V supply voltage, with frequency of 600MHz. This circuit can be widely used in ADC, where speed is desired. We would like to continue our work towards the improvement in the area and power aspects.

TABLE 1: COMPARISON TABLE

DESIGN	SPEED (MHz)	RESOLUTION (mV)
Conventional CMOS Comparator	60	>40
Comparator With Current Sink MOSFETs	<100	40
Comparator With Eexcitory Feedback	200	20
Proposed Design	600	5

VI. ACKNOWLEDGEMENT

The simulations were done by using CADENCE gpdk-180 at Central Institute of Tool Design, Hyderabad. I am thankful to Dr.Sanath Kumar for his guidance throughout the project.

REFERENCES

[1] Amalan Nag, K. L. Baishnab F. A. Talukdar, Member, IEEE ”Low Power, High Precision and Reduced Size CMOS Comparator for High Speed ADC Design” 2010 5th International Conference on Industrial and Information Systems, ICIIS 2010, Jul 29 - Aug 01, 2010, India.

[2] Bang-Sup Song, Seung-Hoon Lee and Michael F. Tempsett ‘‘A 10-b 15- MHz CMOS Recycling Two-step A/D Converter’’ IEEE Journal of Solid- State Circuits, vol. 25, no. 6, December 1990.

[3] David J. Allstot ‘‘A Precision Variable-Supply CMOS Comparator’’, IEEE Journal of Solid State Circuits, vol.sc-17, no.6, Dec.1982

[4] Meena Panchore and R. S. Gamad* ‘‘Low Power and High Speed CMOS Comparator Design Using 0.18µm Technology’’, International Journal of Electronic Engineering Research, ISSN 0975 - 6450 vol. 2 no.1

[5] R. Jacob Baker, Harry W. Li, David E. Boyce, “CMOS- Circuit Design, Layout, And Simulation”, IEEE Press Series on Microelectronic Systems, IEEE Press, Prentice Hall of India Private Limited, Eastern Economy Edition,2002, ISBN 0-471—70055-x

[6] “Design of Analog CMOS Integrated Circuits”, by Behzad Razavi, Tata McGraw Hill Edition 2002, ISBN – 0-07-238032-2