A comparative study of Mixed CNT bundle with Copper for VLSI Interconnect at 32nm

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Abstract— **The aggressive technology scaling in VLSI leads to decrease the size of chip. Such continual miniaturization of VLSI devices has strong impact on the VLSI technology in several ways. The performance of ICs have been increased and the interconnect delay becomes much more significant. Copper interconnects have become a significant performance limiter. Thus to overcome from the limitation of copper Carbon Nanotubes have been proposed as a possible replacement of copper interconnect. Several different configuration of CNT have been proposed out of which Mixed CNT configuration have received much attention for their unique characteristics and as a possible alternative to Cu interconnects in future ICs. In this paper we have compare the Mixed CNT interconnect configurations with copper interconnect. For the first time a compact equivalent circuit model of Mixed CNTs is presented, and the performance of Mixed CNT interconnects is evaluated and compared against traditional Cu interconnects at various parameters.**

Keywords— **Copper (Cu), Carbon Nanotube, Single wall Carbon Nanotube (SWCNT), Multiwall Carbon Nanotube (MWCNT), Mixed Carbon Nanotubes (MCNT)**

I. INTRODUCTION

Development of Integrated Circuits into nanometer scale leads to new challenges for copper. The major challenges are resulted from the steep increase of copper resistivity which is due to surface scattering and grain boundary scattering. The reliability issue due to electromigration, the heat dissipation issue, and the current capacity issue is also effecting the performance. The increase of resistivity in the IC interconnects could result in signal integrity issue, such as long time delay. This steep rise in parasitic resistance of copper interconnects poses serious challenges for interconnect delay especially at the global level where wires traverse long distances and for interconnect reliability , hence it has a significant impact on the performance and reliability of VLSI circuits.

In order to eliminate such problems, changes in the material used for on-chip interconnections have been sought out and the most promising alternative for copper interconnects turns out to be Carbon Nanotube (CNT). The CNTs are grown in the form of seamless cylinders with the walls formed by one atomic layer of graphite (graphene). The diameters of these cylinders are of the order of a nanometer. These tubes are either metallic or semiconductor. For interconnect applications the metallic ones are most suited and useful. There are two configuration of CNTs. Single walled CNT (SWCNT) and Multiwall CNT (MWCNT). CNTs having only one thin wall of graphene sheet are SWCNTs. There are some CNTs which consist of a multiple of concentric SWCNT like graphene tubes. These are termed MWCNT. The metallic CNTs are attractive for interconnect materials because of their high thermal and mechanical stability, thermal conductivity as high as 5800W/mK, ability to carry current in excess of 1014A/m2 current density even at temperatures higher than 200°C and Fermi velocity comparable with that of a metal[1]. It is very difficult to make a good contact with a CNT. The unavoidable contact imperfection increases resistance. CNT resistances in the range 7 KΩ - 100 KΩ have been reported. Such a high resistance is a major disadvantage; if an isolated CNT is used as interconnect. Thus to overcome from this problem and made it circumvented for interconnect application CNT bundles are used instead of isolated ones.

A CNT bundle consists of a large number of electrically parallel isolated CNTs. The result of the parallel connection is considerable reduction of resistance between the ends of the bundle. Therefore, a CNT bundle makes a better interconnect than the isolated counterparts. The type of CNTs in a bundle is generally either SWCNT, MWCNT or Mixed CNT(Mixed SW/MW CNT).

This paper work is aimed to do comprehensive analysis of the performance of Mixed CNT bundle as VLSI interconnects vis-à-vis copper interconnects in a detailed and manner. This analysis is used to identify the parameters of Mixed CNT bundle interconnects that can be exploited to derive maximum benefit from them as well as that give rise to major limitations in their applicability as interconnects.

II. INTERCONNECT CHALLENGES AT NANOSCALE

The continued scaling of semiconductor devices in VLSI integrated circuits means that there is a replacement of many of the traditional materials used. Although, in the past we have seen the replacement of aluminium wires with copper wires due to lower resistance, now copper wires are going through the similar problems due to the increasing resistivity and as a result, wire delay is becoming serious concern among circuit designers and architects. With decrease in cross-section copper interconnect resistivity increases due to surface roughness and grain boundary scattering, causing increase in propagation delay, power dissipation and electromigration. To understand the trend of increasing resistivity, we look at the ITRS roadmap and some of the past works. From ITRS reports, we find that the copper resistivity for future technologies is increasing at a very fast rate as shown in Fig. 1.

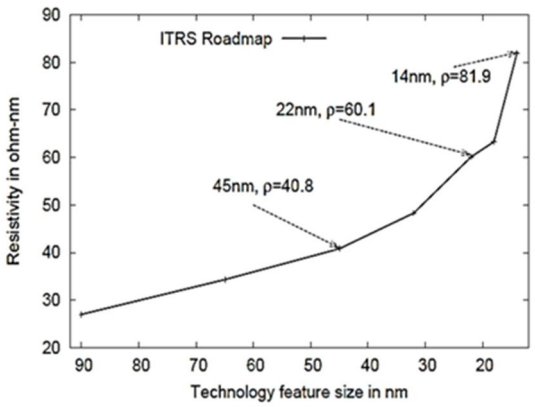

Fig.1:- Resistivity increase as size decreases source from ITRS roadmap. There is a steep increase in resistivity as we move into 32nm and lower technology node [2].

In order to avail the benefits achieved by scaling device dimensions, interconnect induced delay has to be minimized. The challenges from interconnect for nanometer scale VLSI devices have to be addressed through innovative design solutions, circuit & interconnect optimization techniques and material solutions, so that interconnects do not offset the benefits of continued device scaling. Thus to fulfill the demand of future interconnects Carbon Nanotube comes out to be most effective alternative solution and has been recently proposed as a possible future replacement for metal interconnects in future technologies.

Table 1 highlights the five key challenges for the near term (⩾32 nm) and long term (< 32 nm). For the near term, the most difficult challenge for interconnect is the introduction of new materials that meet the wire conductivity requirements and reduce the dielectric permittivity. And for long term, the impact of size effects on interconnect structures must be mitigated.

TABLE 1
Interconnect Difficult Challenges source from ITRS Roadmap [2]

Difficult Challenges ≥ 32nm	**Summary of Issues**
Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Engineering manufacturable interconnect structures, processes and new materials*	Integration complexity, CMP damage ,resist poisoning, dielectric constant degradation. Lack of interconnect /packaging architecture design optimization tool
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.
Three-dimensional control of interconnect features(with it's associated metrology)is required to achieve necessary circuit performance	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials ,reduced feature size, and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features; defect tolerant processes, elimination /reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
Difficult Challenges<32nm	**Summary of Issues**
Mitigate impact of size effects in interconnect structures	Line and via side wall roughness, intersection of porous low-κ voids with sidewall ,barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Three-dimensional control of interconnect features (with its associated metrology)is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at Nano-dimensions.

Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermo mechanical effects. Novel/ active devices may be incorporated into the interconnect.
Identify solutions which address 3D structures and other packaging issues*	3 dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.

**Top three challenges*
CMP—chemical mechanical planarization DRAM—dynamic random access memory

III. INTERCONNECT MODELING

The analysis of copper and Mixed CNT bundle as interconnects for VLSI circuit is done in this section. A model is developed to calculate equivalent circuit parameters for a Mixed CNT bundle and copper based on interconnect geometry. Using this model, the performance of CNT bundle interconnects at global, local and intermediate level is compared to copper wires.

A. *Modeling Parameters of Copper Interconnect*

1) *Resistance*

The resistance per unit length of copper interconnect with rectangular cross-sections were calculated using expression

$$r = \frac{\rho l}{wt} = \frac{(\rho_s + \rho_g)}{wt} l \qquad (1)$$

where the resistivity ρ takes into account the effects due to surface scattering and grain boundary scattering.
Expression for the resistivity is given by

$$\frac{\rho_s}{\rho_0} = 1 + \frac{3}{4}(1-p)\frac{l}{w} \qquad (2)$$

$$\frac{\rho_g}{\rho_o} = 3[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln(1 + \frac{1}{\alpha})] \qquad (3)$$

where

$$\boldsymbol{\alpha} = \frac{\boldsymbol{l}}{\boldsymbol{d}} \times \frac{\boldsymbol{R}}{\boldsymbol{1}} - R$$

2) *Capacitance*

The total effective capacitance of the copper interconnect is given by

$$C_g = \varepsilon \left[\frac{w}{h} + \left\{ 2.22 \left(\frac{s}{s + 0.7h} \right)^{3.19} \right\} + \left\{ 1.17 \left(\frac{s}{s + 1.51h} \right)^{0.76} \left(\frac{t}{t + 0.7h} \right)^{0.12} \right\} \right] \qquad (4)$$

where ε_o is the dielectric permittivity; and ε_r is the relative dielectric permittivity of copper

$$\varepsilon = \varepsilon_r \times 8.86 \times 10^{-12} \qquad (5)$$

Thickness t is determined by t = 3 × W (width of interconnect), s is the space between wires (assumed s=w), h is the height of the wire (h=w × aspect ratio).

3) *Inductance*

The inductance of copper wire with a rectangular cross-section area can be expressed as following

$$L_S = \frac{\mu_0 l}{2\pi} [\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.22(w+t)}{l} \qquad (6)$$

Also Mutual inductance M of copper wire is given by

$$M = \frac{\mu_0 l}{2\pi} [\ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l} \qquad (7)$$

Where μ_o is the permeability and given as $\mu_o = 4\pi \times 10^{-7}$

B. *Modeling Parameters for Mixed CNT Interconnect*

Mixed CNT bundle consist of two types of tubes i.e. SWCNTs and MWCNTs. A mixed SWCNT/MWCNT bundle consists of SWCNTs with a diameter d and MWCNTs with various diameters $D_{inner} \leq d_i \leq D_{outer}$. Since MWCNT have two or more SWCNT, thus no. of shells (N_S) present in MWCNT depends on diameter and is given by

$$N_S = 1 + \frac{D_{outer} - D_{inner}}{2\delta} \qquad (8)$$

where δ=0.34nm (van der Waals distance) is the spacing between adjacent concentric shells. Also D_{outer} and D_{inner} are the maximum and minimum shell diameters. The approximate number of conduction channels per shell for an MWCNT is

$$N_{channel/shell}(d) = (ad+b)\, P_m \quad d > 6nm \qquad (9a)$$

$$= 2P_m \quad d < 6nm \qquad (9b)$$

where a = 0.1836 nm^{-1}, b = 1.275, d is the shell diameter and P_m i.e. probability of metallic tube is equal to 1/3 (similar to an SWCNT bundle) [4].
A new approach for mixed CNT bundle equivalent RLC circuit is shown in fig.2 [5] which contains equivalent circuit of bundle SWCNT and bundled MWCNT interconnects. This circuit model is made by considering three levels in bundles, 1st bottom level of bundle contains

N_A no. of CNTs where $N_A = n_w.2^{nd}$ intermediate level contain N_B no. of CNTs where $N_B = N_A - 1$ and remaining bundle contain N_C no. of CNT which is given by $N_C = n_H - N_A - N_B$, where n_w and n_h are the number of SWCNTs in a row and the height of the bundle, respectively. In this approach metal-nanotube contact resistance (R_C) is at both ends have value vary from zero to hundred kilo-ohms and M (=N_S) represented the no. of shells. If there is no scattering at the contacts or along quantum wire then R_Q is expressed as $h/4e^2 \approx 6.45k\Omega/\mu m$, also L_K and C_{ESC} remains same as of SWCNT. Apart from this, tubes in same or different bundle experience the other capacitance known as coupling capacitance (C_B) that can be expressed as

$$C_B = \frac{\pi \varepsilon l}{\ln\left[\left(\frac{d_{c-c}}{2r}\right) + \left(\sqrt{\left(\frac{d_{c-c}}{2r}\right)^2 + 1}\right)\right]} \quad (10)$$

Where dc-c is the distance between the center of any two CNTs, l is the length of nanotube and r is mean radius of two CNTs [5].

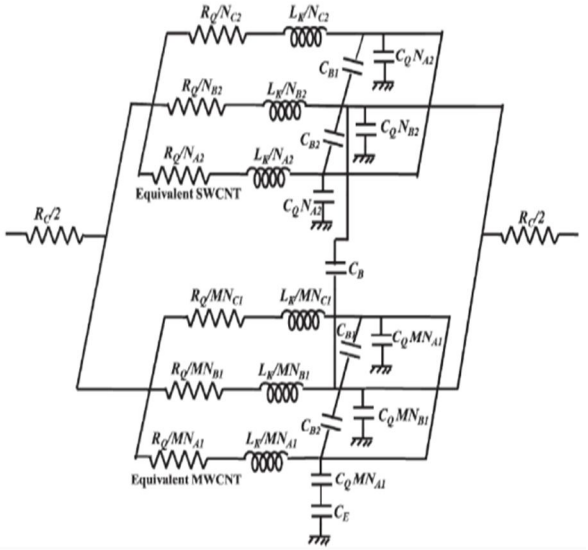

Fig.2: Equivalent RLC model For Mixed CNT Bundle

1) Resistance

The resistance for a mixed CNT bundle is given by

$$R_{mix\ bundle} = \left(\int \frac{N(D_{outer})\partial D_{outer}}{R_{MWCNT}(D_{outer}, l)}\right)^{-1} \quad (11)$$

where $R_{MWCNT}(D_{outer}, l)$ is total resistance of MWCNT & $N(D_{outer})$ is the tube count for given D_{outer}, for N_{bundle} CNTs in the bundle it is expressed as

$$N(D_{outer}) = \frac{N_{bundle}}{\sigma_{D_{outer}}\sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{D_{outer} - \overline{D_{outer}}}{\sigma_{D_{outer}}}\right)^2\right] \quad (12)$$

where $\overline{D_{outer}}$ is mean diameter [4].

2) Capacitance

The inter shell coupling capacitance C_c in an MWCNT and the electrostatic coupling capacitance C_E between two adjacent CNTs are considered along with the electrostatic capacitance of the outermost shells of the bundle. Thus the total capacitance of the mixed CNT bundle after including C_{int} will be given by

$$\frac{1}{C_{bundle}} = \frac{1}{C_{QSWCNT}} + \frac{1}{C_{ESWCNT}} + \frac{1}{C_{MWCNT}} + \frac{1}{C_{int.bundle}} \quad (13)$$

where C_{QSWNT} & C_{ESWCNT} are quantum and electrostatic capacitance of SWCNT, C_{MWCNT} = total MWCNT capacitance and $C_{int.bundle}$ is inter-CNT coupling capacitance and is given by

$$C_{int.bundle} = \frac{2\pi\varepsilon}{\ln(\frac{b}{a})} \quad (14)$$

were 'a' is inner CNT radius & 'b' is the radius of circle formed by outer CNT[6]

3) *Inductance*

The inductance of Mixed CNT arises from two source magnetic inductance (L_M) of mix bundle and the kinetic inductance (L_K) of mix bundle. The total kinetic inductance of a mixed bundle is the parallel inductance value of all the conduction channels in the bundle and is given by

$$L_{K\ mix\ bundle} = \frac{L_{K\ channel}}{N_{channel,bundle}} \quad (15)$$

were

$$N_{channel,bundle} = \sum_{D_{max}} N(D_{outer}) \times \sum_{D} N_{\frac{channel}{shell}}(d) \quad (16)$$

Also magnetic inductance L_m is calculated using the equivalent conductivity method [7].

IV. COMPARATIVE ANALYSIS OF INTERCONNECT BASED ON PARAMETERS AND EQUIVALENTS CIRCUIT DESCRIBED PREVIOUSLY

In this section, two parameters resistance and delay of Cu with mixed CNT are studied on the basis of parameters describe in above sections.We measured the resistances of the Local, Intermediate and Global interconnects, also delay and energy delay product (EDP) for intermediate interconnect is done by considering the geometries suggested in [8, 9] for 32nm.

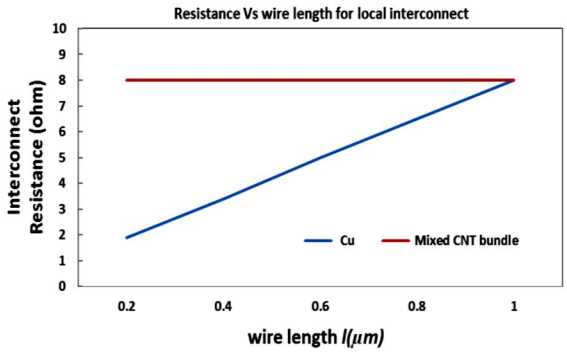

Fig.3 (a): Comparison of resistance of Mixed CNT bundle of Mixed CNT bundle with Cu for local interconnect length at 32 nm node

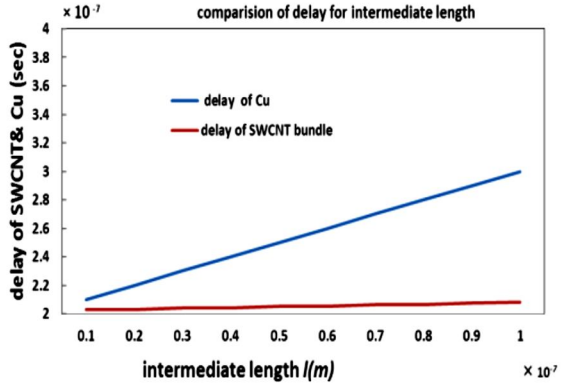

Fig.3 (b) Comparison of resistance with Cu for semiglobal interconnect length at 32 nm node.

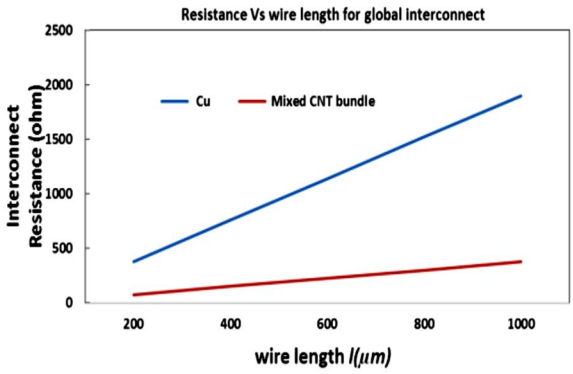

Fig.3(c) Comparison of resistance of Mixed CNT bundle with Cu for global interconnect length for 32 nm node.

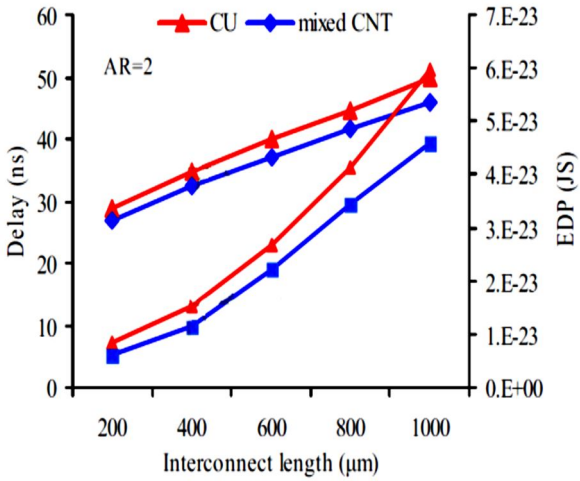

Fig.4 Delay & energy delay product (EDP) performance comparison of Cu and mixed CNT bundle for intermediate interconnect

From Figure 3(a) we see that the CNT bundle Local interconnect have higher resistance as compared to Cu. This is because at local level ($l \leqslant \lambda$) the CNTs in the bundle operate in the ballistic region and has a high value of length independent intrinsic resistance associated with them, whereas the Cu interconnect resistance varies with length simply . Figure 3(b) and Figure 3(c) depicts that the resistances of Intermediate and Global interconnects for CNT bundle is smaller than Cu. This is because surface scattering of electrons, enhanced grain boundary scattering, and presence of highly resistive diffusion barrier layer cause sharp rise in the resistivity of Cu interconnects when the dimensions are of the order of MFP (around 40nm) of electrons in Cu [1]. It has been observed from Fig. 4 that mixed CNT bundle interconnect outperforms the Cu interconnects performance in terms of delay and energy delay product (EDP) for very long interconnect lengths [10].

V. CONCLUSIONS

In this paper we have compare the Mixed CNT interconnect configurations with copper interconnect. From analysis we have found that the mix bundles of CNTs have smaller resistances for Intermediate and Global interconnects but for Local interconnect, the CNT bundle resistance is much higher than Cu. Thus by analysis of graphs we observed that the resistance of CNT bundle interconnects can be optimized by varying the average diameter of CNTs and by varying density of tubes in the bundle. Also we observe that mixed CNT bundle interconnect outperforms the Cu interconnects performance in terms of delay and energy delay product (EDP) for very long interconnect lengths. Thus we can say that to overcome from the limitation of copper, Carbon Nanotubes have a great potential and a possible replacement of copper interconnect.

REFERENCES

[1] Davood Fathi and Behjat Forouzandeh, "Interconnect Challenges and Carbon Nanotube as Interconnect in Nano VLSI Circuits".OnlineAvailable:http:// www.intechopen.com / books/ carbon nanotubes

[2] International Technology Roadmap for Semiconductors, 2005.Online Available: http://public.itrs.net

[3] A. G. Chiariello, A. Maffucci, G. Miano and F. Villone , High Frequency and Crosstalk Analysis ofVLSI Carbon Nanotube Nanointerconnects, 2009 IEEE.

[4] Sudeep Pasricha, Nikil Dutt, Fadi J. Kurdahi, "Exploring Carbon Nanotube Bundle Global Interconnects for Chip Multiprocessor Applications", 2009 22nd International Conference on VLSI Design.

[5] Manoj Kumar Majumder,B.K Kaushik, S.K Manhas and Jainender Kumar, "Analysis of cross talk delay and power dissipation in Mixed CNT Bundle Interconnects", 2012 International Conference on Communications, Devices and Intelligent Systems (CODIS).

[6] P. Uma Sathyakam, Member,and P. S. Mallick, "Effect of realistic Inter-CNT Coupling Capacitance in mixed CNT bundle" , Nanoscience, Technology and Societal Implications (NSTSI), 2011 International Conference.

[7] W. Wang, et al. "Inductance of mixed carbon nanotube bundles," Micro & Nano Letters, IET , vol.2, no.2, pp.35-39, June 2007.

[8] N. Srivastava, et al, "Carbon Interconnects: Implications for Performance, Power Dissipation and Thermal Management", ieeexplore.ieee.org/iel5/10701/33791/01609320.pdf , 2005.

[9] H. Li, et al, "Modelling of Proceedings of Asia-Pacific Microwave Conference 2006.Carbon Nanotube Interconnects and Comparative Analysis with Cu Interconnects", in the

[10] S.D.Pable, Mohd.Hasan and Mohd.Ajmal Kafeel,"Performance Analysis of Ultra Low-Power Mixed CNT Interconnects for Scaled Technology",2011 International Symposium on Electronic System Design.