Comparison of Current Modes in CMOS Analog Multipliers

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***Abstract*— A study and comparison between current mode CMOS analog multiplier, ±1.5 V High frequency four quadrant current multiplier and ±1.2 V High frequency four quadrant current multiplier has been carried out in this paper. Current multiplier has been simulated in SPICE with 0.35µm and 0.5µ m technology. Simulation has been done with supply voltage of 3.3V,1.5V and 1.2V respectively. The simulated results show that characteristic of multipliers are linear with 10µA, 30µA and 20µA input range respectively and power dissipation of ±1.2 V High frequency four quadrant current multiplier is less as compared to the other circuits in 0.35 µm and 0.5 µm technology. These circuits are widely used for analog signal processing application.**

Index temrs---CMOS analog multiplier,current mode in 0.35µm and 0.5µ m technology

I. INTRODUCTION

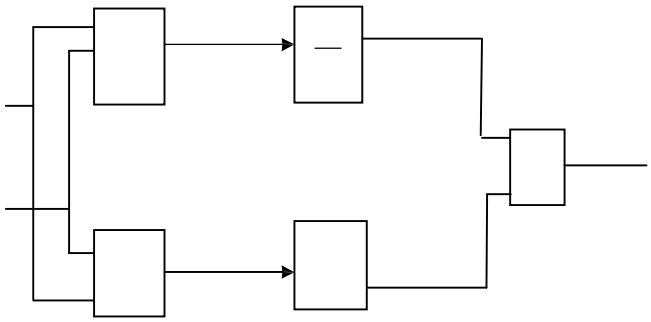
Multiplication of two signals is one of the most important operations in analog signal processing. The multiplier is not only used as a computational building block but also as a programming element in system such as filters, mixers, synthesizers, converter and modulators in communication systems. These are also important for non-linear analog signal processing functions finding application in adaptive filtering, modulation, fuzzy integrated system, frequency translation, automatic gain controlling and neural network . Current multiplier can be designed either using transistor in linear region, in saturation region.

Main feature of standard CMOS fabrications are simplicity, low voltage operation, low power consumption and wide dynamic current range. In addition it is insensitive to temperature and process variation .

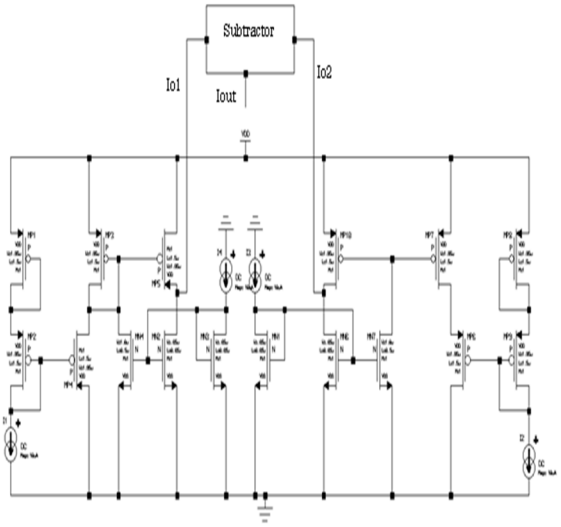
II. CIRCUIT DESCRIPTION

The principle of operation of the multiplier is based on the square-difference identity. There are three steps as shown in fig.1. and described as below:

1. Sum and subtraction both inputs.
2. Take the square of terms of first step and divided it by a constant current i.e. 4I.
3. Subtraction of second step with each other that output can be expressed as [4]



Current-mode squarer circuit based on the dual translinear loop. The circuit consists of two dual translinear loops. The first loop transistor Mp1 to Mp4 provides a (X-Y) input function to the squarer circuit provides output (X-Y)2. The second loop transistor Mp6 to Mp9 provides a (X+Y) input function to the squarer circuit provides output (X+Y)2



. A ±1.5 V High frequency current multiplier

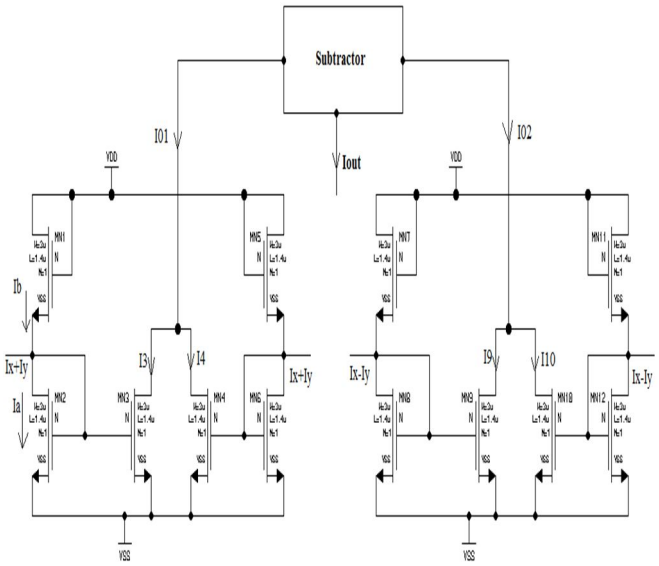
Four quadrant CMOS current multiplier categorized into two groups: (1) Switched-capacitor approach

(2) Continuous time approach.

In continuous time approach transistor could be biased in weak or strong inversion region. Generally transistor operates in saturation region because the square-algebraic identity can be easily realized [3].

shows the four quadrant current multiplier. By using quadratic relation between the input and output currents.

Thus output current is multiplication of current Ix and Iy with multiplication gain factor determined by the transconductance parameter and the supply dependent parameter [4].



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4 (MP1, MN1 and MN3) where the relationship between the input current, Iin, and the output current, Iout, are quadratic [5]. The quadratic cell consists of MN1 and MP1 which both of them operate at triode region and MN3 which operate at saturation region. If MN1 and MP1 have the same transconductance i.e.

III. THE MULTIPLIER CIRCUIT

The goals of adopting differential balanced current

signals are:

x_to increase the linearity trough the cancellation of

the even order harmonics;

x_to lower the interference and noise effects.

A generic differential current signal I is balanced if

it is possible to express it as the difference of two
signal components I+ and I-:

$$I = I^{+} - I^{-} = x \cdot I_B$$

where

$$I^{+} = \frac{1}{2} I_B (1 + x) \quad \text{and} \quad I^{-} = \frac{1}{2} I_B (1 - x),$$

IB is a bias term and x is the value of the variable to be coded.

We set IB (i.e. the bias current) at 250nA, the information carrying value x varies in the range [-1,+1], I- and I+ vary in the range [0 y 250nA], I in the range [-250nA y 250nA].

The four quadrant synaptic multiplier multiplies the input x (x varies in the range [-1 y + 1]) times the weight value w (w varies in the range [-1 y + 1]) as follows:

$$I_{Syn} = x \cdot w \cdot I_B$$

where Isyn is the output synaptic current. Both the input and the weight values are coded by differential and balanced current mode signals.

Following the translinear principle [4] and [5], the basic circuit schema of the four-quadrant translinear multiplier is shown in Figure 1. The two type-A Translinear Loops (TLs) are evidenced: TL1 is formed by M5, M6, M9 and M10, TL2 is formed by M6, M7, M8 and M9.

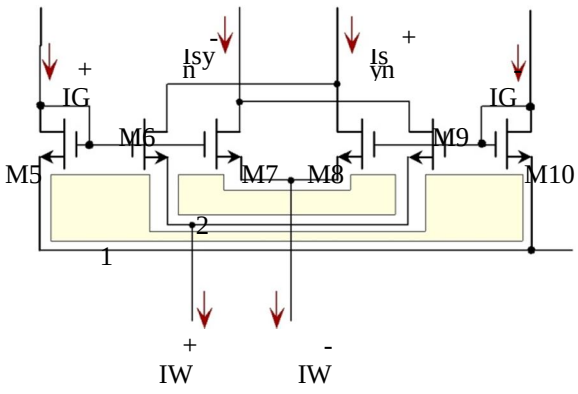

Figure 1: Basic circuit schema of the four-quadrant translinear multiplier.

The meaning of the circuit variables is the following:

x_IG+ and IG- are the positive and the negative input current components;

x_IW+ and IW- are the positive and the negative weight current components;

ISYN + and ISYN- are the positive and the negative output current components.

If all the transistors work in weak inversion and saturation region, we can write: IB is a bias term and x is the value of the variable to be coded.

$$I_{M5} = I_{M6} + I_{M9} = I_{M6} + I_{M10}, \quad \text{from TL1}$$

$$I_{M6} + I_{M8} = I_{M7} + I_{M9}, \quad \text{from TL2}$$

Moreover:

$$I_G^{+} = I_{M5}, \quad I_G^{-} = I_{M10}$$

$$I_{M6} = I_{W+} - I_{M9}, \quad I_{M7} = I_{W-} - I_{M8}$$

Taking into account the coding of information (see above):

$$I_G^{+} = \frac{(1+x) I_B}{2}, \quad I_G^{-} = \frac{(1-x) I_B}{2},$$

$$I_G = I_G^{+} - I_G^{-} = x \cdot I_B$$

$$I_W^{+} = \frac{(1+w) I_B}{2}, \quad I_W^{-} = \frac{(1-w) I_B}{2},$$

$$I_W = I_W^{+} - I_W^{-} = w \cdot I_B$$

we can derive the expression of the currents flowing in the transistors of the two TLs:

$$I_{M6} = \frac{(x + w + x \cdot w + 1)}{4} I_B,$$

$$I_{M7} = \frac{(-x + w - x \cdot w + 1)}{4} I_B$$

I M 8 (x w _ x _w _1) B , 4

I M 9 (_x w _ x _ w _1) B 4

Since I Syn I M 6 _ I M 8 and I Syn _ I M 7 _ I M 9 , the positive and negative components of the four-quadrant translinear multiplier output current are:

I Syn _ (1_ x w) I B and I Syn _ (1_ x w) I B (1)

The output current is:

I Syn _ _ I Syn _ x w I B (2)

RESULTS AND DESCRIPTION

The low voltage CMOS analog multiplier, A ±1.5 V High frequency four quadrant current multiplier and A ±1.2 V High frequency four quadrant current multiplier have been simulated in SPICE with 0.35µm and 0.5µm technology with supply voltage of 3.3V, 1.5V and 1.2V respectively. Table 1. shows the result of power dissipation, output current and current range of these multipliers. Table1. shows that power dissipation of ±1.2 V High frequency four quadrant current multiplier is less in 0.35µ m as well as in 0.5µ m technology as compared to other circuit. Fig.5 and fig.6. shows that d.c. transfer characteristics of low voltage CMOS analog multiplier are linear with 10µA input range and input voltage is 3.3V in 0.5µm and 0.35µm technology respectively. Fig.7. and fig.8. shows that d.c. transfer characteristics of A ±1.5 V High frequency four quadrant current multiplier also linear with 30µA input range and input voltage is 1.5V in 0.5µm and 0.35µm technology. Fig.9. and fig.10. shows that d.c. transfer characteristics of A ±1.2 V High frequency four quadrant current multiplier also linear with 20µA input range and input voltage is 1.2V in 0.5µm and 0.35µm technology

IV. CONCLUSION

The low voltage CMOS analog multiplier, A ±1.5 V High frequency four quadrant current multiplier and A ±1.2 V High frequency four quadrant current multiplier has been studied and simulated in SPICE with 0.35µm and 0.5µm technology with supply voltage 3.3V, 1.5V and 1.2V. The d.c. transfer characteristics of low voltage CMOS analog multiplier, A ±1.5 V High frequency four quadrant current multiplier and A ±1.2 V High frequency four quadrant current multiplier are linear with 10µA, 30µA and 20µA input range respectively.

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