A Novel Approach to Implement a Vedic Multiplier for High Speed Applications

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Abstract: Now-a-days in VLSI technology speed optimization plays a vital role. So designing of high speed devices became necessary to fulfill the end user requirements. Generally the processor designing is mainly depending upon the MAC units. In that particularly multiplier architecture comes under crucial designing. In this paper the VEDIC multiplier (Nikhilam Sutra) which is very ancient multiplier whose importance is discussed. The design of multiplier consists of Radix Selection Unit, Exponent Determinant (ED), Mean Determinant (MD) and Comparator. In this paper the Xilinx ISE EDA Tool is used for synthesis and simulation. Ultimately the multiplier shows the product of the provided inputs with reduced latency along with optimized power estimation.

Keywords: Vedic Mathematics, partial product, Exponent & Mean determinant, Xilinx.

1. Introduction

The speed of a processor greatly depends on its multiplier's performance. This in turn increases the demand for high speed multipliers, at the same time keeping in mind low area and moderate power consumption. Over the past few decades, several new architectures of multipliers have been designed and explored. Multipliers based on the Booth's and modified Booth's algorithm is quite popular in modern VLSI design but come along with their own set of disadvantages. In these algorithms, the multiplication process, involves several intermediate operations before arriving at the final answer. The intermediate stages include several comparisons, additions and subtractions which reduce the speed exponentially with the total number of bits present in the multiplier and the multiplicand. Since speed is our major concern, utilizing such type of architectures is not a feasible approach since it involves several time consuming operations.

In order to address the disadvantages with respect to speed of the above mentioned methods, and explored a new approach to multiplier design based on ancient Vedic Mathematics. Vedic Mathematics is an ancient and eminent approach which acts as a foundation to solve several mathematical challenges encountered in the current day

scenario. Vedic Mathematics existed in ancient India and was rediscovered by a popular mathematician, Sri Bharati Krishna Tirthaji.

He bifurcated Vedic mathematics into 16 simple sutras (formulae). These Sutras deal with Arithmetic, Algebra, Geometry, Trigonometry, Analytical Geometry etc. The simplicity in the Vedic mathematics sutras paves way for its application in several prominent domains of engineering like Signal Processing, Control Engineering and VLSI.

2. ABOUT "NIKHILAM SUTRA "

Nikhilam sutra means "all from 9 and last from 10". Mathematical description of this sutra can be fonnulated as:

Assuming A and B are two n-bit numbers to be multiplied and their product is equals to P.

$$A = \sum_{i=0}^{n-1} A_i 10^i \quad \text{Where } A_i \in \{0,1..9\} \qquad (1)$$

$$B = \sum_{i=0}^{n-1} B_i 10^i \quad \text{Where } B_i \in \{0,1..9\} \qquad (2)$$

Multiplication Rule:

$$P=AB \qquad (3)$$

$$P = AB + 10^{2n} + 10^n(A + B) - 10^{2n} - 10^n(A + B) \qquad (4)$$

$$P = \{10^n(A + B) - 10^{2n}\} + 10^{2n} - 10^n(A + B) + AB \qquad (5)$$

Equation no 5 can be derived for both the numbers if the number is greater than the base or less than the base.

If the number is greater than the base:

$$P = \{10^n(A + B) - 10^n\} + (10^n - A)(10^n - B) \qquad (6)$$

If the number is less than the base:

$$P = \{10^n(A + B) - 10^n\} + (A - 10^n)(B - 10^n) \qquad (7)$$

$$P = \{10^n\{A - (10^n - B)\} + (10^n - A)(10^n - B) \qquad (8)$$

$$P = 10^n(A - \bar{B}) + \bar{A}\,\bar{B} \qquad (9)$$

Where $\bar{A}$ and $\bar{B}$ are the 10^n compliments of A and B.

$$\bar{A} = 10^n - \sum_{i=0}^{n-1} A_i 10^i \qquad (10)$$

$$\bar{A} = \sum_{i=1}^{n-1} (9 - A_i)10^i + (10 - A_0) \qquad (11)$$

The serious drawback of Nikhilam sutra can be summarized as:

(i) Both the multiplier and multiplicand are less or greater than the base.

(ii) Multiplier and multiplicand are nearer to the base.

3. PROPOSED MULT1PLIER ARCHITECTURE DESIGN

The mathematical expression for the proposed algorithm is shown below. Broadly this algorithm is divided into three parts. (i) Radix Selection Unit (ii) Exponent Determinant (iii) Multiplier.

Consider two n bit numbers X and Y. kl and k2 are the exponent of X and Y respectively(The assumption which the paper can taken is the imaginary term is zero). X and Y can be represented as:

$$X = Zk1 \pm Zl \qquad (12)$$

$$y = Zk2 \pm Z2 \qquad (13)$$

For the fast multiplication using Nikhilam sutra the bases of the multiplicand and the multiplier would be same, (here we have considered different base) thus the equation (13) can be rewritten as

$$Y * 2^{k_1-k_2} = 2^{k_1} \pm z_2 2^{k_1-k_2} \quad (14)$$

$$X * Y * 2^{k_1-k_2} = (2^{k_1} \pm Z_1)(2^{k_1} \pm z_2 2^{k_1-k_2}) \quad (15)$$

$$= 2^{2k_1} \pm Z_1 2^{k_1} \pm z_2 2^{k_1-k_2} \pm z_1 z_2 2^{k_1-k_2} \quad (16)$$

$$= 2^{k_1}(2^{k_1} \pm Z_1 \pm z_2 2^{k_1-k_2}) \pm z_1 x_2 2^{k_1-k_2} \quad (17)$$

$$= 2^{k_1}(X \pm z_2 2^{k_1-k_2}) \pm z_1 z_2 2^{k_1-k_2} \quad (18)$$

$$P = XY = 2^{k_2}(X \pm z_2 2^{k_1-k_2}) \pm z_1 z_2 \quad (19)$$

Hardware implementation of this mathematics is shown in Fig. 1. The architecture can be decomposed into three main subsections: (i) Radix Selection Unit (RSU) (ii) Exponent Determinant (ED) and (iii) Array Multiplier. The Radix Selection Unit is required to select the proper radices corresponding to the input numbers. If the selected radix is nearer to the given number then the multiplication of the residual parts (Zl xz2) can be easier to compute. The Subtractor blocks are required to extract the residual parts (Zl and Z2). The second subsection (ED) is used to extract the power (kl and k2) of the radix and it is followed by a subtractor to calculate the value of (k1-k2).The third subsection array multiplier [10] is used to calculate the product (Zl xZZ). The output of the subtractor (klk2) and Zz are fed to the shifter block to calculate the value of Z2 x Zk1-k2.The first adder-subtractor block has been used to calculate the value of X ± Z2 x Zk1 -k2• The output of the first adder-subtractor and the output of the second Exponent Determinant (k2) are fed to the second shifter block to compute the value of Zk2 x (X ± Z2 X Zk1-k2). The output of the multiplier (Zl xz2) and the output of the second shifter (Zk2 x (X ± Z2 x Zk1-k2))are fed to the second addeRadix Selection Unitbtractor block to compute the value of (Zk2 x (X ± Z2 x Zk1-k2)) ± ZlZ2'A. Mathematical expression/or RADIX SELECTION UNIT. Consider an 'n' bit binary number X, and it can be represented as X = Where Then the values of X must lie in the range . Consider the mean of the range is equals to A.

$$A = \frac{2^{n-1} + 2^n}{2} \quad (20)$$

$$A = 2^{n-2} * 3$$

If X>A then radix = 2^n

If X>A then radix = 2^{n-1}

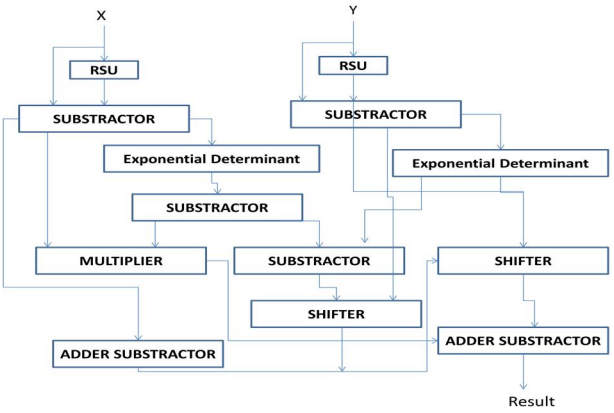

Figure 1 Hardware implementation of "Nikhilam Sutra "

The Block level architecture of RADIX SELECTION UNIT is shown in Fig. 2. Radix Selection Unit consists of three main subsections: (i) Exponent Determinant (ED), (ii) Mean Determinant (MD) and (iii) Comparator. 'n' number bit from input X is fed to the ED block. The maximum power of X is extracted at the output which is again fed to shifter and the adder block. The second input to the shifter is the (n+ 1) bit representation of decimal '1 '.If the maximum power of X from the ED unit is (n-1) then the output of the shifter is The adder unit is needed to increment the value of the maximum power of X by '1'. The second shifter is needed to generate the value of here n is the incremented value taken from the adder block. The Mean Determinant unit is required to compute the mean of The Comparator compares the actual input with the mean value of If the input is greater than the mean then is selected as the required radix. If the input is less than the mean then -1 is selected as the radix. The select input to the multiplexer block is taken from the output of the comparator[8][9].

Exponent Determinant

The hardware implementation of the exponent determinant is shown in Fig. 3.The integer part or exponent of the number from the binary fixed point number can be obtained by the maximum power of the radix. For the nonzero input, shifting operation is executed using parallel in parallel out (PIPO) shift registers. The number of select lines (in Fig A it is denoted as S], So) of the PIPO shifter is chosen as per the binary representation of the number . 'Shift' pin is assigned in PIPO shifter to check whether the number is to be shifted or not (to initialize the operation 'Shift' pin is initialized to low). A decrementer has been integrated in this architecture to follow the maximum power of the radix. A sequential searching procedure has been implemented here to search the first 'I' starting from the MSB side by using shifting technique. For an N bit number, the value is fed to the input of decrementer [8][9].

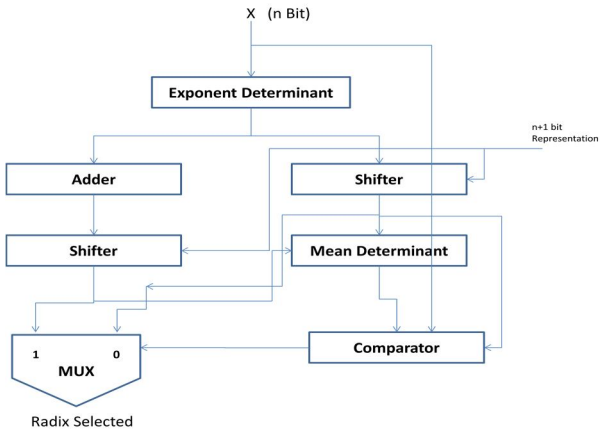

Figure 2 Hardware implementation of RADIX SELECTION UNIT

The decremented is decremented based on a control signal which is generated by the searched result. If the searched bit is '0' then the control signal

becomes low then decrementer start decrementing the input value (Here the decrementer is operating in active low logic). The searched bit is used as a controller of the decrementer. When the searched bit is 'I' then the control signal becomes high and the decrementer stops further decrementing and shifter also stops shifting operation. The output of the decrementer shows the integer part (exponent) of the number[8][9].

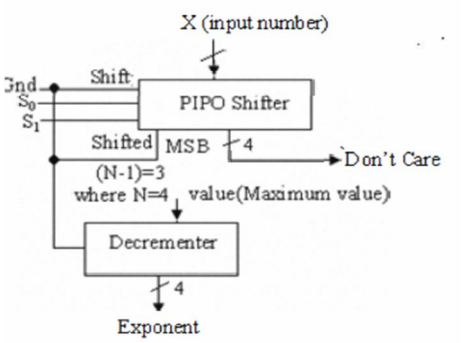

Figure 3 Hardware implementation of exponent determinant

4. Results

In this paper the VEDIC multiplier using Nikhilam Sutra is implemented using VERILOG HDL. From the simulated waveforms the functionality is verified and confirms the operation of the design. With a little bit of trade off in terms of speed the power consumption is reduced drastically. In this paper the Xilinx xpower Tool is used for power analysis and Xilinx ISE is used for simulation and synthesis. The Simulation result and the RTL Schematic of the proposed Multiplier is shown if Fig 4 & 5. The device utilization summary is listed in Table.1.

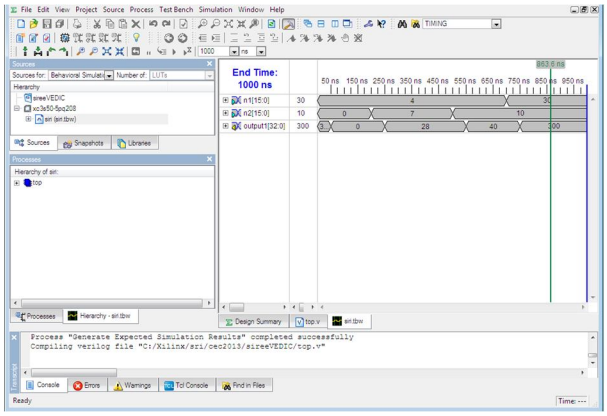

Figure 4 Simulation Result for Vedic Multiplier

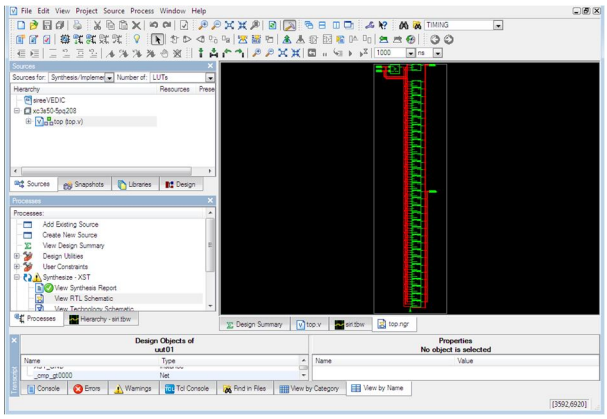

Figure 5 RTL Schematic for Vedic Multiplier

Total 84.578ns (30.042ns logic, 54.536ns route) (35.5% logic, 64.5% route)

Total memory usage - 261972 kilobytes

Table-1
Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slices	605	768	78%
Number of 4 input LUTs	1106	1536	72%
Number of bonded IOBs	65	124	52%
Number of MULT18X18s	1	4	25%
Total estimated power consumption			2

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