Design and Simulation of Low Power Reduced Read & Write Stability in SRAM Memory

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Abstract: Low Power design and portable is major concern in this present World of VLSI Technology. Due to the rapid scaling procedure exiting losses their properties. In this paper we shows the operation of a Conventional SRAM and drawbacks of existing one to overcome the drawbacks we show a proposed 8T SRAM design and a Schmitt trigger SRAM technology design and their comparison of power consumption are shown using the Tanner Tool simulation

Keywords: VLSI, SRAM Schmitt Trigger

I INTRODUCTION

The IRTS roadmap predicts that the 90% of SoC is covered with memory by the year 2K13. Because of the high speed, low power consumption, robustness and ability of integrating with digital logic blocks, so the bigger the size of SRAM larger is the power consumed. We many reasons for using SRAM in system design. Speed, cost, density and features are the main design tradeoffs for selecting SRAM for your design. When speed is considered SRAM has an edge over DRAM.

Due to this many attempts were being made to decrease the power consumption in SRAM which will increase the battery lifetime of the devices which were operated using battery such as PDA’s, wireless, cellular phone and low power biomedical devices. For this scaling of supply voltage is an effective method. But due to this the gate delay is increased which reduces the frequency of operations. Increase in the frequency of operation also increases the power dissipation of circuit due to increment of dynamic power dissipation.

CMOS digital circuits occur in two forms: dynamic and static. Dynamic power dissipation occurs in the 1 logic gates that are in the process of switching from one state to another. During this process, any internal and external capacitance associated with the gate's transistors has to be charged, thereby consuming power. Static power dissipation is associated with inactive logic gates (i.e., not currently switching from one state to another). Dynamic power is important during normal operation, especially at high operating frequencies, whereas static power is more important during standby, especially for battery-powered devices. For dynamic loss reduction here we shows proposed design which reduces the dynamic power by using additional voltage source and we show Schmitt trigger SRAM based operation for reduce power dissipation as well as improved read capabilities shows in later section

II EXISTING WORKS

1. Conventional 6T SRAM design:

There are many topologies for SRAM in past decades 6T SRAM got its attention for the tolerance capability for noise over another SRAM cell design. The 6T SRAM cell design consists of two access transistors and two cross coupled CMOS inverters. Bit lines are the input/output ports of the cell with high capacitive loading. The operations READ and WRITE are conducted by these bit lines only; we will see how these are carried out.

a) Read Operation: Before starting of the read operation, we should charge the bit lines to VDD. When the word line (WL) is enabled, the bit line which connected to the node of the cell containing ‘0’ is discharged through the NMOS transistor. By this we can know which node is containing ‘0’ and which is having ‘1’ in it. Using sense amplifiers we can know the node containing 1/0 by sensing the bit lines. The bit line containing ‘1’ means it's connected to the node containing ‘1’ and vice versa.

b) Write Operation: For writing 1/0 we should provide the data to the bit line (BL), with respect to the bit line bar (BL). When the word line (WL) is enabled the data is written into respective node.

Figure: 1 Conventional 6T SRAM

But the conventional 6T SRAM have stability limitations at low supply voltages. Hence we go for 8T SRAM design. It
has the advantage of low power at read ‘1’ operation. As it does not consume power at read ‘1’ cycle.

2. Proposed SRAM Design:
To overcome the drawback that associated with conventional 6T SRAM in this paper we show a new modified designs 6T SRAM. The proposed SRAM design shows a almost constant power dissipation when frequency increases. In proposed SRAM we add a additional two voltages nodes across the internodes of SRAM to reduce the voltage swing so as the power dissipation of the circuit will be reduced.

![Figure: 2 Proposed 8T SRAM Design](image)

The additional Voltage sources which are connected to the output node of SRAM were controlled by the bit line depended transistors which reduces the voltage swing in the output node, so the dynamic losses are reduced. Because dynamic losses are depend upon the equation

\[ P_{\text{dynamic}} = \alpha C V_{dd} V_{\text{Swing}} f \]

So the dynamic losses are directly proportional to the operating frequency and also the \( V_{\text{Swing}} \) i.e. voltage swing that was occurred in the SRAM network.
As Voltage Swing reduces the dynamic loss also reduces which makes the constant dynamic loss with increase in operating frequency.

3. Need of Schmitt Trigger Based SRAM Designs:
In order to resolve the conflicting read versus write design requirements in the conventional 6T bit cell, we apply the Schmitt Trigger (ST) principle for the cross-coupled inverter pair. A Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition. In the proposed ST SRAM bit cells, the feedback mechanism is used only in the pull-down path, as shown in figure.

During input transition, the feedback transistor (NF) tries to preserve the logic “1” at output ( ) node by raising the source voltage of pull-down Nmos (N1). This results in higher switching threshold of the inverter with very sharp transfer characteristics. Since a read-failure is initiated by a input transition for the inverter storing logic “1,” higher switching threshold with sharp transfer characteristics of the Schmitt trigger gives robust read operation.

![Figure: 3 Inverter with Schmitt Trigger Connection](image)

For the input transition, the feedback mechanism is not present. This results in smooth transfer characteristics that are essential for easy write operation. Thus, input-dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write-ability of the SRAM bit cell.

![Figure: 4 Schmitt Trigger SRAM](image)

4. Simulation and Results:
These circuits are designed and simulated using S-Edit, T-spice and W-edit of tanner tools 13.0

![Figure: 5 Conventional 6T SRAM Cell](image)
IV. References:


Table: 1 comparison of 6t, 8t and Schmitt trigger

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional 6T SRAM</td>
<td>6.322254e-007 watts</td>
</tr>
<tr>
<td>Proposed 8T SRAM</td>
<td>3.569343e-007 watts</td>
</tr>
<tr>
<td>Schmitt Trigger SRAM</td>
<td>2.719961e-007 watts</td>
</tr>
</tbody>
</table>

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III. Conclusion:

The Proposed 8T SRAM makes an effective way of reduction of dynamic losses in the Conventional 6T SRAM design by reducing the voltage swing in the network. The proposed Schmitt Trigger SRAM shows effective characteristics than 8T SRAM by using Schmitt connection in inter network that used for designing the SRAM.