Programmable High Speed 8-Bit Binary Incrementer Decrementer

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Abstract:
This paper presents the eight bit CMOS base incrementer and decrementer logic design using eight bit adder and subtractor. The parametric simulation is done on MICROWIND layout editor tool. The any conventional static CMOS adder with pullup and pulldown logic requires 32 MOSFET whereas our design adder requires 30 MOSFETs. Our design methodology is based on static CMOS logic and transmission gate logic to achieve smaller delays, reduce power dissipation and optimized area. We can use a high-speed parallel adder in incrementer / decrementer to improve the operating speed which can count up or count down from the loaded value by one step in one clock cycle.

Keywords: Incrementer/ decrementer,

Introduction:
The VLSI base microprocessor and digital signal processor system requires addition as a fundamental arithmetic operation. The incrementer decrementer circuit is commonly use in frequency dividers and address generation in processors. The higher speed adder requires large area however high-speed parallel adder should be utilized in the adder-based incrementer / decrementer to improve the operating speed which can count up or count down by one step in one clock cycle. For this incrementer decrementer logic uses adder circuit. Among the various adders the carry propagat adder is mostly use but it have the speed limitation due to its propagation from less significant stages to higher significant stages. Some techniques based on carry generation method, such as Carry Select, Carry Skip and Carry Look ahead techniques have been introduced to improve the speed of Ripple Carry Adder. But these types of adder require large area.

Related Work:
Nikhil Kaswan, Ishan Munje, Yash Kothari design 4-bit incrementer/decrementer can operate up to 5GHz with 200x160 um2 optimized area. They design the multiplexer base full adder logic for their propose circuit [1]. The power consumption is optimize with minimum size for both NMOS and PMOS. The W/L's of all transistors in the subsystems were kept in the ratio of 2:1 for the pull up and pull down network respectively[1]. The design the computational unit base on arithmatic adder which are identical for all adder units, so called Metamorphosis of Partial Full Adder (MPFA) and look ahead circuit. Enhanced Multiple-Output Domino Logic by Zhongde Wang, Graham A. Jullien, William C. Miller, Jinghong Wang, and Sami S. Bizzan, the researchers showed that Using an enhanced multiple output domino logic (EMODL) implementation of a carry look ahead adder (CLA), sums of several consecutive bits can be built in one nFET tree with a single carry-in. Based on this result, a new sparse carry chain architecture is proposed for the CLA adder [3].

Methodology:
The major drawback of the parallel adder is its slow speed due to the time it takes to propagate the carry. Thus to overcome this drawback we propose a transmission gate base adder cell. In our work the use of transmission gate reduces the number of transistors which overcomes the area trade offs. The major limitation of the parallel adder is that the delay increases linearly with the bit length. The circuit consists of a t-gate based multiplexer and a non-inverting buffer (built as a cascade of two inverters). One additional inverter is used to generate the inverse of the clock input signal, required to control the transmission-gates. If both the clock signal and the inverted clock signal are available from external circuitry, this inverter can be removed. The major limitation of the parallel adder is that the delay raises linearly with the bit length. Each full adder has to wait for the carry out of the previous stage to output steady-state result. The result is a reduced carry propagation time. The basic building blocks in this adder is the PG generator, carry generator and sum gernerator.

Single-Bit Full Adder Cell:
The full adder logic cell is design by using two transmission gate base half adder circuit. The behaviour of half adder include the logical XOR and logical AND operation. The property of XOR logic is, when its any one input is binary '0' the output will follow the second input otherwise output
follows the complement of its second input. By using this property we can design the half adder sum logic in multiplexer like architecture. Similar the property of AND logic gate is when its any one input is binary '0' the output will be '0' regardless the value of second input otherwise output follows the second input. By using this property we can design the half adder sum logic in multiplexer like architecture. The Sum of A=1 and B=1 cannot be expressed by a single bit, and a result with a higher significance than the Sum is required. This result is known as the Carry-out, which states that an overflow has occurred. The 1-bit FA is an improved half adder circuit having an additional Carry in signal, which allows it to be cascaded with other adders and, hence, is commonly used as a basic building block for generic adder arrays. Since the Full adder is the mainly used structure in a broad range of computational complexities, a significant amount of research effort was made on the realization of efficient adder structures. Note that the truth table of the half adder corresponds to the first four entries in the truth table where Carry-in=0. The architecture designs of our adder logic consist of transmission gate (TG) base multiplexer logic.

Timing Simulation:
Timing simulation of our design is done on MICRWIND layout editor tool. All the possible input patterns are applied on the design and its output responses are analyze. For simulation all eight possible combinations of values of input signals for a FA cell, i.e., 000, 001, 010,.., 111 are use. By using three bit inputs of full adder cell it is possible to use total sixty four transissions of all possible eight combination of inputs are applied on simulator. In the process of time delay measuring the previous values of the input signals should be considered together with the current signal values. This is due to the fact that there exist cases when the values of input signals remain unchanged implying that the outputs remain unchanged as well, and, therefore, no time delay should be measured.

Implementation:
The recent developments in VLSI technology use arithmetic operations which includes addition, subtraction and multiplication operation. The 1-bit full adder is the building block of these operation modules. By using the merits and demerits of parallel adder and carry look ahead adder the purpose of this paper is to propose a new structure to achieve higher operation speed in a much smaller on-chip area with optimize power dissipation. Our one bit full adder is design on 50nm technology using transmission gate. The variation between the pass transistor logic and the complementary CMOS logic design is that the source end of the pass transistor logic is connected to some input signals instead of the power supply.

Results:

![Image](https://via.placeholder.com/150)

Fig 1 Schematic design for CMOS and TG base multiplexer logic

![Image](https://via.placeholder.com/150)

Fig 1 Schematic circuit for Incrementer Decrmeneter logic

The incremenent deccmeneter logic circuit includes transmission gate base fuladders, xor,logic gates and flipflop base counter logic shown in fig 1. Xor logic gate is a odd parity generator which have propey that when any of its input is '0' then the second input will transfer towards output , in other hand if one of its input is '1' then 1’s compliment of second input is transfer towards the output. This property is use to generates the 2:s complement to get negative equivalent of the second number while using deccmenet logic. The count value from which the circuit count up or count down is loaded from XOR logic to the adder circuit.
Fig 2 Layout design for 8 bit addsubtract logic

The layout of Incrementer Decrementer circuit is shown in fig 2. This layout is design on MICROWIND layout simulator. It design with 280 NMOS and 272 PMOS transistors.

Fig 3 Timing simulation of addition operation when addsub signal is at ‘0’.

Fig 4 Timing simulation of subtraction operation when addsub signal is at ‘1’.

Conclusion:
The above circuits is simulated in micro wind 3.1 using 90nm CMOS technology The delay measured in the range of 2ns and power consumed in the range of 7.0 to 9.0 microwatt. A transmission gate base design is an analog switch controlled by logic signals. It uses 280 NMOS and 272 PMOS type transistor. We design the basic building blocks of adder subtractor by using transmission gate. Transmission Gate has is a high-quality switch with low resistance and capacitance.

Sizing is also not necessary in general, as the resistance and capacitance decrease and increase respectively as the gate W=L ratio is increased. TG is commonly used to implement designs with the minimum number of transistors.

Reference: