Design of Energy Efficient Arithmetic Circuits Using Charge Recovery Adiabatic Logic

B. Dilli Kumar[1,] M. Bharathi[2]

[1]*M. Tech (VLSI), Department of ECE, Sree Vidyanikethan Engineering College, Tirupati, India*[,]

[2]*Assistant Professor, Department of ECE, Sree Vidyanikethan Engineering College, Tirupati, India,*

Abstract- **Low power has emerged as a principle theme in today electronic industry. Energy efficiency is one of the most important features of modern electronic systems designed for high speed and portable applications. The power consumption of the electronic devices can be reduced by adopting different design styles. Adiabatic logic style is said to be an attractive solution for such low power electronic applications. This paper presents an energy efficient technique for digital circuits that uses adiabatic logic. The proposed technique has less power dissipation when compared to the conventional CMOS design style. This paper evaluates the full adder in different adiabatic logic styles and their results were compared with the conventional CMOS design. The simulation results indicate that the proposed technique is advantageous in many of the low power digital applications.**

Keywords: **Adiabatic, Charge recovery, low power, energy efficient, digital circuits, sinusoidal power clock.**

I.   INTRODUCTION

Power consumption plays an important role in the present day VLSI technology. As many of the present day electronic devices are portable, they need more battery backup which can be achieved only with the low power consumption circuits that are internally designed in them. So energy efficiency has become main concern in the portable equipments to get better performance with less power dissipation. As the power dissipation in a device increases then extra circuitry is necessary to cool the device and to protect the device from thermal breakdown which also results in increase of total area of the device. In order to overcome these problems the power dissipation of the circuit is to be reduced by adopting different low power techniques. The less the power dissipation, the more efficient the circuit will be.

From the past few decades CMOS technology plays a dominant role in designing low power consuming devices. Compared to different logic families CMOS has less power dissipation which made it superior over the previous low power techniques. The power consumption in conventional CMOS circuit is due to switching activity of the devices from one state to another state and due to the charging and discharging of load capacitor at the output node.

The power dissipation in conventional CMOS design can be minimized by reducing the supply voltage, node capacitance value and switching activity. But reducing the values of these parameters may degrade the performance of the device. So an efficient low power technique other than CMOS is needed that has less power dissipation compared to CMOS which can be done by using adiabatic technique.

The present paper focuses on a novel energy efficient technique called adiabatic logic which is based on energy recovery principle. In this technique instead of discharging the consumed energy is recycled back to the power supply thereby reducing overall power consumption. In the present paper the performance of full adder is evaluated in different adiabatic logic styles and their results were compared with the conventional CMOS design. As full adder is one of the basic building blocks of many of the digital circuits, the present paper mainly concern on its design. The performance of this device was evaluated in different adiabatic techniques of ECRL, PFAL, 2PASCL, and PFAL&2PASCL. Simulation results shows that the proposed technique is efficient over the conventional CMOS design in terms of power dissipation.

II.   CMOS DESIGN

CMOS is the basic building block of many of the digital circuits. The CMOS circuit itself acts as an inverter. It can be realized as a combination of PMOS in the pull up section whose source is connected to power supply and NMOS in the pull down section whose source is connected to ground and the output is taken across the drain junction of the two devices. The CMOS circuit has less power dissipation when compared to many of the previous VLSI families of RTL, TTL and ECL. The power consumption in CMOS is due to the switching activity of the transistors from one state to another state, charging and discharging of the load capacitance and frequency of operation.

(i)   INVERTER

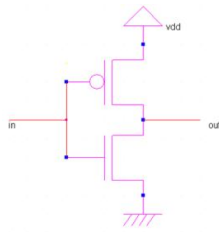The basic CMOS inverter circuit is shown in figure 1

Fig. 1: CMOS inverter

The operation of the circuit can be evaluated in two stages of charging phase and discharging phase. During the charging phase, the input to the circuit is logic LOW. During this phase, the PMOS transistor conducts and NMOS transistor goes in to OFF state which charges the output value to power supply results in logic HIGH output. The equivalent circuit consists of a resistor in series with the output load capacitance which shows a charging path from power supply to output terminal. Here the resistor acts ac PMOS ON resistor.
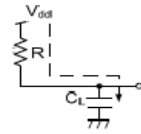
Fig. 2: Equivalent circuit for charging process in CMOS

During the discharging phase, the input to the circuit is logic HIGH. During this phase, the NMOS transistor conducts and PMOS transistor goes into OFF state which results in a discharging path from output terminal to ground. The value that is stored at the output during the charging phase discharges towards the ground results in logic LOW output. The equivalent circuit consists of a resistor in series with output terminal to ground. Here the resistor acts as NMOS ON resistor.
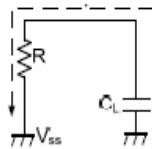

Fig. 3: Equivalent circuit for discharging process in CMOS

From the operation of the CMOS design it is evident that during the charging process, the output load capacitor is charged to $Q = CLVdd$ and the energy stored at the output is $(½)CLVdd^2$. During the discharging phase, the amount of energy dissipated is also $(½)CLVdd^2$. So the total amount of energy dissipated during the charging and discharging phases is

$$E_{dissipated} = CLVdd^2 \qquad (1)$$

(ii) FULL ADDER

A basic full adder has three inputs and two outputs which are sum and carry. The logic circuit of this full adder can be implemented with the help of XOR gate, AND gates and OR gates. The logic for sum requires XOR gate while the logic for carry requires AND and OR gates. The full adder design in static CMOS using complementary pull up pMOS network and pull down nMOS network is the most conventional one. The basic circuit for CMOS full adder is
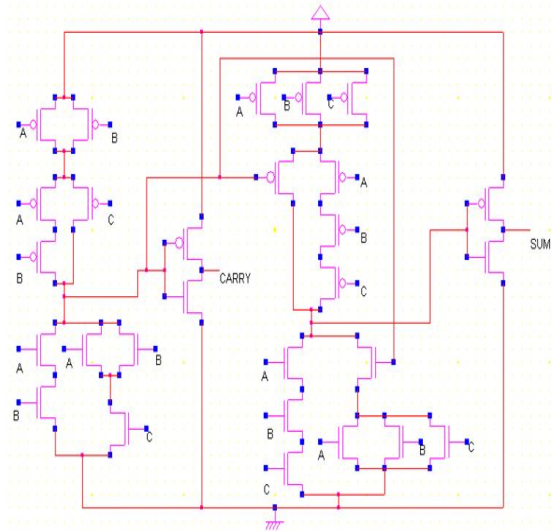

Fig. 4: CMOS full adder

Fig.4 shows the circuit for full adder in conventional CMOS design. It requires 28 transistors.

The power consumption of the CMOS circuit is based on the following equation

$$P = CV^2f \qquad (2)$$

From the equation it is evident that the power dissipation of CMOS can be reduced by minimizing the supply voltage, node capacitance and switching activity to some extent. But reducing the values of these parameters may suffer from some disadvantages. Reducing the load capacitance is strongly limited by the technology. Reducing the supply voltage may degrade the performance of the device. Reducing the supply voltage may also suffer from leakage problems.

In order to overcome these problems an efficient low power technique called adiabatic logic is explained in this paper.

III.   ADIABATIC LOGIC

The word ADIABATIC is derived from the Greek word "adiabatos", which means there is no exchange of energy with the environment and hence no energy loss in the form of heat dissipation. Adiabatic logic is commonly used to reduce the energy loss during the charging and discharging process of circuit operation. Adiabatic logic is also known as "energy recovery" or "charge recovery" logic. As the name itself indicates that instead of dissipating the stored energy during charging process at the output node towards ground it recycles the energy back to the power supply thereby reducing the overall power dissipation and hence the power consumption also decreases. The adiabatic logic uses AC power supply instead of constant DC supply, this is one of the main reasons in the reduction of power dissipation.

The adiabatic logic can be explained with the help of basic inverter circuit
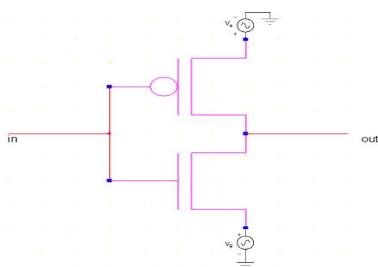
Fig. 5: Adiabatic inverter

The adiabatic inverter circuit can be constructed using CMOS inverter with two AC power supplies instead of DC supply. The power supply's are arranged in such a way that one of the clock is in phase while the other is out of phase with the first one. The operation of the adiabatic inverter can be explained in two stages. During the charging phase, the PMOS transistor conducts and NMOS transistor goes into OFF state which charges the output load capacitor towards the power supply results in logic HIGH output.
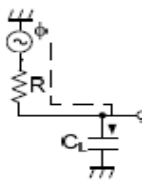
Fig. 6: Equivalent circuit for charging process in adiabatic inverter

During discharging phase, the NMOS transistor conducts and PMOS transistor goes into OFF state. Instead of discharging the stored value at the output towards ground, the energy is recycled back to the power supply. Its equivalent circuit consists of a resistor in series with output load capacitance and power supply.
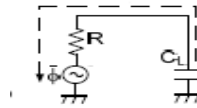
Fig. 7: Equivalent circuit for charge recovery process in adiabatic inverter

The charging process and the charge recovery process are efficient only when the charging voltage is varying one. Lower the rate of charging, lesser the power drawn from the supply voltage.

IV. ADIABATIC TECHNIQUES

Adiabatic logic has a different logic style which helps in the reduction of the power dissipation of the circuit. The present paper explains basic full adder using some of the important adiabatic techniques.

(i)   ECRL

Efficient charge recovery logic consists of two cross couple PMOS transistors in the pull up section where as the pull down section is constructed with a tree of NMOS transistors. Its structure is similar to Cascode Voltage Switch Logic (CVSL) with differential signaling. The logic function in the functional block can be realized with only NMOS transistors in the pull down section. The basic inverter and full adder in ECRL logic can be constructed as
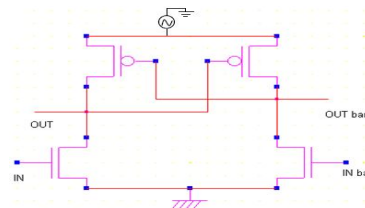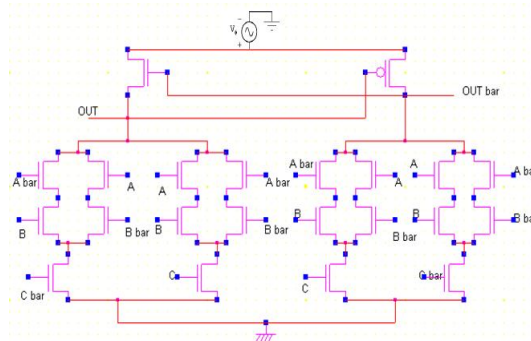
Fig. 8: ECRL inverter
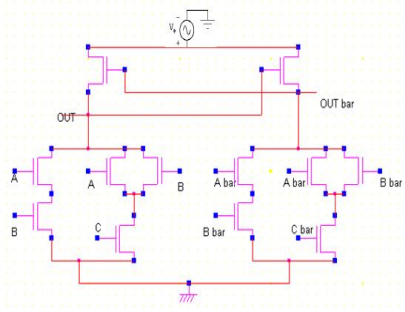
Fig. 9: ECRL sum circuit

Fig. 10: ECRL carry circuit

(iii)   PFAL

The Positive Feedback Adiabatic Logic is a partial energy recovery circuit. It is also known as PAL-2N (Pass transistor Adiabatic Logic). The core of PFAL logic is a latch made up of two PMOS and two NMOS transistors that avoid logic level degradation on the output nodes. The logic function in the functional block can be realized with only NMOS transistors connected parallel to the PMOS transistors. The primary advantage of PFAL over ECRL is that the functional blocks are in parallel with the PMOSFETs forming transmission gate. It also has the advantage of implementing both the true function and its complimentary function.

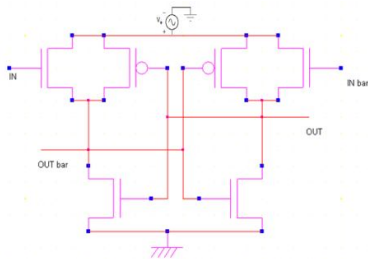Using PFAL, the basic inverter and full adder can be constructed as
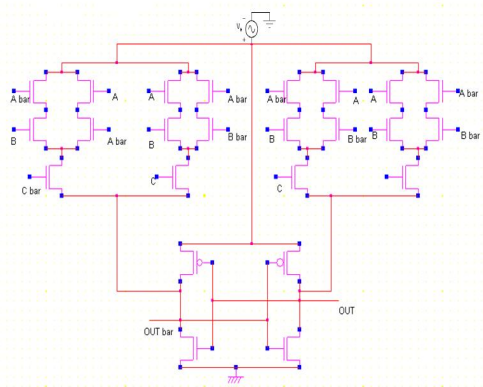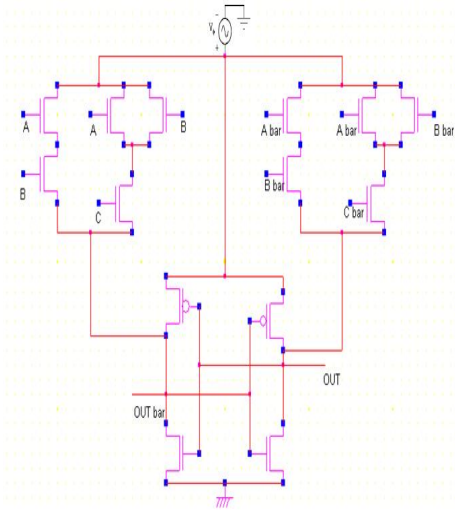

Fig. 11: PFAL inverter

Fig. 12: PFAL sum

Fig. 13: PFAL carry

(iv)   2PASCL

The Two Phase Adiabatic Static Clocked Logic (2PASCL) uses two phase clocking split level sinusoidal power supply's which has symmetrical and unsymmetrical power clocks where one clock is in phase while the other is out of phase. The circuit has two diodes in its construction where one diode is placed between the output node and power clock, and another diode connected between one of the terminals of NMOS and power source. Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. The circuit operation is divided into two phases "hold phase" and "evaluation phase". During the evaluation phase, the power clock swings up and power source swings down. During the hold phase, the power source swings up and power clock swings down.

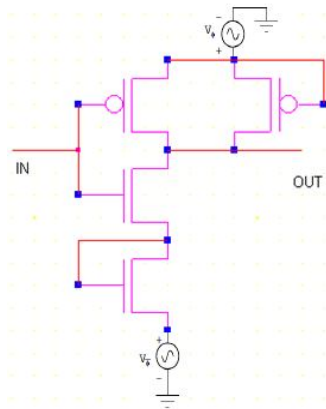Using 2PASCL the basic inverter and full adder can be constructed as

Fig. 14: 2PASCL inverter

and PFAL and it also gives the true function and complementary function of a given circuit.

Using PFAL&2PASCL, the basic inverter and full adder can be constructed as
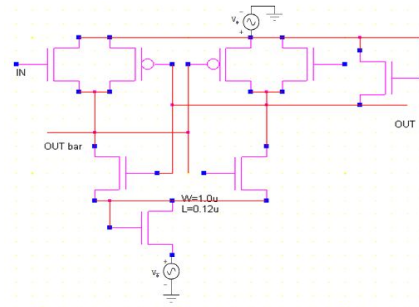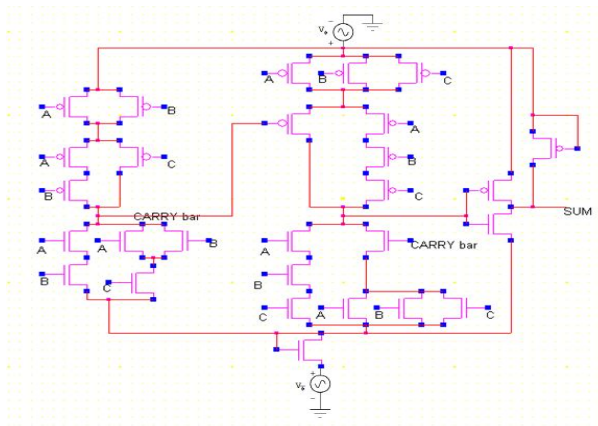

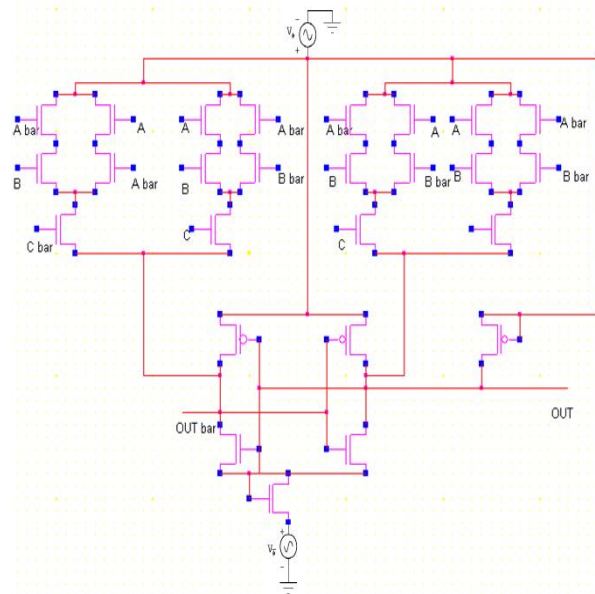Fig. 17: PFAL&2PASCL inverter

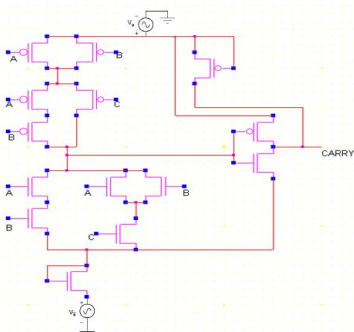Fig. 15: 2PASCL sum

Fig. 18: PFAL & 2PASCL sum

Fig. 16: 2PASCL carry

(v)   PFAL& 2PASCL

The PFAl&2PASCL logic can be realized as a combination of both PFAL and 2PASCL. Its structure is similar to 2PASCL except the core part of 2PASCL is replaced by PFAL logic circuit. It has two power clock signals operated in two different modes. The major advantage of this technique is it has less power dissipation compared to ECRL
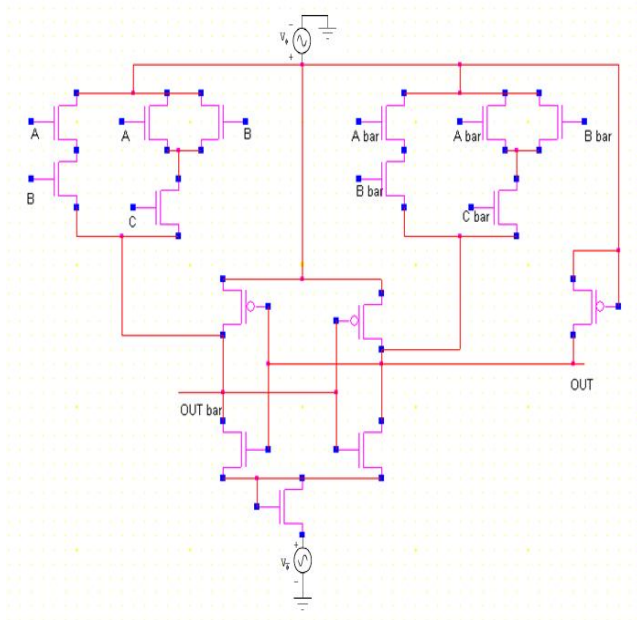
Fig. 19: PFAL & 2PASCL carry

V.   SIMULATION RESULTS AND DISCUSSION

The simulation results were verified using PSPICE software at 50 KHz and 50 MHz frequency. The simulation results of full adder in conventional CMOS design and different adiabatic logic design styles were presented in this section
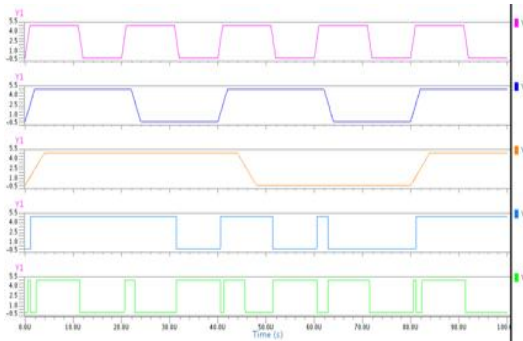

Fig. 20: Simulated waveforms CMOS full adder

Fig. 20 shows the simulated waveforms of full adder, where the top three signals indicate inputs while the bottom two signals are carry and sum respectively.
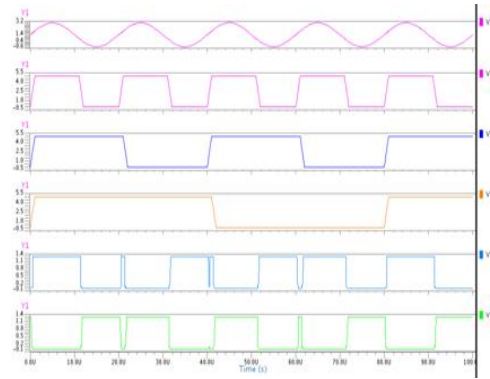

Fig. 21: Simulated waveforms of ECRL sum

Fig. 21 shows the simulated waveforms of ECRL sum, where the uppermost signal indicate sinusoidal power clock, the three signals below it are input signals and the bottom two signals are output and its complimentary signals.
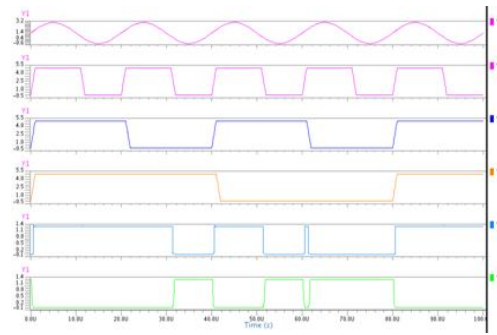

Fig. 22: Simulated waveforms of ECRL carry

Fig. 22 shows the simulated waveform of ECRL carry, where the top signal indicates the sinusoidal power clock, the three signals below it are inputs while the bottom two signals are output and its complimentary signals respectively.
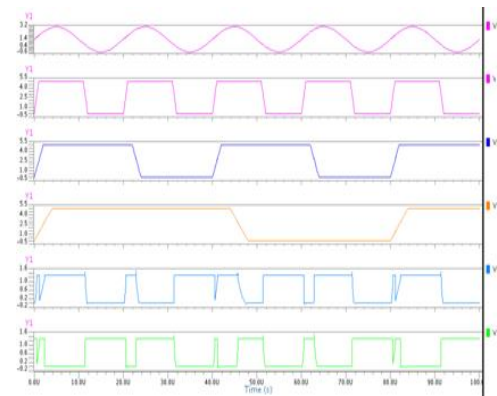

Fig. 23: Simulated waveforms of PFAL sum

Fig. 23 shows the simulated waveform of PFAL sum, where the uppermost signal indicates sinusoidal power clock, the three signals below it indicate inputs and the lower two signals are output signal and its complimentary signal respectively.
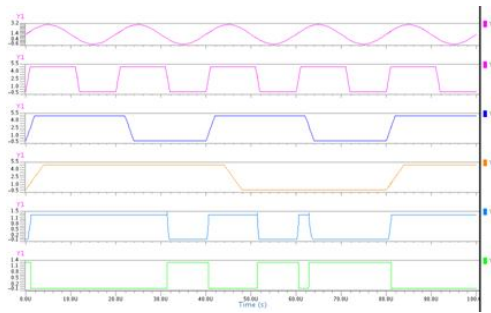

Fig. 24: Simulated waveforms of PFAL carry

Fig. 24 shows the simulated waveform of PFAL carry, where the uppermost signal indicates sinusoidal power clock, the three signals below it indicate inputs and the lower two signals are output signal and its complimentary signal respectively.
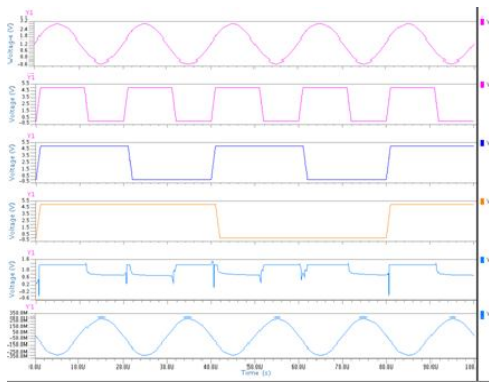

Fig. 25: Simulated waveforms of 2PASCL sum

Fig. 25 shows the simulated waveform of 2PASCL sum, where the top and bottom signals indicate sinusoidal power clocks, the signal between power clocks are three inputs and output signals respectively.
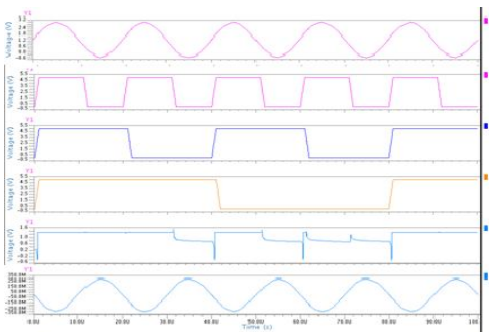

Fig. 26: Simulated waveforms of 2PASCL carry

Fig. 26 shows the simulated waveforms of Modified 2PASCL carry, where the top and bottom signals indicate sinusoidal power clock signals and the signals between power clocks are three inputs and output signals respectively.
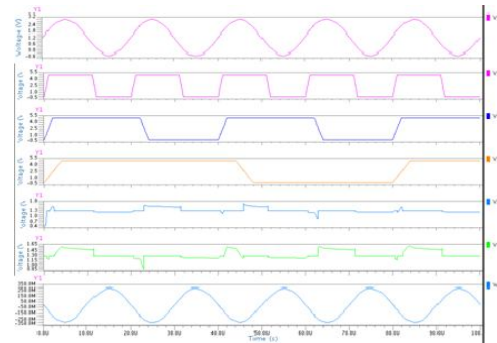
Fig. 27: Simulated waveforms of PFAL&2PASCL sum

Fig. 27 shows the simulated waveforms of PFAL&2PASCL sum, where the top and bottom signals indicate sinusoidal power clocks and the signals between power clocks are three inputs, output and complimentary output signals respectively. Where the flat amplitude refers to logic HIGH and varying amplitude refers to logic LOW.

Fig. 28: Simulated waveforms of PFAL & 2PASCL carry

Fig. 28 shows the simulated waveforms of PFAL&2PASCL carry, where the top and bottom signals indicate sinusoidal power clocks and the signals between power clocks are three inputs, output and complimentary output signals respectively. Where the flat amplitude refers to logic HIGH and varying amplitude refers to logic LOW.
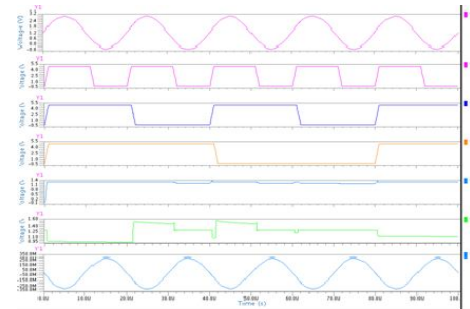
Table: 1: Comparison of different parameters of full adder in adiabatic logic with CMOS

	Logic style	Power dissipation (Watts)	Memory Space allocated (bytes)	Average no. of Newton iterations	Number of transistors	Latency (%)
S U M	CMOS	2.4029 E-10	43274240	3.89928	28	0.000
	ECRL	4.2591 E-07	43274240	4.93630	28	0.000
	PFAL	1.2857 E-10	43274240	4.37168	30	0.000
	2PASCL	1.0448 E-11	43274240	4.38441	28	0.000
	PFAL&2PASL	3.7550 E-11	43270144	3.88861	32	0.000
C A R R Y	CMOS	1.0020 E-10	43294720	3.19901	12	0.000
	ECRL	1.5400 E-06	43282432	4.49095	18	0.000
	PFAL	1.1840 E-10	43286528	4.47440	20	0.000
	2PASCL	9.1543 E-12	43282432	3.86297	14	0.000
	PFAL&2PASL	2.6742 E-11	43286528	4.19346	22	0.000

Table 1 shows that the power dissipation of different adiabatic logic styles is lesser than the conventional CMOS design. The power supply that is given to the adiabatic circuits is also lesser than the conventional CMOS design**.**

VI.   CONCLUSION

This paper proposes energy efficient adiabatic logic for digital circuits. The results were simulated using PSPICE and comparison has been done for different parameters of full adder in different adiabatic logic styles and CMOS design. The results show that the proposed adiabatic logic has less power dissipation compared to conventional CMOS design and it also uses less power supply. These advantages made this logic more convenient for energy efficient digital applications.

REFERENCES

[1]   Atul Kumar Maurya and Ganesh Kumar, "Adiabatic Logic: Energy Efficient Technique for VLSI Applications", International Conference on Computer& Communication Technology (ICCCT)-2011.

[2]   Vojin G. Oklobd"zija, Dragan Maksimovi' c, "Pass-Transistor Adiabatic Logic Using Single Power-Clock Supply ", IEEE Transactions on Circuits and Systems, Vol. 44, No. 10, October 1997.

[3]   A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low power CMOS digital design,'' *IEEE J. Solid-State Circ.*, vol. 27, no. 4, pp.473-484, Apr. 1992.

[4]   T. Indermauer and M. Horowitz, "Evaluation of Charge Recovery Circuits and Adiabatic Switching for Low Power Design," Technical Digest IEEE Sym. Low Power Electronics, San Diego, pp. 102-103, Oct. 2002.

[5]   Arsalan, M. Shams, M., "Charge-recovery power clock generators for adiabatic logic circuits", 18th International Conference on VLSI Design, pp. 171- 174, 3-7 January 2005.

[6]   Dragan Maksimovic et al, "Clocked CMOS adiabatic Logic with Integrated Single Phase
Power Clock Supply", IEEE Transactions on VLSI Systems, vol 8, No 4, pp 460-463, August 2000.

[7]   W.C. Athas, L. Svensson, J.G. Koller et ,N.Tzartzanis and E.Y.Chou: "Low-power Digital Systems Bared on Adiabatic-switching Principles". IEEE Transactions on VLSI Systems. Vol. 2, No. 4, pp. 398-407 December. 1994.

[8]   Satyam Mandavilli, Prashanth Paramahans " An Efficient Adiabatic Circuit Design Approach for" International Journal of Recent Trends in Engineering, Vol 2, No. 1, November 2009 Low Power Applications.

[9]   A. Vetuli, S. Di Pascoli, and L.M. Reyneri, "Positive feedback inadiabatic logic," Electron.Lett.,vol.32, pp.1867-1869, Sept. 1996.

[10]   N. Anuar, Y. Takahashi, T. Sekine, "Two phase clocked adiabatic static CMOS logic," proc. IEEE SOCC 2009, pp. 83-86, Oct. 2009.

[11]   N. Anuar, Y. Takahashi, T. Sekine, "Two-Phase clocked adiabatic static CMOS logic and its logic family" Journal of semiconductor technology and science, vol 10, no. 1, Mar. 2010.

Authors:

B. Dilli kumar , Student, is currently Pursuing his M.Tech VLSI., in ECE department of Sree Vidyanikethan Engineering College, Tirupati. He has completed B.Tech in Electronics and Communication Engineering in Jawaharlal Nehru Technological University, Anantapur. His research areas are VLSI, Digital IC Design, and VLSI and Signal processing.

M. Bharathi, Assistant Professor, Department of ECE, Sree Vidyanikethan Engineering College (Autonomous), Tirupati, India. She has completed M.Tech in VLSI Design, in Satyabhama University. Her research areas are Digital System Design, VLSI Signal Processing