High Speed Architecture Design Of Viterbi Decoder Using Verilog HDL

Karri Megha Shyam¹, B.N. Srinivasa Rao², R. Prasada Rao³
¹Final M.Tech Student, ²Assistant Professor, ³Assistant Professor
Dept. of Electronics and Communication Engineering, Avanthi Institute of Engineering & Technology, Narsipatnam, Visakhapatnam, Andhra Pradesh.

Abstract: The main purpose of this study is to yield the gains obtained by the developers with the usage of Viterbi algorithm. Research mainly centers on the grandness of Viterbi algorithm in the practical applications with the VHDL code. Research not only helps the students related to the communications but it also helps the people who are in the field of decoders as it is one of the efficient method for reducing the errors while communication procedure is in advance. Here, VHDL code is used in order to implement the Viterbi algorithm in a proper way. Apart from various codes, researcher selected VHDL code for this research as it offers the high capability in designing the electronic systems. Students and the business people and one can easily understand and analyze the Viterbi algorithm concepts and can gain more knowledge on the VHDL code and the tools that are used in this research.

I. Introduction

Error correcting code is a method to find the errors sequentially and correct it based on the remaining constraints such as bit length etc. This study is so called as coding theory. Error detection is the simple method that is checking of digits, applications are credit card number mistakes. It is also called as the block codes. These are mainly used in the CD players and mobile phones. The sum of the digits given the module of some number.

In the coding theory forward error correction is a method used for controlling errors in the data exchange in noisy channels. The main theme is the sender encode his message using error correcting codes. The receiver receives the encoded message and find the errors in the message avoiding the retransmission. This gives the ability to avoid resending the data in the reverse channel in fixed band width.

This technique is applied where the situations are about to retransmission is more cost effective and one way communication. The information which is sending is stored in the storage devices to reveal the corrupted data. It uses digital bit stream with the modular carrier. It is used in multicast communications also.

FEC processing in a receiver may be applied to a digital bit stream or in the demodulation of a digitally modulated carrier. It is an integral part of the initial analog-to-digital conversion. Most of the researchers uses bit error rate to find the bit errors and it depends on the length of the message. Viterbi decoder implements a soft-decision algorithm to demodulate digital data from an analog signal corrupted by noise.

Forward Error Correction codes are divided into two types.

- **Block codes** work on fixed-size blocks (packets) of bits or symbols of predetermined size. Practical block codes can decoded in polynomial time to their block length.
- **Convolutional codes** work on bit or symbol streams of arbitrary length. They are decoded with the Viterbi algorithm and other algorithms are used. Viterbi decoding allows asymptotically optimal decoding efficiency with increasing constraint length of the convolutional code and at the expense of exponentially increasing complexity. It can be turned into a block code, if desired, by "tail-biting".

II. RELATED WORK

There are more number of block coding techniques in that the most of them is related to hamming distance. Hamming ECC is commonly used to correct NAND flash memory errors. It gives single-bit error correction and 2-bit error detection. These are only compatible for more single level cell (SLC) NAND. Denser multi level cell (MLC) NAND requires multi-bit correcting ECC such as BCH. NOR Flash typically does not use any error correction.

The traditional block codes are usually implemented the decision algorithms every input there is output signal. That means wherever needs decision is 1 or 0 bit. Soft-decision algorithms like the Viterbi decoder process analog signals and allows for much higher error-correction performance than hard-decision decoding. The traditional block codes apply the algebraic properties of finite fields.

A convolutional code is a wing of error-correcting code in which consists of

- each m-bit information symbol converted into n bit symbol, where m/n is the code rate (n ≥ m) and
• Converting is a function of the last $k$ information symbols, where $k$ is the constraint length of the code.

Convolutional codes are used in most of the applications and it mainly used in the video communication. These are mainly used in the hard decision codes. It encodes the data and stored in 1 bit registers which is indexed and starts with 0. The encoder has $n\text{mod}2$ adders where the logic is: $0+0 = 0$, $0+1 = 1$, $1+0 = 1$, $1+1 = 0$, and $n$ generator polynomials one for each adder. An input bit $m_i$ is stored in leftmost register. Generator polynomials are used and the encoder outputs $n$ bits. Bit shift all register values to the right represented as $m_1$ moves to registers represented as $m_0$, $m_0$ moves to $m_1$ and wait for the next input bit. If there are no remaining input bits and the encoder continues output until all registers have returned to the zero state.

Several algorithms exist for decoding convolutional codes. For small values of $k$ the Viterbi algorithm is universally used as it provides maximum likelihood performance and is highly parallelizable. We use Viterbi decoders are thus easy to implement in VLSI hardware and in software on CPUs with SIMD instruction sets.

Details of Errors occurred during the coding in communication process:

Transferring of data from one person to another person is called communication which requires more programming for the mechanism and there is chance to get errors in the signal. If there are simple errors there are adjusted using the sequence.

But major problems can be solved randomly utilizing few of the important features of Viterbi algorithm which yields to the original sequence. The most important feature for communication is to facilitate error free data transmission among digital or analog functioning signals along with amplification. Coding in communication system is divided into four sections as

1) Encryption: mainly used for security of data,
2) Data compression: used for data streaming and to reduce the space,
3) Error translation: used to demonstrate the data for transmission of communication channels
4) Error Control: identifies the errors and correct them as soon as possible.

Digital signals are represented as 0 and 1 and detecting errors and the noise occurred during the transmission is used for the correct those errors. Wired communication can leads to the errors due to the random motion and transmit through the conductors such as registers. In wireless communication there are some resources for noise such as mobiles gives disturbance to signal. The original signal is normally added with the noise signal at receiver input. The forward error correction auto repeat request (ARQ), hybrid ARQ and error code correction (channel coding) are the general methods used for error correction [9].

III. PROPOSED WORK

In our work we introduced a solution for block codes and provide continues data stream. For we choose Viterbi algorithm. In Viterbi algorithm we provide continues data stream for bit streams. In Viterbi algorithm, we need to find the shortest path for the set of observations. For finding the shortest path we use trellis representation in this algorithm. Trellis graph is used to represent the observation path. It uses forward error correcting coded based on the convolutional codes.

Viterbi algorithm uses syndrome trellis coding and its is explained as follows.

The trellis will be assumed to have a periodic structure and the meaning that the Viterbi decoding algorithm operations will be the same for every state transition interval. To construct such a trellis, we can use a memory-$\nu$ binary shift register whose contents at any given time define the state of the trellis. The states are represented as 00, 01, 10 and 11.

![State Transition](image)

The Viterbi decoding algorithm is a decoding process for convolutional codes for a memory-less channel. It defines the normal flow of the noisy channel and error recovery adds the duplicate information to the original information I and output t is transformed through a communication channel. Input at receiver is the information with redundancy. The receiver extract the original information through a decoding algorithm and generates an estimate (e). A decoding algorithm increases the probability $p(r|e)$ is a maximum likelihood (ML) algorithm. An algorithm which maximizes the $p(e|r)$ through correct selection of the estimate (e) is called a maximum a posteriori (MAP) algorithm. Two methods have same results when the source information i has a uniform distribution.
The main tasks in the Viterbi decoding process are as follows:
1. Quantization: Conversion of the analog inputs into digital.
2. Synchronization: Detection of the boundaries of frames and code symbols.
3. Branch metric computation.
4. State metric update: Update the state metric using the new branch metric.
5. Survivor path recording: Tag the surviving path at each node.
6. Output decision generation: Generation of the decoded output sequence based on the survivor path information.

The below block diagram shows the Viterbi decoding algorithm performs the above tasks in the specified order. It has different parts have different works. In this process the signals are quantized and converted into digital signals. The block detects the frame boundaries of code words and symbol boundaries. We consider that the Viterbi decoder receives successive code symbols and in which the boundaries of the symbols and the frames have been identified.

1. **Branch Metric Unit (BMU):** It calculates the shortest length between the input pairs and ideal pairs.
2. **Path Metrics Calculation:** For every state it calculates for survivor ending in a metrics needed.
3. **Trace back:** To get the expected results this is responsible to be simulated at the hardware implementations that don’t store the actual information regarding the survivor paths. But are stores one bit of information every time.

   The branch metric computation block compares the received code symbol with the expected code symbol and counts the number of differing bits. The state metric update block selects the survivor path and updates the state metric.

   Each wing is usually implemented by a module called Add-Compare-Select module. Both adders compute the partial path metric of each branch and the comparator compares the two partial metrics and the selector selects an appropriate branch. Novel partial path metric updates the state metric of state p and the respective survivor path-recording block records the survivor path.

   The number of necessary ACS module is equal to half the number of total states. Time sharing of some ACS modules is possible to save the hardware and such sharing slows down the operation and dissipates more power. In this gist we reckon replication of necessary ACS modules and which is more power efficient.

### IV.EXPERIMENTAL RESULTS

The input values for Viterbi encoder are specified in the developed code. Providing input every time for the developed design is time taking process. So, the input values are included directly in the developed code, so that simulation process can be executed directly. The Viterbi encoder input values given in this project are:

```
0110100110010110100101100110100110010110011010010
1101001100101101001011001101001011010011001011001
1010
```

Each input value will be processed and a corresponding output will be provided for the Viterbi encoder. The output values will be specified in the form of wave forms in both Xilinx and active HDL simulation environments.
ANALYSIS OF SIMULATION USING XILINX

When clock signal is applied to the Viterbi decoder reset button is set as 0, and the system reset button kept as 0, the cyclic encoded data starts after 100ns by applying the valid encoded pulse train to the decoder enc_symbol 0 and enc_symbol 1 varies according to the periodic pulse train. According to the enc_symbol the encoded output bit also a pulse train.

The dec_symbol 0 consists an 3'h0 error bits at decoder process up to 100ns, after 100ns it decodes 3bits at a time changes continuously every 50ns. dec_valid_in is a continuous pulse train when dec_symbol is change their bit stream every after 100ns. Thus we get dec_out bit and dec_valid_out bits same as 1. the count of decoder is 103 and the buf_in_cnt as 102. from that the decoder buf_out_cnt and total count can be represented as 0 bit count.

The concerned output for the above encoder is

031211211022332212022131231100110223322231100112
13112021022332212022131231100110
112131120210223322231100

And for decoded symbol 1 when the value is given as 7 then the output is the demux value given as 0 7 0 7 0 7

When decoded valid input value is given as ‘0’ then the output is continues signal.

For a pattern value when given as ‘3’ then there will be no changes in the signal and similar appears when the decoded bit output, decoded valid output and decoded output error value is set to ‘0’.

When glb_seed value is set to 000E4048 then there appear a demux in the result. For cnt, value is set to 1 then the result 104101010101010101010101010101010101010101010

And finally for buffer output count, total count and sim done value when set to ‘0’ the n there will be no changes in the signal.

Implementation of Viterbi encoder can also be simulated with the help of active HDL simulation environments. Active-HDL is an Aldec product developed using Field Programmable Gate Array (FPGA) with HDL simulator. The main reason for choosing this tool for simulation is that it can support graphical and text based designs with various simulation languages.

Synthesis and Implementation

The design can be synthesized and implemented after verifying the design behavior with simulations. The process of synthesis and implementation can provide a clear view on how the developed code is working for obtaining simulation results.

The entire code developed for this project can be visualized using Xilinx hardware device. How the Viterbi algorithm code for encoder and decoder is working in a step by step process can be analyzed based on results of implementation.
Checking the details of the design after implementing each and every action is necessary. Synthesis report can provide an opportunity to view all the resources utilized by the developed design.

Implementing the design in FPGA editor can provide the below results. This view is providing in-built working process and routing information.

A user can verify the design before using it in a device; floor planner view can provide the opportunity to identify the Viterbi decoder position. Positions of all components used while developing the design can be obtained by just a click.

All the trellis occurred are arbitrarily solved even in presence of two or more simple errors in input string using Viterbi algorithm and at same time the in presence of more errors the decryption will be low even then the algorithm works effectively this is the main advantage in implementation of Viterbi algorithm. The Use of this algorithm is found to be advantageous due to its cost effectiveness in modulated minimize at the same time the functional performance in some situation would modulate in maintaining the original cost. Linear functioning of linear pulse distance is due to convenient source sequence.

Analysis:

The implementation of Viterbi algorithm is somewhat difficult even though the process of algorithm is simple. Conventional encoding can be easily implemented on Viterbi algorithm even though there exist a large gap in complexity with the transmission side. State trellis uses conventional encoding, the decoder explores rotates between states because it is a finite state machine. It requires large memory registers for storing results. There is some delay in final decision on a sequence of transitions because of the size of the input code is very high. By observing the transition metrics between states the decision can be done and the results are updated in the form of Hamming distance or Euclidean with the error-corrupted received sequence.

The computation process of conventional codes depends on the minimum distance and then on the constraint size and coding speed. There are continuous changes in implementation process in order to increase the parameters like Gain. Complexity raise up to maximum limit in order change the old techniques. Now a day’s some algorithmic part and Systolic architectures in implementing on various devices Adaptive Viterbi decoding (AVD). Only subsets of the states are used in AVD algorithm for storing and implementation process. Due to decrease in size of states, the performance also reduces. In order to increase the performance of decoder, it is implemented at shorter distances. When channel status information is available, Replace stronger codes with simpler codes for high speed switching between different coding rates.

For better use of power and coding rates in circuits’ adaptive channel coding systems are used. The adaptive decoder algorithm must contain programmability or re-programmability at hardware logic level or algorithmic level in order to increase the computation levels. Field programmable gate array device is mentioned here for achieving both parameters power and coding rate.

The fundamental concept used in Software radio terminal is re-programmability which is present either at hardware level or algorithmic level. An interface with different communication standards are used in Software defined radio terminals and it must consist of high decoding capability for reprogrammable devices. Viterbi decoder use convolution codes for channel decoding in its programmable architecture and is similar to a special class of standards and specifications.

Viterbi decoder program is used for switching between UMTS and GPRS whenever the implementation uses only decoder, reconfiguration is not a major problem. FPGA holds the total transceiver digital processing sub-system in real time applications. In order to decrease the
problems in design process re use the same building blocks. At transmission time for particular application programmability is used where data coding rate is continuously changed at run time.

The Viterbi decoding process conventional codes of fixed size of 5 and 9 and the code rate ½ and 1/3 by using FPGA there is possibility of implementing extra features in the Viterbi decoder (e.g. different standards and new functions).

IV. CONCLUSION

As Viterbi algorithm is conceived more interesting and challenging for this research topic, it is considered, and also it has wide variety of applications in digital communications field. This research helps to generate more profits by the developers using Viterbi algorithm. This research mainly concerned with implementation of Viterbi algorithm using VHDL coding. Viterbi algorithm has many advantages like low power consumption and main advantage is error correcting using VHDL. Anyone reading this document will have to gain the cognition of working with different tools like Xilinx ISE and MODELSIM.

References:


BIOGRAPHIES:

Karim Megha Shyam completed B.Tech Degree in Electronics and Communication Engineering from Al-Ameer College of Engineering & Information Technology, Visakhapatnam. currently pursuing M.Tech in from Avanthi Institute of
Engineering & Technology, Narsipatnam, Visakhapatnam, Andhra Pradesh. Interesting research areas VLSI custom design.

B.N. Srinivasa Rao received his B.Tech degree in Electronics and Communication Engineering from JNT University, Hyderabad, India and M.Tech in VLSI System Design from JNT University, Hyderabad, India. He is currently working as an Assistant Professor in Avanthi Institute of Engineering and Technology, Visakhapatnam, Andhra Pradesh, India. He has 5 years teaching and 9 years industrial experience. He has 10 publications in various International conferences. His area of interest VLSI Semi and full custom design. He guided many projects for B.Tech and M.Tech students.

R. Prasada Rao received his B.Tech degree in Electronics and Communication Engineering from Andhra University, Visakhapatnam, India and M.Tech in VLSI System Design from JNT University, Hyderabad, India. He is currently working as an Assistant Professor in Avanthi Institute of Engineering and Technology, Visakhapatnam, Andhra Pradesh, India. He has 8 years teaching experience. He has 2 publications in various International conferences. His area of interest is Digital Electronics, Signals and Systems and Signal Processing. He guided many projects for B.Tech and M.Tech students.