Dynamically Reconfigurable RISC Microprocessor design using MIPS Instruction Set

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Abstract: *Today's world suggests multifunction in each products. This paper design a RISC processor using MIPS instruction set architecture which supports multifunctioning. Dynamic Reconfiguration refers to the ability of the Processor to update its internal Instruction Decode and Execute stage in order to support new functions, while the system is running. This project presents a principle on how performance can be improved in the context of microprocessor Units applications, using the MIPS instruction set.*

Keywords - *RISC, MIPS, dynamically reconfigurable.*

I. INTRODUCTION

MIPS can be abbreviated as Microprocessor without Interlocked Pipelining Stages. It was first developed by Sony, Nintendo and NEC. It was developed to overcome the problems of the conventional design i.e. using same instruction set for all the applications makes instruction set busy and system a delaying system. MIPS processor core assigned different formats for certain instructions for their easy implementation.

RISC CPU have more advantages, such as reduced number of instructions, faster speed, and simplified structure easier implementation. RISC CPU is extensive use in embedded system. RISC processor has a load store load instruction.

This paper is a zoom in on how the MIPS instruction Set is embedded in an RISC Processor by increasing the performance.

II. LITERATURE SURVEY

In this section we briefly review some of the works of designing RISC static processors.

In the scheme presented in [1] ensure the power reduction of a RISC processor .Here they created a RISC processor using MIPS architecture .They included clock gating and multi Vt technique to reduce the power. They have also incorporated hazard detection unit to remove the hazards if any.

In the paper [2] a RISC processor has been designed in FPGA. They adopted top-down design method and use VHDL to describe system. They analyzed MIPS instruction format, instruction data path, decoder module function and design theory based on RISC CPU instruction set.

In the section [3] Stall in MIPS architecture has been reduced to maximum. Stall frequently happens in pipeline architecture which results in larger clock cycles. Here they reduced stall by introducing pre-fetching unit.

Another work [6] propose a 16-bit non-pipelined RISC processor, which is used for signal processing applications with 24 instruction set.

III.PROPOSED WORK

A. MIPS PROCESSOR ARCHITECTURE

Architecture of MIPS RISC microprocessor includes, fix-length straight forward decoded instruction, memory access is limited to load and store instruction format, a large general purpose register file.

The 32 bit RISC MIPS processor has 5 stages.

1. Instruction fetch (IF)
2. Instruction Decode (ID)
3. Execution (EXE)
4. Data memory (MEM)
5. Write back (WB)

The MIPS single cycle processor performs the tasks of instruction fetch, instruction decode, execute and memory access and write back all in one clock cycle.

The architecture of RISC processor is shown in fig 1 with all the 5 Stages. Pipeling improves the performance of the processor

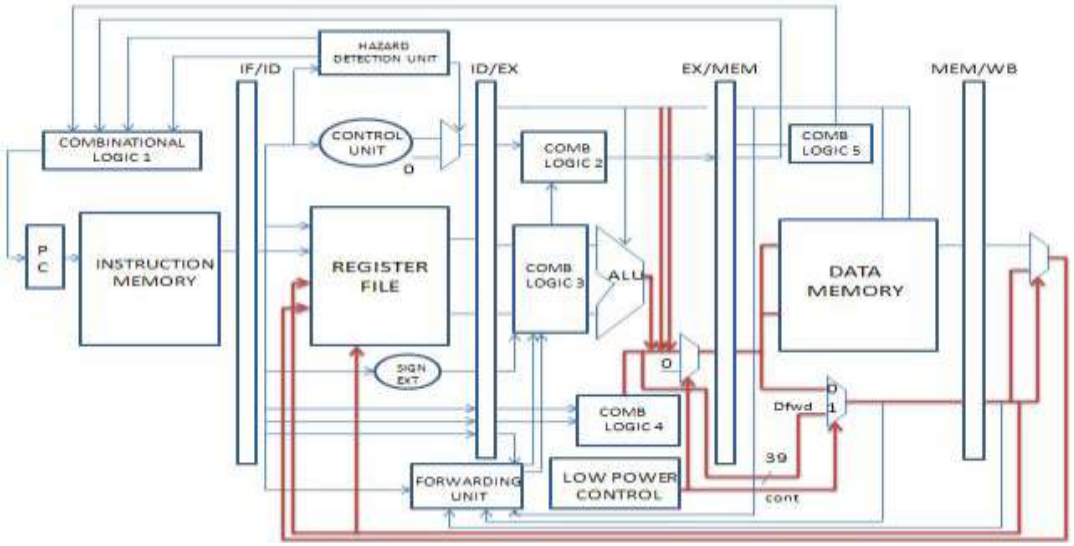


Fig 1: Block Diagram of RISC processor

B. DYNAMIC PROCESSOR

Processor that can automatically configure is called dynamic processor. Here the processor has been designed as 8 bit processor, 16 bit processor and 32 bit processor. According to our need we can reconfigure our processor.

By providing selection lines we can select the corresponding processor. We have provided 2 bit selection line.

- 01--8 bit processor
- 10--16 bit processor
- 11—32bit processor

In real time projects it provides the flexibility to switch between the processors.

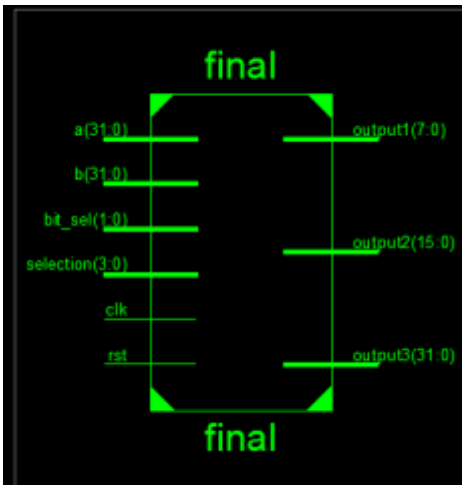


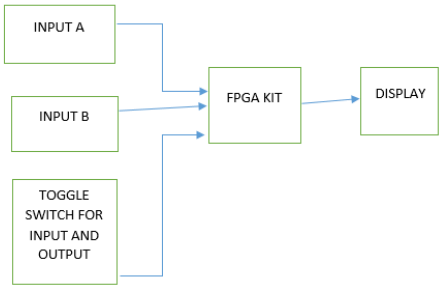
Fig 2: Schematic view of dynamic processor

Algorithm:

1. Accept the inputs as 32 bit
2. Select the processor.
3. If the processor is 8 bit, Load 8 bit LSB of inputs.
4. If the processor is 16 bit, Load 16 bit LSB of inputs.
5. If the processor is 32 bit, load the complete value.
6. Select the instruction.
7. All the values are fetched, decoded and executed.
8. The result will be stored in the output register
9. According to the processor selection only the corresponding set of registers will be active.
10. The output will be displayed in corresponding 8 bit,16 bit,32 bit output lines.

C. FPGA IMPLEMENTATION

The processor is synthesized in Xilinx FPGA. Field programmable gate array.



IV. RESULTS

The Processor is designed in VHDL ,simulated with ModelSim. The synthesis tool Xilinx Spartan - 3E was used to verify results and for implanting the work in FPGA.

Fig 3: 8 bit RISC processor

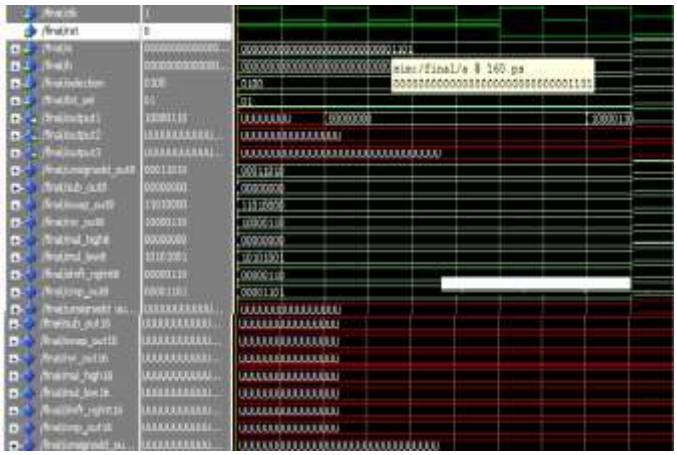


Fig43: 16 bit RISC processor

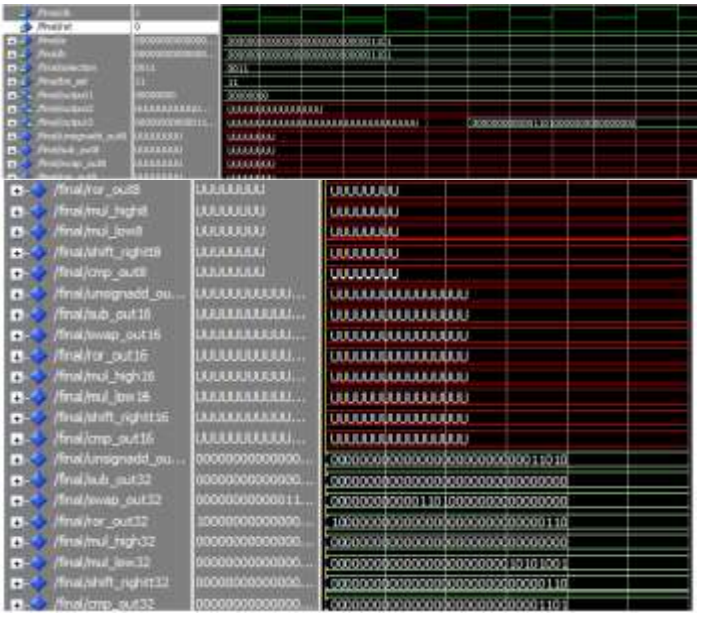


Fig 5: 32 bit RISC processor

V. Conclusions

The proposed system is designed for better performance. The processor was successfully designed in Verilog HDL, simulated with ModelSim 10.4 and synthesized on to a Xilinx Spartan-3E for FPGA implementation. The system can be rec configured itself while the processor is running Future work can be done by adding number of instructions .

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