International Journal of Engineering Trends and Technology
ISSN: 2231–5381 / https://doi.org/10.14445/22315381/IJETT-V71I12P222

Volume 71 Issue 12, 225-232, December 2023

Original Article

Design of DC-DC Boost Converter Single Input Dual Output for WSN Application using 180nm CMOS Process Technology

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Received: 18 July 2023 Revised: 11 September 2023 Accepted: 20 November 2023 Published: 06 December 2023

Abstract *- This research introduces a dc-dc boost converter single input dual output design for wireless sensor network (WSN) applications. The WSN applications are used in various fields such as environmental monitoring, healthcare systems, industrial automation, and other fields dealing with electronic devices where power management is crucial. The designed converter was a synchronous boost converter with single input dual output with the advantage of improving flexibility. It can be used where different components may require different voltages, reducing complicated control systems and being much more cost-effective for WSN applications. The control circuits were obtained in a 180 nm CMOS process together with the boost converter. The simulation result demonstrated the effective amplification of the input voltage of 1.8V by the converter, resulting in two output voltages of 3.3V and 5V. The device also yields 83.4% efficiency ranging from 20mA to 220mA load current. This converter is suitable for WSN applications.*

Keywords *- Boost converter, Dual output, Power management, Synchronous topology, Wireless Sensor Network.*

1. Introduction

A wireless sensor network or WSN is a network made up of spatially distributed nodes that can transmit data to each other and monitor natural or physical conditions [1]. A WSN node connects a single or numerous sensors distributed in large quantities. It can be made up of a few, several, hundred, or even thousands of nodes. The sensors gather data that they will transmit to the nodes. The collected data is then processed and analyzed in accordance with the needs of the system. This process is done wirelessly between the nodes and the hub [2]. These nodes are resource-constrained and concurrently extremely dependent on battery management, storage capabilities, multiplication, data/signal size, and accessible bandwidth [3].

For applications involving wireless sensor networks, power management is crucial. This is because systems often consist of multiple subcircuits, each needing a different voltage level. There is a need to supply a well-regulated voltage for various integrated circuits. Power management is essential in cases like high-precision analog sensing components requiring a voltage that does not drift or a sensor node component needing a greater voltage than the battery can supply. Rather than using a lot of batteries to supply the different components of the device, the right power management system will help alleviate the space problem [4-7] and efficiency. One good approach to producing various controlled voltages from a single source is by using DC-DC boost converters.

Single Input Single Output (SISO) DC-DC boost converters with different voltage gains can be merged to produce the desired various output voltages; however, it influences the cost and control scheme of the system, making the control structure complex [3, 8, 9]. Existing boost converter topologies are not cost-effective and may be inefficient regarding flexibility.

In order to address these challenges, the researchers intended to design a synchronous boost converter with single input dual output using CMOS process technology with the advantage of improving flexibility since it can be used where different components may require different voltages, reducing complicated control systems and much more cost-effective for WSN applications. The proposed system consists of a boost converter with single input dual output, which can provide a step-up output voltage. It uses a pulse width modulation technique that produces a fixed frequency and fixed amplitude pulse train with variable pulse width.

2. Review of Related Literature

The work of N. Amira et al. [10] discusses the importance of the boost converter in power management in wireless sensor networks. It demonstrates several problems that are applicable to designing a boost converter. The technology and topology of this work were inspired by S. Bose et al. [11], which gives high efficiency, and the control technique for the designed dc-dc boost converter was built using the method of C.S. Lee [9].

Table 1. Summary of related literature

Parameters	[10]	[11]	[9]
Technology	Not Specified	CMOS 180nm	CMOS-350nm
Topology	Asynchronous	Synchronous	Not Specified
Number of Outputs	Single Output	Single Output	Single Output
Conventional Efficiency	70%	75%	82%
Mode of Conversion	Boost	Boost	Boost

3. Methodology

The system overview of the proposed design of the single input dual output dc-dc boost converter for WSN application using 180nm CMOS process technology is shown in Figure 1.

Table 2. DC-DC boost converter desired specifications

Parameters	Desired Values	
Technology	180nm CMOS	
Voltage Input Range	1.7V-1.8V	
Voltage output	3.3V	5V
Efficiency Conversion	78%-85%	
Switching Frequency	500kHz	
Minimum Loading Current	<10mA	
Maximum Loading Current	200mA	

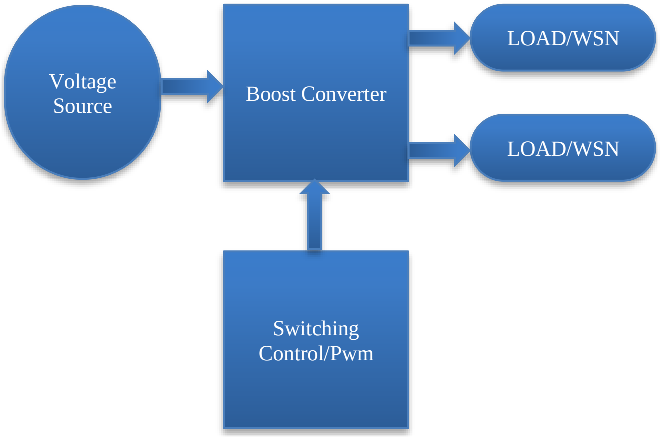

Fig. 1 System overview

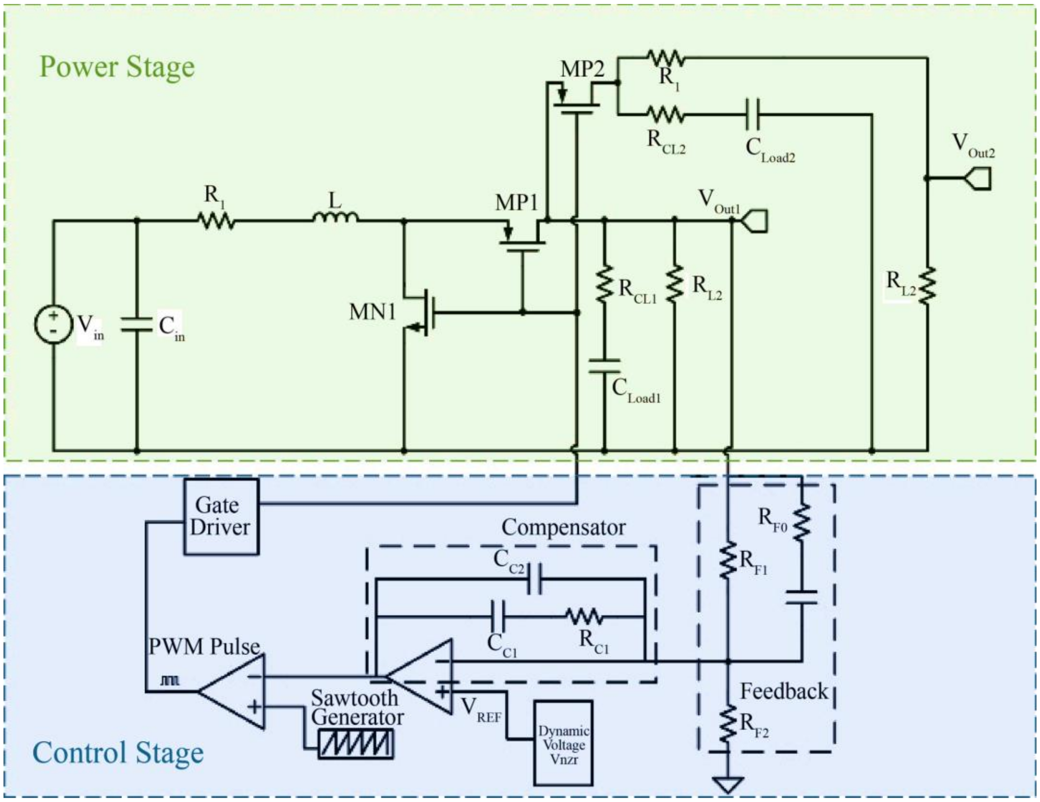

Fig. 2 A Boost converter with single input dual output system

Figure 2 depicts the overall schematic of the proposed design boost converter; it has a single input voltage with a dual output voltage of 3.3V and 5V. The boost converter utilizes pulse width modulation to control the operation of the power MOS switch. The proposed DC-DC boost converter was divided into subcircuits: the power stage and the control stage. A capacitor, inductor, a diode, and a switch (CMOS) compose the power stage of a DC-DC boost converter. Meanwhile, the control stage consists of subcircuits: the bandgap reference voltage, error amplifier, compensator, PWM control, and driver.

3.1. Power Stage

The PMOS in the power stage was used on the high side of the switch, and NMOS was used on the low side. In order to maintain stable output voltages, a feedback loop was employed to regulate the duty cycle of the switch signal based on the voltage level of the two outputs. The power stage devices are connected, as shown in Figure 3.

3.2. Control Stage

The steady-state output of the boost converter can be controlled by adjusting the duty cycle. Therefore, we use a control circuit in the switch to adjust the duty cycle. Because of this, additional circuitry is required to change the duty cycle, and thus the amount of time the inductor receives energy from the source, to create a full dc-dc boost converter single input dual output system.

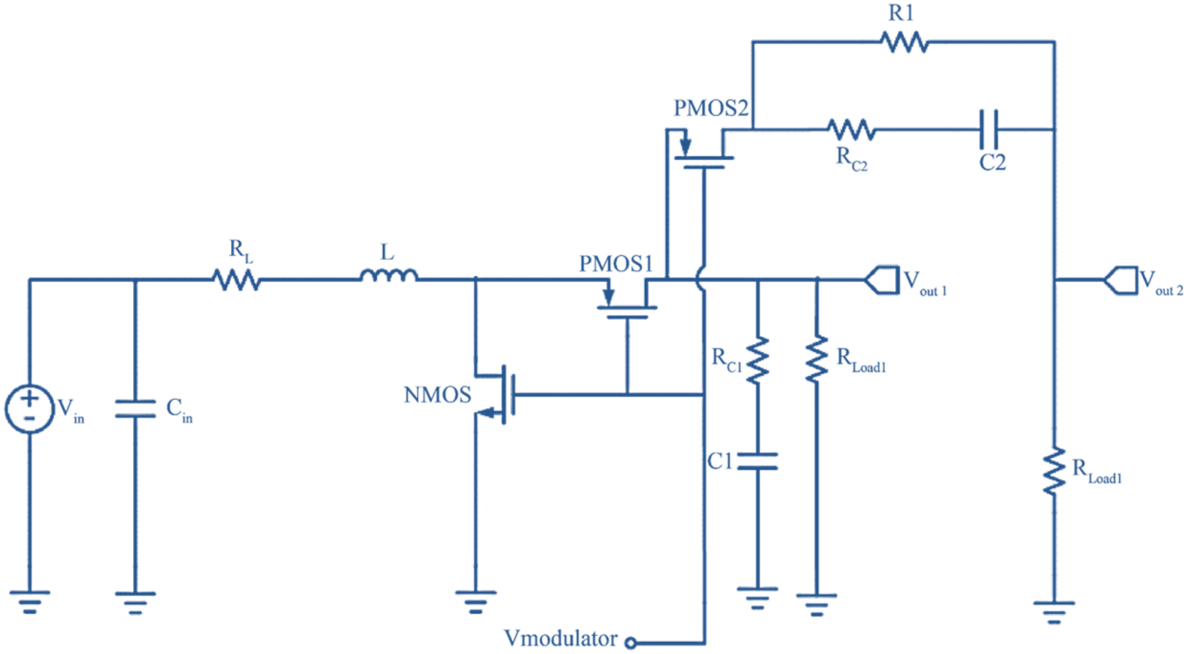

Fig. 3 Power stage

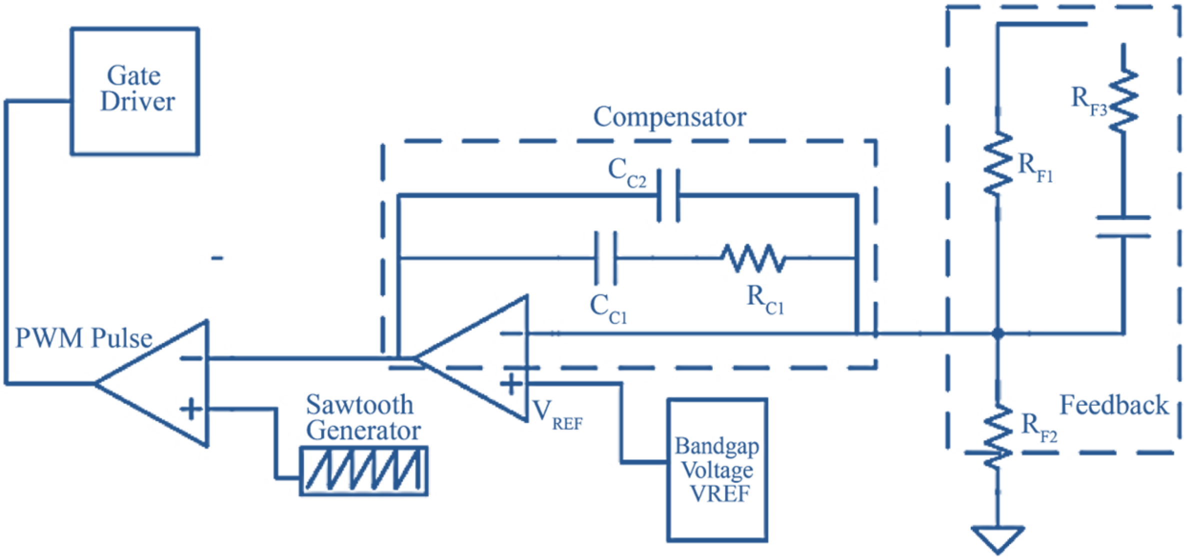

Fig. 4 Control Stage

Table 3. Compensation type and location of zero crossover frequency

Compensation Type	Relative location of the crossover and power stage frequencies
Type II	FLC<FESR<Fc
Type III – A	FLC<Fc< FESR<Fs/2
Type III- B	FLC<Fc<Fs/2< FESR

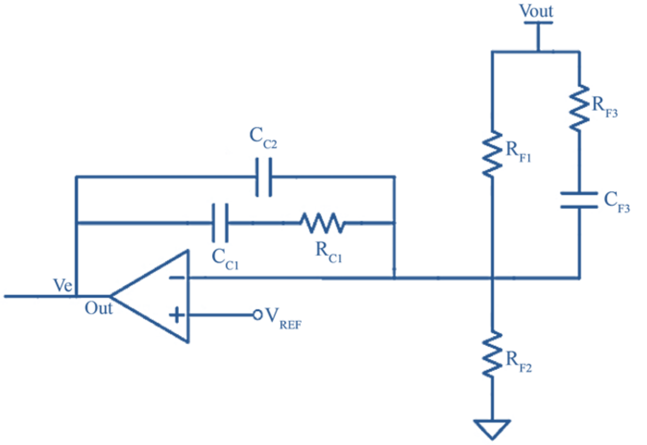

Fig. 5 Compensation circuit

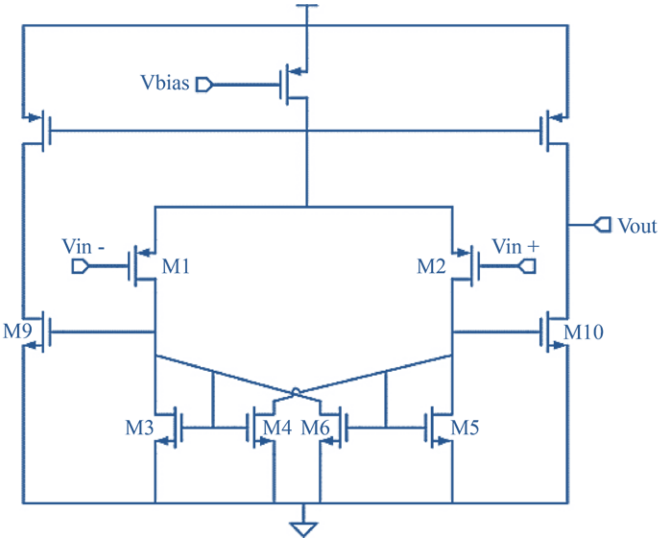

Fig. 6 Hysteresis comparator

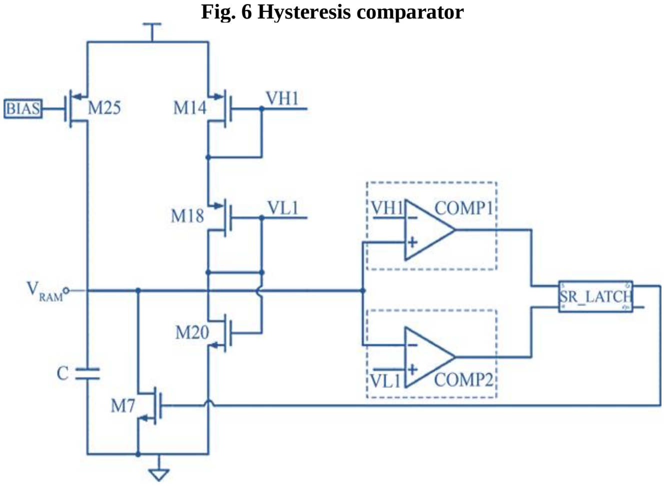

Fig. 7 Ramp generator

Figure 4 illustrates an error amplifier that uses a feedback route to sense the output voltage V1 and V2 across the load and regulate the switch. The most widely used control technique is pulse width modulation (PWM), which regulates the duty cycle of the circuitry.

3.3. Compensation Circuit

Compensation type must be considered, especially in designing a voltage regulator. The compensation that is used in this design is the Type III compensation, as illustrated in Figure 5, which is an external component extension to the error amplifier. The circuit comprises resistors and capacitors that serve as phase and gain shapers for the power stage. Having a higher gain of the system can improve the line and load regulation. The Type III compensators can provide output voltage stability in the proposed design of the boost converter system by solving the appropriate values for the capacitors and resistors.

Type III compensation is employed in the proposed boost converter because, aside from its greater stability advantages compared to other types of compensation, the solve parameters conform to the type III compensation. Table 3 shows the summary for the compensation type and location of zero crossover frequency of the boost converter.

3.4. Hysteresis Comparator

A comparator is an electronic device that generates a binary output by comparing an input voltage signal to a reference voltage. The comparator's output level depends on whether the input signal is greater or less than the reference voltage. Hysteresis is usually implemented using positive feedback from the output terminal. It also refers to the variation between the input signal voltages at which the comparator's output is completely ON or completely OFF. Figure 6 shows the schematic of the hysteresis comparator.

3.5. Ramp Generator

The ramp generator has the same principle as the oscillator. It has a vital role in controlling the frequency and duty cycle of Pulse-Width-Modulated (PWM) switching systems. Figure 7 shows the schematic of the ramp generator used in this study.

The designed circuit consists of a reset switch controlled by two comparators whose reference signals establish the lower (VL) and upper (VH) voltage limits of the ramp and a current source for timed charging of the capacitor. Figure 7 depicts the schematic circuit of the ramp generator.

To generate the ramp signal it starts by charging capacitor C with a constant current from transistor M25 until the voltage across the capacitor reaches the upper limit VH, causing the output of comparator 1 (COMP1) to go high. At this point, transistor M7 discharges the capacitor with a current much larger than the charging current, resulting in a rapid drop in the ramp signal until it falls below VL. When the ramp signal drops below VL, the output of comparator 2 (COMP2) goes high, triggering the input terminal R of the flip-flop and causing the output Q to change from high to low, which turns off transistor M7. This marks the start of a new cycle, and the process repeats periodically.

3.6. Voltage Reference

The purpose of the bandgap voltage reference circuit is to generate a stable voltage reference VREF that remains unaffected by variations in temperature, supply voltage, and process variations.

This ensures that the circuit's performance is consistent and reliable regardless of changes in these factors. In this study, a low voltage and low power bandgap reference is designed. The voltage bandgap design has a startup architecture to ensure stable and reliable startup reference voltage. Figure 8 shows the schematic circuit of the voltage reference.

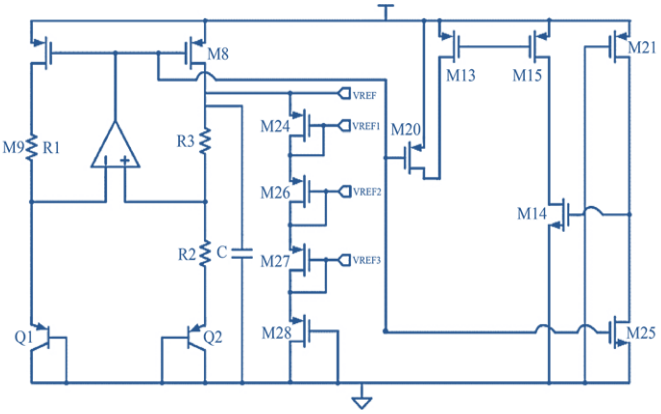

Fig. 8 Voltage reference

4. Results

4.1. Simulation Results

The results from simulating the proposed dc-dc boost single input dual output converter are shown in the figures below. The output voltage summary is shown in Table 4.

Table 4. Boost converter output summary with corners

Corner	VBOOST	$I_{Inductor}$	I_{LOAD}
TT, vdd = 1.8V, temp = 25°C	3.34 V, 5.02 V	1.2 4 A	222 mA, 223 mA
FF, vdd = 1.98V, temp = 0°C	3.35 V, 5.06 V	1.27 A	223 mA, 225 mA
SS, vdd = 1.62V, temp = 85°C	3.04 V, 4.67 V	1.05 A	213 mA, 209 mA

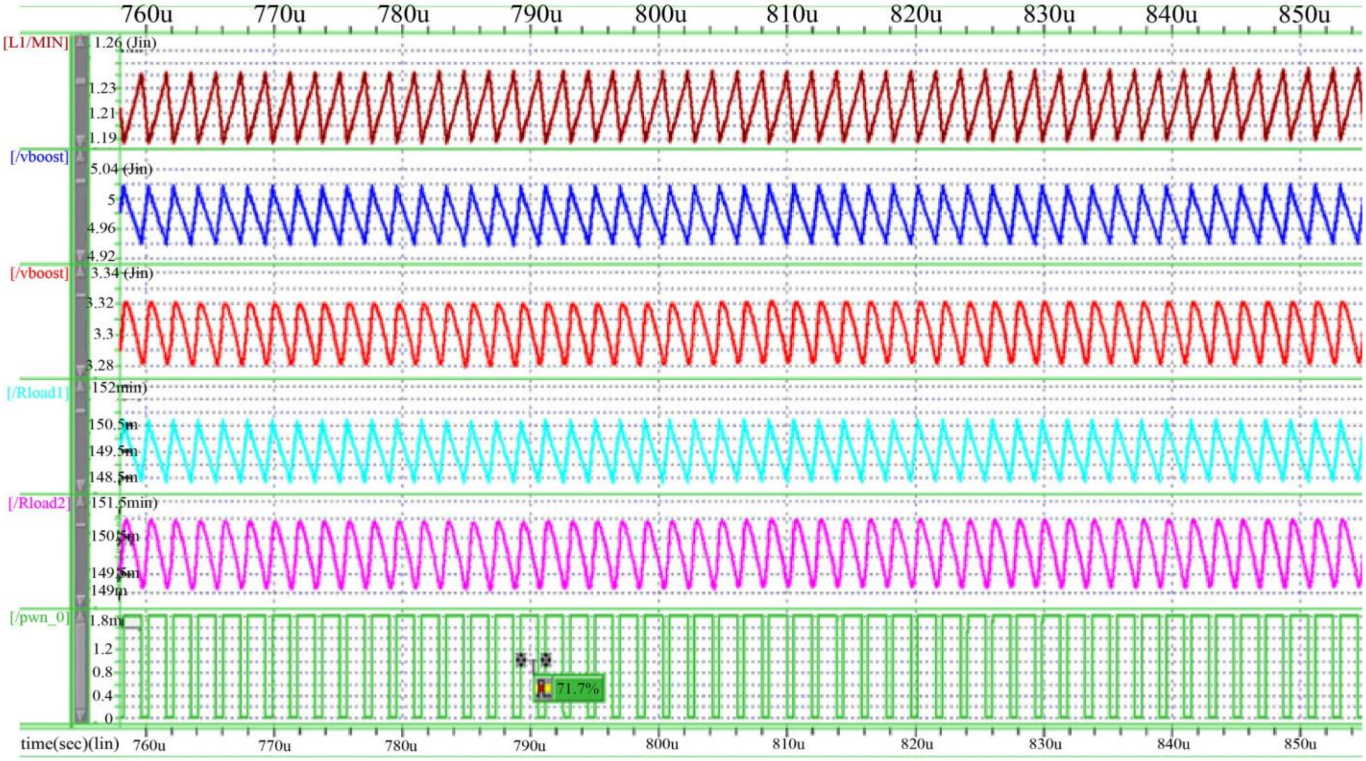

Fig. 9 Power stage simulation

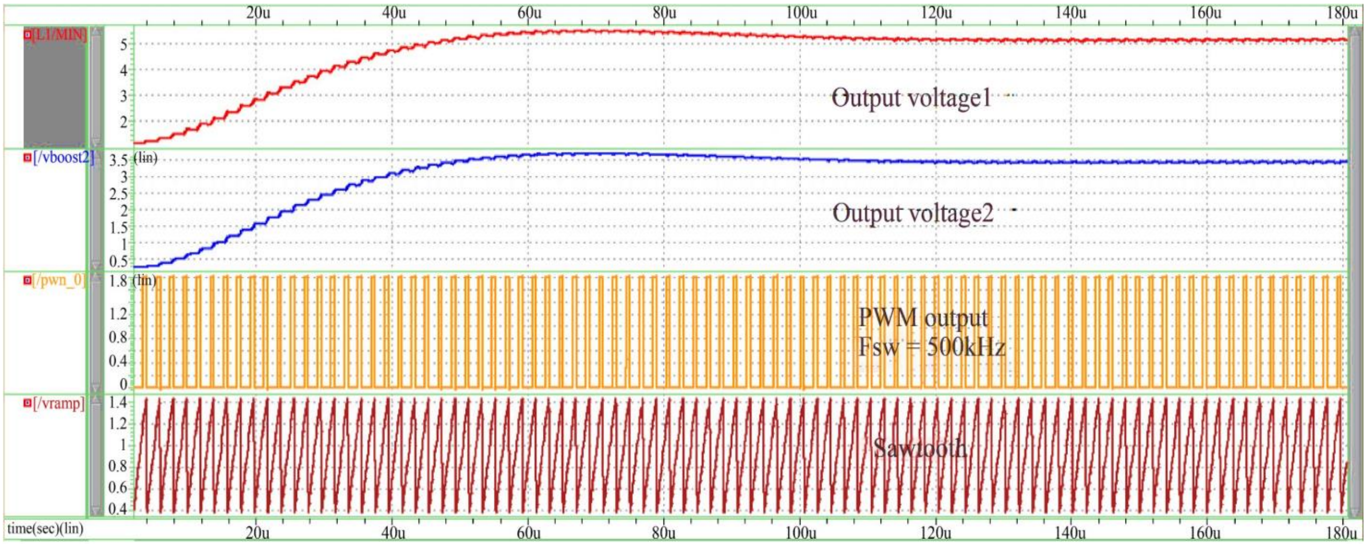

Fig. 10 PWM output

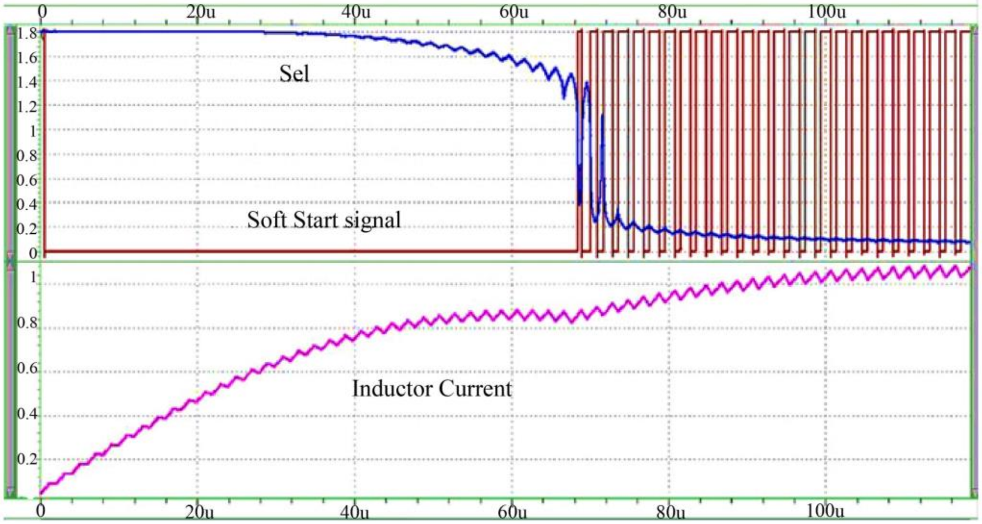

Fig. 11 Soft start output

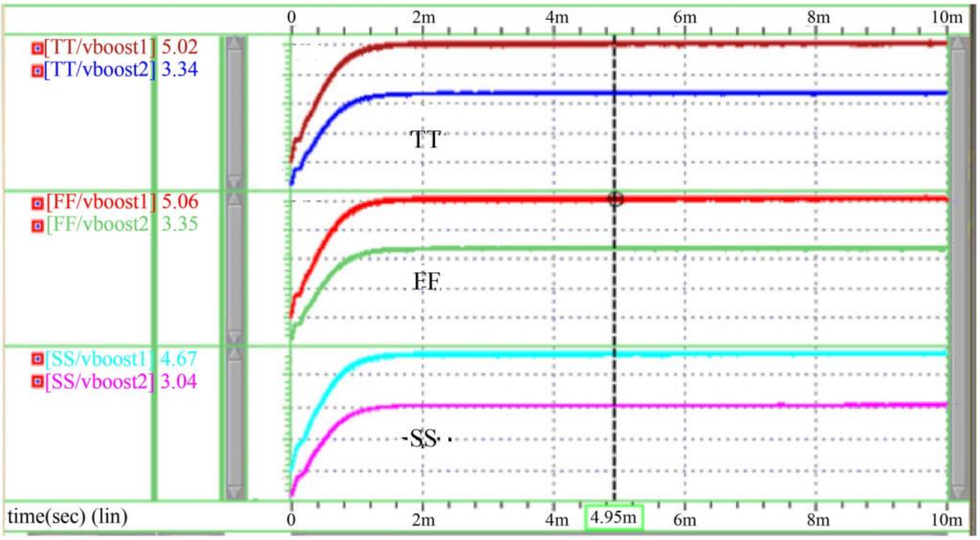

Fig. 12 Boosted outputs voltage with corners simulation

5. Discussion

The power stage simulation shows the behavior of the components using transient analysis. The designed boost converter steps up the input voltage of 1.8V to 5V and 3.3V. A type 3 compensation network was utilized to ensure the PWM circuit's stability and control. The (Verror) voltage error was subsequently compared with a 500kHz sawtooth wave signal to generate a steady frequency output. In the initial stage of the switching cycle, the PWM signal is at a low state, which enables the power of the PMOS switch. Upon the sawtooth ramp going beyond the Verror threshold voltage, the PWM goes to a high state, which turns off the power PMOS switch. In the course of heavy load conditions, the analog transient voltage Verror exceeds Vramp. Then, the soft start circuit generates a gradual decrease in the PWM signal to drive the power PMOS switch. The device operates slowly until it reaches the initial steady state. Soft start is integrated to avoid in-rush currents that occur in the input of power supplies. During the power-on, the design converter slowly increases the voltages in the non-inverting input of the error amplifier. The converter successfully boosts the desired output with minimal variations. The output of the inverted low pass filter is high during the soft start. The results were close to the input voltage, and the output voltage and inductor current slowly rose until the voltage output reached the desired voltages of 3.3 V and 5 V.

6. Conclusion

This paper presents a DC-DC boost converter single input dual output for wireless sensor network applications. The proposed design was a success since it achieved and met the desired specifications needed for the study. The boost converter successfully produces the 3.3 V and 5 V outputs for WSN applications. A soft start circuit was also employed in the circuit to protect the device from in-rush current, thus protecting the battery. The simulation results obtained a maximum efficiency of 83.4% at 200 mA load. The voltage ripple is also considered while designing the circuit, which yields a 3% for the pulse width modulation.

Acknowledgement

The researchers would like to express their gratitude to the Almighty God for the guidance and protection and hope to complete this research study. As researchers, they would like to extend their sincere thanks to the following: Center for Integrated Device Research (DOST-CIDR) for the licensed software and the Center for Renewable Energy, Automation and Fabrication Technologies (CSU-CRAFT) for assisting us with the venue for laboratory works. To the faculty, who give them insights and knowledge about the topic, and to the researcher's parents, who humbly provide financial assistance and support.

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