International Journal of Engineering Trends and Technology
ISSN: 2231–5381 / https://doi.org/10.14445/22315381/IJETT-V71I4P212
Volume 71 Issue 4, 128-139, April 2023

Review Article

Design and Implementation of C/A code Generation for SOC-based GNSS-SDR Applications

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Received: 16 November 2022 Revised: 27 March 2023 Accepted: 13 April 2023 Published: 25 April 2023

Abstract *- GNSS receivers may now be found in a variety of miniaturised platforms, chipsets, microprocessors, Integrated Chips (IC), DSPs, FPGAs, portable devices, and even the majority of mobile phones. This trend is expected to continue in the near future. In point of fact, GNSS receivers may run on a diverse range of platforms. This flexibility is achieved by a careful balancing act between a number of factors, including receiver performance, cost, power consumption, and battery life. In addition, the growing capabilities of microprocessors have made it possible for software receivers to emerge with performance comparable to that of implemented hardware receivers. This has provided certain user applications with the flexibility that is required for them to function properly. This work aims to demonstrate the GNSS software receiver architecture, which can receive all of the GNSS signals currently being received by the antenna at any given time. This article presents a discussion on the most recent developments in GNSS receiver designs. The primary block of GPS and GLONASS has been implemented in both Matlab as well as Xilinx Vivado tools.*

Keywords *- GNSS-SDR, SDR architectures, GPS, GLONASS, SoC.*

1. Introduction

In order to offer mobile operators a more efficient receiver, offering an increased quality of service, a new receiver will have to be designed to offer all navigation systems better location accuracy in all environments (urban, rural, and inside buildings). It then becomes necessary to locate mobile receivers very precisely everywhere in the world. The idea then is to define a multi-constellation receiver making it possible to receive the best signals coming from any satellite positioning system and to process them through the same interface without the need to change the equipment by moving from one place to another. In this paper, various state-of-the-art radio technologies are discussed and presented their interests and illustrate their fields of application for a long time.

Different navigation positioning systems exist; the Global Positioning System (GPS) is the oldest constellation which provides user position [1], which is an American system operational since 1994, followed by the GLONASS system (Global Orbiting Navigation Satellite System) [2], which is also an operational system but developed by Russians. Finally, the GALILEO system [3] is currently being deployed by Europeans. Other systems are also in preparation, especially in China BEIDOU [4]. The general principles implemented by these systems are similar. A notable difference resides in the difference in central frequencies with different bit rates and modulations.

The first thing to know is the specifications of existing Global Navigation Satellite System (GNSS) standards to analyze better and interpret the signal detected on reception. The specification of the GPS standard is discussed due to most of the research works carried out on the development of software-based GPS receivers. The GPS standard is the best-known satellite tracking system. It was designed in the early 1970s by the United States Department of Defense. GPS is originally made up of 24 functional satellites that continuously transmit on two different carrier frequencies, one called L1 (1575.42MHz) with a wavelength of 19.05 cm and the other L2 (1227.60MHz) with a wavelength of 24.45 cm. In practice, the configuration is spread over around thirty satellites in order to ensure optimal coverage over the entire globe. There are six circular orbital planes at an average altitude of 20200 km. Each orbit is inclined at approximately 55 degrees with respect to the equatorial plane and has 5 to 6 satellites. The GPS constellation provides visibility of five to eight satellites all over the earth. The GPS system's ground segment or control segment is defined by about ten stations installed and controlled by the US military. The satellites that make up the space segment communicate with the ground segment, which can apply the corrections (orbit, navigation message, etc.) necessary for the system's proper functioning in real-time. The control segment allows, among other things, the satellites to transmit their ephemerides with precision through the navigation message. The latter then uses the information of this message transmitted to a receiver to calculate its position [5].

The Global Positioning System (GPS) employs not one but two distinct varieties of pseudo-random number or PRN codes: the P code, which is utilized for the defence signal, and the C/A code, which can be used for the civilian signal. Sequences of these codes are a sequence of 1 and 0 bits. Each satellite is assigned two specific sequences: one military and one civilian. The civil sequence or C/A code (for Coarse Acquisition) is a binary information sequence or also called Pseudo-Random code (PRN), consisting of 1023 bits (or even chips). It is delivered with a chip rate of 1023 KHz (1.023 MHz) and a total sequence of a code length, therefore, lasting 1 ms. Each series of 1023 chips is unique for each satellite, making it possible to distinguish them by functioning as a satellite identifier. There are 32 sequences; these are gold codes whose orthogonality properties ensure sharing the same frequency band by following the multiplexing principle by Code Division Multiple Access (CDMA). The military sequence, or P. code, is actually a 7-day fraction of a unique code that lasts 266 days. Each week a given satellite is assigned a fraction of seven days of this code which it will transmit throughout the week. This fraction is changed randomly every week. It is, therefore, necessary to know the beginning of each sequence in order to use it [7].

The remaining satellite constellations, such as GLONASS, GALILEO and BEIDOU systems, have their own standards [8]. The satellite signals structure and modulation schemes vary based on the satellite constellation. The idea of receiving and processing all of these signals by the same receiver allows a significant improvement in terms of positioning accuracy and service availability. It is thus understood that developing a receiver capable of processing several constellations is essential. The development of low-power GNSS software receivers has a significant impact on a wide range of applications, including mobile devices, the Internet of Things (IoT), unmanned aerial vehicles (UAVs), and other battery-powered systems [9].

Despite the numerous benefits of low-power GNSS software receivers, several research gaps still need to be addressed. Here are some of the research gaps: While low-power GNSS software receivers are already energy-efficient, there is still room for improvement in terms of reducing power consumption. Research is needed to develop more efficient algorithms and techniques for power optimization that can reduce energy consumption without sacrificing performance. GNSS signals can be affected by various environmental factors, such as buildings, trees, and weather conditions, which can impact the accuracy and reliability of GNSS receivers. Research is needed to develop robust algorithms that can mitigate the effects of these environmental factors on low-power GNSS software receivers. Low-power GNSS software receivers can be integrated with other sensors, such as accelerometers and gyroscopes, to provide additional location information and improve accuracy. However, there is a need for research to explore the optimal ways of integrating these sensors to achieve maximum accuracy and efficiency. As the number of IoT devices and other low-power systems continues to grow, there is a need for low-power GNSS software receivers that can scale up to meet the demands of these systems. Research is needed to develop scalable algorithms and architectures that can handle the increasing volume of data generated by these devices. Low-power GNSS software receivers are susceptible to various security and privacy threats, such as jamming and spoofing. Research is needed to develop secure and privacy-preserving algorithms and techniques to protect low-power GNSS software receivers from these threats.

Overall, addressing these research gaps will help further improve the performance, reliability, and security of low-power GNSS software receivers and make them more suitable for various applications. In this paper, the state of art receiver architectures is discussed. The main motivation of this review work is to develop a reconfigurable and low-power GNSS correlator to meet the latest communication protocols. The major contribution of this research work is to develop a C/A code generation for both GPS and GLONASS systems. The paper is organised as follows: Section II provides the study of GNSS receiver designs, and Section III explains the C/A codes or PRN code generation for GPS and GLONASS satellite constellation systems. The corresponding findings are described in section IV.

2. Review of GNSS Receiver Architectures

In this section, a study is conducted on the architectures deployed to design GNSS receivers since their first appearance. We start with the classic architecture of a traditional GPS receiver. We then detail the emerging architectures to get an idea of the architecture to choose to design our low-power receiver towards the end.

2.1.Traditional GPS Receiver Architecture

In order to present new approaches to signal processing used in modern GNSS receivers, it is necessary to present the old architecture of traditional GPS receivers and understand its functionalities. The first version of the GPS receiver is a sequential receiver that uses the sequential processing technique (one sample at a time). While the new versions exploit the Software Defined Radio (SDR) architecture and provide digital signal processing. The signal processing is carried out at the DSP (Digital Signal Processing) level by algorithms.

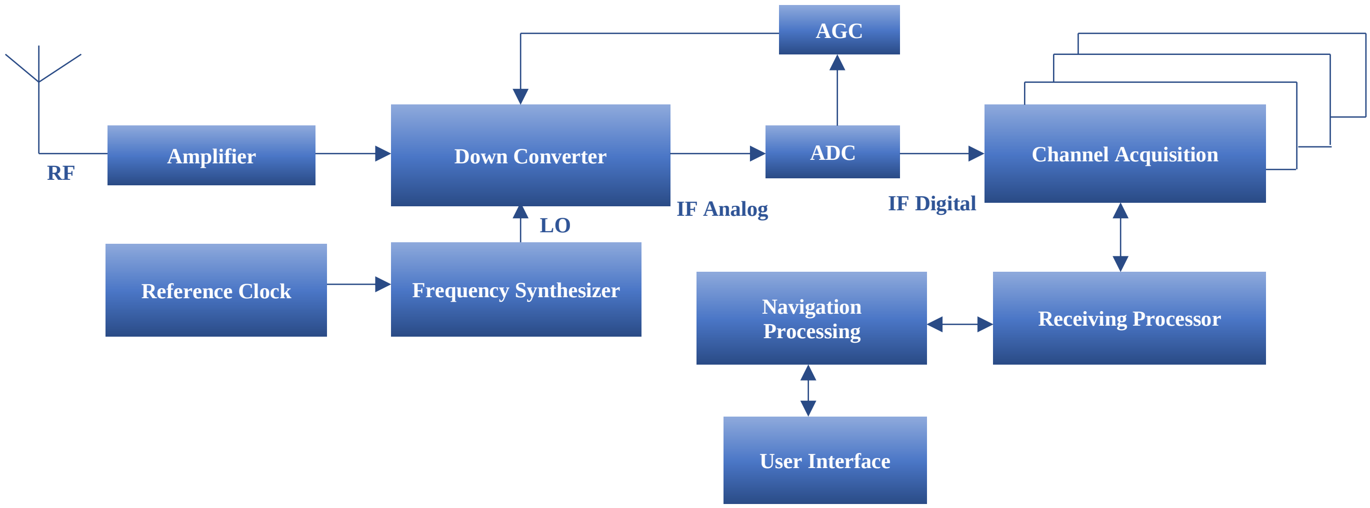

Fig. 1 Basic GPS receiver Architecture

The three primary components of the receiver are shown in Figure 1. These components include the first RF section, which comprises an antenna, amplification circuits, Analog to Digital Converter, also known as ADC and frequency-synthesiser. The second section consists of the channel acquisition stage of the various satellites. The last part includes the tracking and navigation processing block [10].more details for better visibility on the implementation of the RF stage of a GPS receiver.

2.1.1. RF Frontend

The antenna receives the RF signal from the GNSS satellites. Depending on the type of antenna, it can pick up only the L1 signal or both L1 and L2 signals together. The received RF signal level is very low. The pre-amplification stage amplifies this signal without degrading its SNR value. The presence of bandpass filters at this stage is necessary to reject RF interference outside the passband [11]. These filters can be broadband covering the carrier frequencies L1 and L2, or else selective with dual bands. The choice of these filters varies on the different applications. Before the frequency transposition can take place, the picture frequencies must be removed from the signal, and this requires the use of at least one filter. The amplified and filtered RF signals are down-sampled into IF to the product by a pure sine wave coming from the Local Oscillator (LO). This sine wave is generated by a frequency synthesizer driven by the reference clock.

The analog IF signal is digitized by sampling, whose rate is determined according to the frequency band of this signal. This rate varies in the different receivers according to the way of the prior filtering of the RF signal. However, typical sampling rates vary between 4 to 10 MHz, For processing the main lobe of the PRN code, whose bandwidth is 2.046 MHz. The necessary sampling rate will be at least 4.092 MHz, according to Shannon's theorem [12,13]. Quantization of the GPS signal takes no more than three bits to sample. However, a single bit is sufficient for low-cost commercial receivers, while one to three bits are generally used for receivers with heavier applications [14]. For more than one quantization bit, an Automatic Gain Controller (AGC) is needed to optimize the input range of the ADC converter. A single-bit scan, which a voltage comparator can realize, simplifies the RF module's architecture because the signal is clipped. In [16]. Akos gives us

2.1.2. Tracking Loops

When an initial, less precise gathering of the GPS signal has been finished, the tracking process of the GPS receiver will begin in the digital component of the device. Both the code and carrier tracking loops work together to improve the measurements of the carrier and code phases, respectively. In the case of significant and sudden changes in these values, the tracking process fails, resulting in a loop dropout. This will require pre-acquisition, or a restart, in order to re-evaluate the updated phase shifts. The design of the tracking loop is conducted in detail in [11, 17].

Microprocessors and digital signal processors (DSPs) are often the components responsible for carrying out code and tracking loops. These devices are also in charge of managing the code and carrier NCOs in their respective networks. While the code loop is typically a delay-locked loop (DLL), the carrier loop is frequently a phase-locked loop (PLL). There is a possibility that the code loop is also a frequency-locked loop (FLL)

2.2. Emergence of new GNSS Receivers

The growing capabilities of microprocessors have made it possible for software radio receivers of the SDR type to emerge. These receivers have performance comparable to that of hardware receivers that have been implemented, and they provide the flexibility required for certain user applications. As a result of the development of regional and worldwide multiple satellite navigation systems, multi-constellation receivers are rapidly becoming the focus of research.

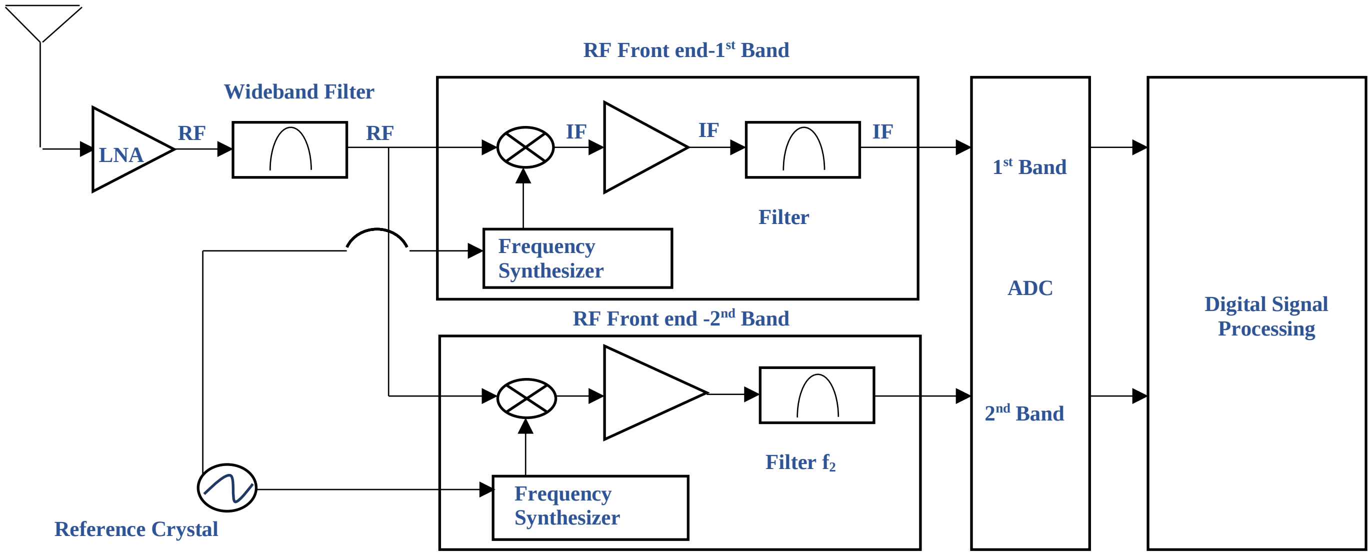

Fig. 2 Super heterodyne architecture of a multiband receiver [20]

This is in consideration of future developments. At the system design level, this has been actively supported with the goals of achieving interoperability and compatibility. By considering selective degradations of services, GPS systems allow localization precisions of the order of 5 to 10 m. The major interest of a multi-standard positioning system is to be able to reduce location error by increasing the accuracy rate. In research article [18] shows us how processing GPS and Galileo signals together can increase the accuracy rate.

In recent years, several research works aimed to find an optimized architecture for a multi-standard receiver. The first classical architectures used are the homodyne, heterodyne and super-heterodyne architectures. In the literature, several works have been validated by exploiting these architectures.

In [20], the super-heterodyne architecture allows each signal to be converted using a Local Oscillator (LO) before sampling. This architecture requires an RF stage for each new signal introduced in a different band. Figure 2 illustrates this super-heterodyne architecture for two distinct bands of GNSS signals. Adding another band adds another RF stage. Therefore the design complexity will increase by introducing more signal bands. To remedy this problem, [20] proposes to work with the Direct RF Sampling (DRFS) architecture. The frequency schemes for the DRFS design proposed in [23] are as follows: G1 will have a band that extends from 1.5 GHz to 1.6 GHz, which will cover a bandwidth of 50.54 MHz; G2 will have a band that extends from 1.1 GHz to 1.2 GHz, which will have a band that extends 131.76 MHz. Working with GPS signals centred at 1.575 GHz and having a sampling frequency of 300 MHz allowed this design to be verified for use in the GI band.

For a dual-band GPS L1 / GALILEO E1 GNSS receiver, a Low IF type design was developed in [21]. This architecture makes it feasible to transpose the carrier frequency, which is centred at 1575.42 MHz, to a fixed low intermediate frequency of 20.42 MHz. The problem encountered in this architecture is the DC-offset problem. As the energy of the GPS signal C/A codes is in DC, which adds noticeable noise, sometimes can eliminate and destroy the useful signal and consider it noise. The problem of selecting fixed frequencies prevents the introduction of new bands and is limited to the double L1/E1 bands. In the proposed receiver, the L1/El signals picked up by an antenna are of low amplitude; they are first amplified and then filtered by a SAW filter (Selective Acoustic Waves) which provides image rejection greater than 40 dB. The filtered signals are converted into fixed IF equal to 20.42 MHz by using a local oscillator. The analog IF signals are then converted to a baseband with an ADC of sampling frequency equal to 16.638 MHz and of resolution 1 bit, as indicated in Figure 3. The biggest disadvantage of this architecture is the major use of analog components (mixer and oscillator), which complicates the design of a GNSS receiver with more than two bands.

A multiband receiver based on this architecture needs to add other mixers and an LO, explaining an increase in energy consumption and massive use of the chip area. Another solution, as indicated in [21], makes it possible to remedy this problem of extension of the other GPS and GALILEO signals in the L5 and E5a bands. It would be adding a two-input switch to switch between bands and use two antennas. The first is to pick up signals from the L1/E1 band, and the second is to receive signals from the L5/E5a band. Figure 4 shows the Low IF architecture for receiving both L1/E1 and L5/E5a bands.

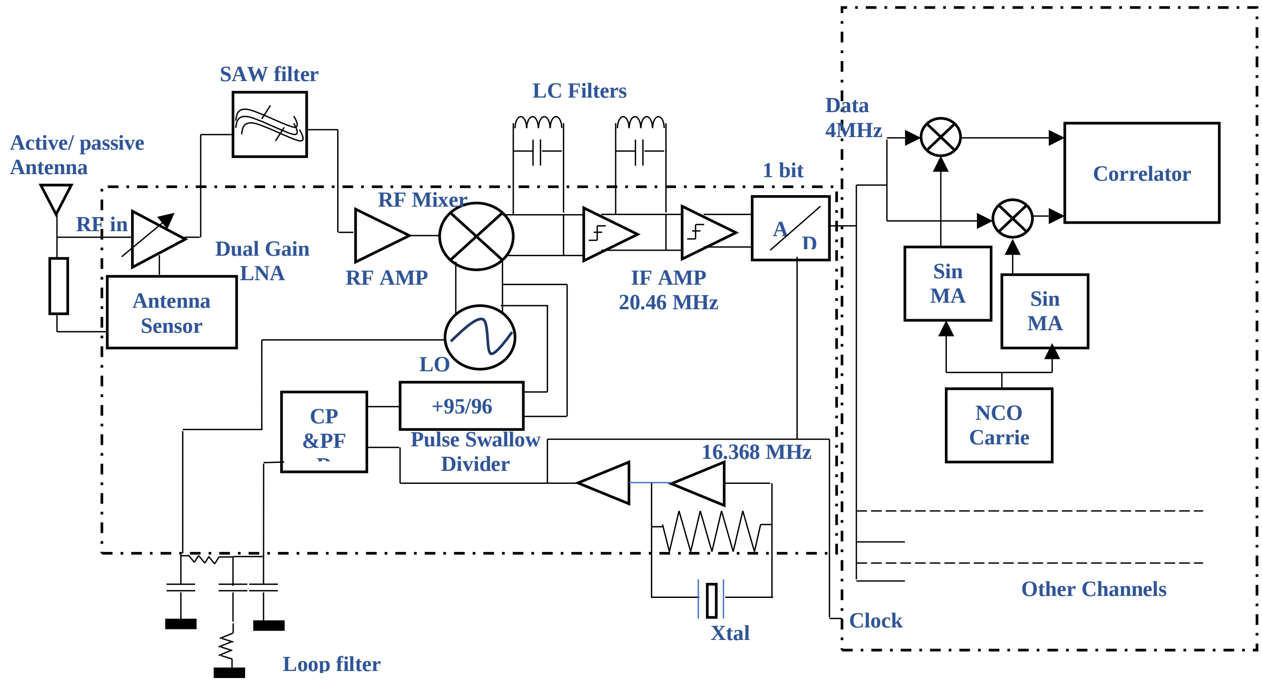

Fig. 3 GPS L1/GALILEO E1 pro-Dual Band Low IF Receiver posed in [21]

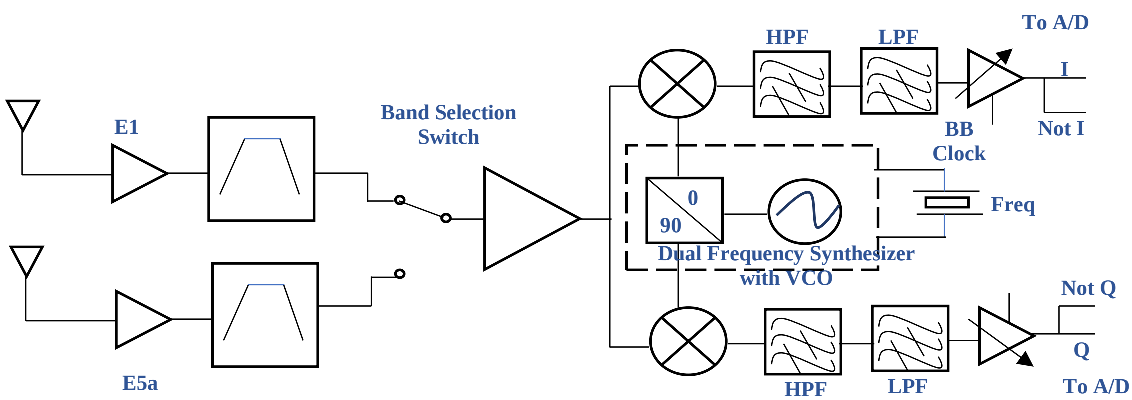

Fig. 4 GPS / GALILEO Multiband Receiver (L1/El and L5/E5a) in [22]

When the band selector switch has been used to pick the signal band, an acquisition stage is then set up to convert the RF signals into analogue intermediate frequencies using a LO. This process occurs after the band has been chosen. The L1/E1 band signals are converted from 1575.42 MHz to 5.67 MHz, and the L5/E5a band signals centered at (1175.45 MHz)/(119.15 MHz), respectively, are converted to 3.2 MHz.

In [23], a receiver using the low IF architecture is presented. It captures all bands of GPS, GALILEO and BEIDOU standards. This receiver, presented in Figure 5, is composed of two independent stages for the simultaneous reception of signals. Each channel is clocked by a local oscillator having a bandwidth covering the RF bands of the three standards. This architecture provides another local oscillator to clock the ADC and AGC. The disadvantages of this proposal are identic to those of the classic Low IF architecture.

Moreover, it has a higher energy consumption following the use of several local oscillators to generate the clock signals of the various components of the chain. The receiver presented in [24] processes the lower Band signals 1.2 GHz or the Upper Band 1.6 MHz from the four standards GPS, GLONASS, GALILEO and BEIDOU. Figure 6 shows two RF frontends built into this receiver. Two channels for digital processing with two fixed frequencies at 15.902 MHz and 15.48 MHz are offered for lower and upper bands, respectively. Two frequency synthesizers FS1 and FS2, are used in the proposed receiver [24]; they provide a wide band which exceeds 1.4 GHz, which covers the entire RF band. A switch is used to switch between the bands and link the two RF stages and the two channels.

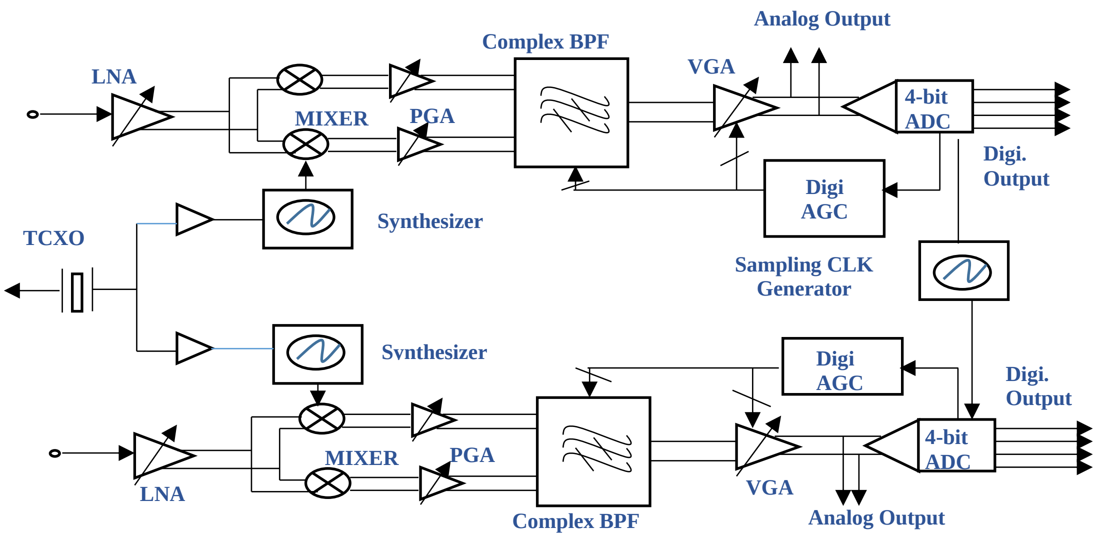

Fig. 5 GNSS receiver in [23]

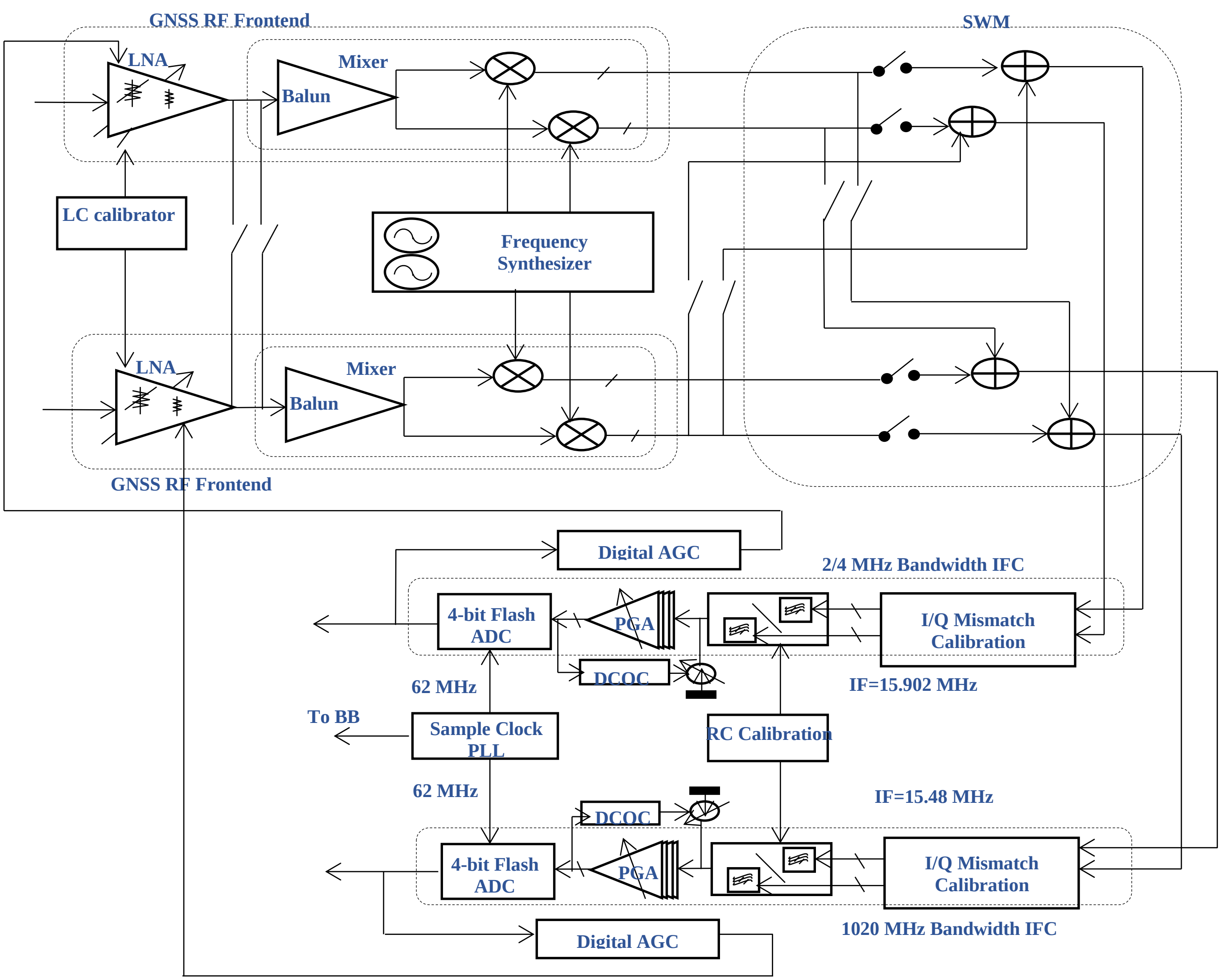

Fig. 6 Low IF receiver proposed in [24].

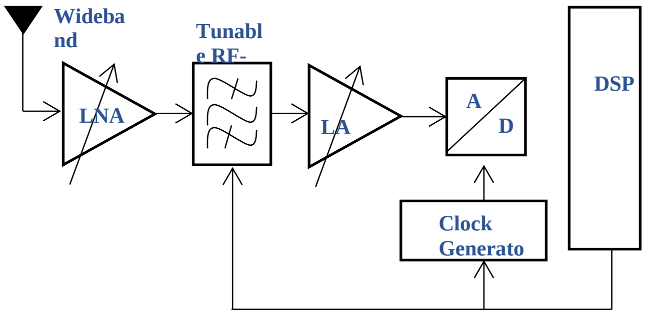

Fig. 7 Architecture of a subsampling GNSS receiver [24]

The most widespread architectures in the design of satellite positioning receivers are the heterodyne and low IF architectures; these architectures include analog components (mixer, local oscillator, filter, etc.). Signal processing through these receivers is done largely in the analog domain, and only a small portion is done in digital, which complicates receiver design and results in increased area and power consumption. Some research articles proposed an alternative to the RF sub-sampling architecture to compensate for this problem. Then latter, a Software Defined Radio (SDR) type architecture was introduced. The SDR offers versatility and flexibility in the design of the reconfigurable receiver and makes it possible to advance the digital processing as close as possible to the antenna.

2.3. Down-sampling GNSS RF architectures

For RF subsampling receivers, a few architectures are proposed [25,26]. In [25], a reconfigurable SDR receiver is described. This receiver is equipped with a broadband antenna for picking up signals from the RF bands, followed by an amplifier for boosting the weak signal strength picked up at the antenna's output (the level of the SNR is estimated at -26.83 dB). The receiver in Figure 7 uses a variable frequency generator to manage the ADC and the filter, whose frequency is reconfigurable. This generator makes it possible to adjust the frequency at the level of the ADC as well as at the level of the filter. For analog-to-digital conversion, a sigma-delta (∑Δ) modulator is used. A solution is proposed to relax the topology and attenuate the interference of adjacent bands by CT ∑Δ-ADC.

In [20], as discussed before, a comparison between classical architecture and direct sampling architecture is explained. Then the interest in a new DRFS architecture is proposed as an alternative and presented in Figure 8.

An ADC digital circuit integrated into the Field Programmable Gate Array (FPGA) ensures the intermediate frequency conversion. For this approach, a critical choice for the sampling frequencies is requested. A frequency of 300 MHz is required in order to be able to sample signals in the L1 band. The frequency of 1080 MHz is estimated to sample all signals of different bands.

The receiver presented in [26] is a proposed RF subsampling receiver. It is designed to receive GPS and GLONASS, and GALILEO signals. As shown in the block diagram of the architecture of this receiver in Figure 9, the GNSS signals picked up by an antenna have low levels, so a block of amplification circuits is placed after the antenna to amplify these levels. After that, a variable gain amplifier is inserted there so that the signal level may be adjusted and controlled.

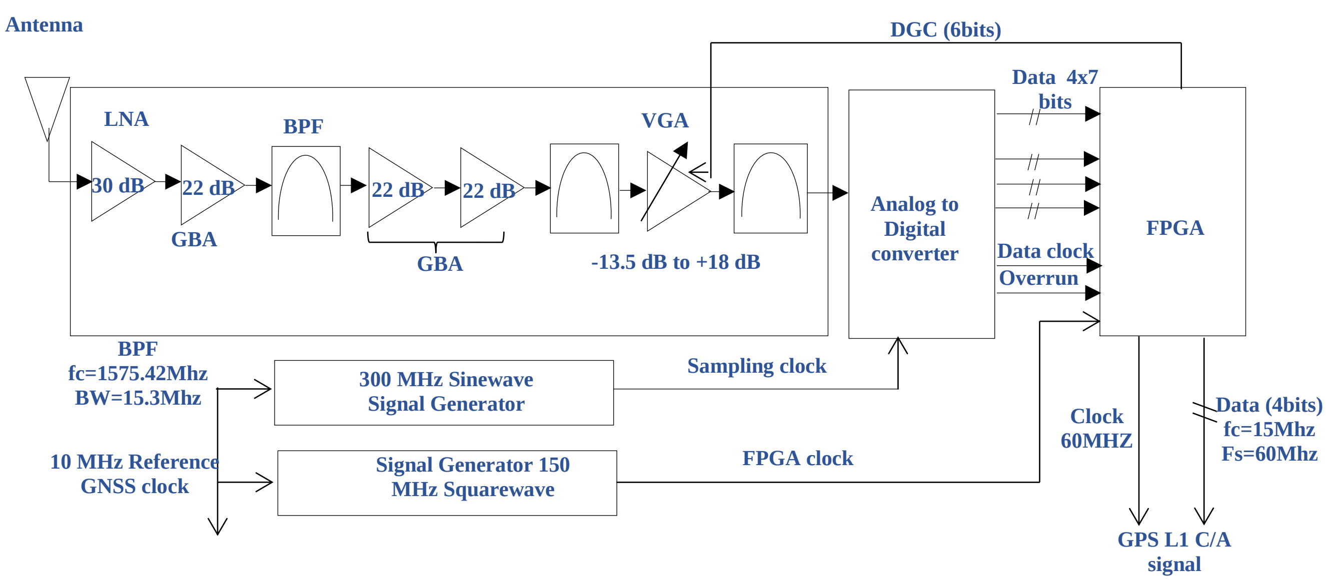

Fig. 8 The RF subsampling architecture in [18]

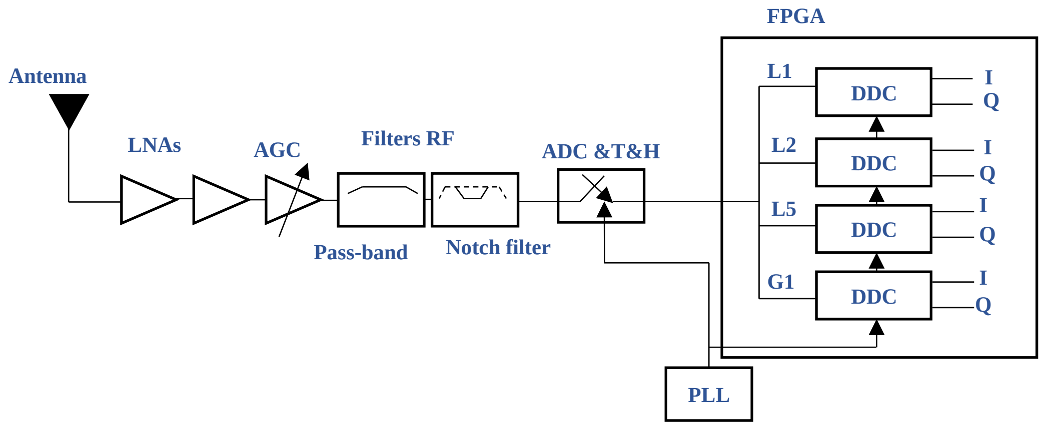

Fig. 9 GNSS receiver in [25]

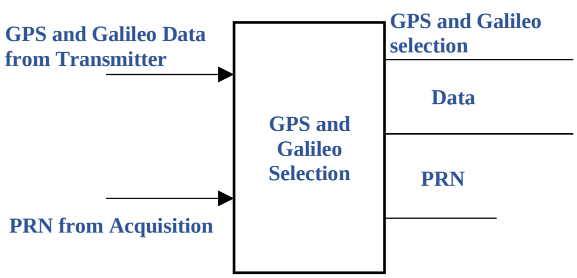

Fig. 10 Controller of Reconfigurable Architecture

After that, a series of filters are positioned to choose relevant signals and attenuate defects of bands near each other. We make use of an ADC that comes equipped with its own sample and hold circuit. The sampling frequency is fixed equal to 247.566 MHz to convert these signals into intermediate frequencies. A Digital Down Converter (DDC) circuit is placed for baseband conversion.

The GPS L1 C/A signal and the Galileo E1 signal will both use the same radio interface if this option is used. In addition, in order to demodulate the navigation message, a control block is added. This block, seen in Figure 10, allows for the differentiation between the GPS and Galileo signals to develop the hardware design for the GPS L1 C/A code tracking and signal tracking block and the Galileo E1 receiver, Xilinx ISE Design hardware, is used [26].

An investigation into the effects of a variety of narrowband interference (NBI) profiles on GPS LI C/A and Galileo E1 is presented in [27]. This investigation was carried out with the intention of improving signal quality, and it was successful because satellite signals reach the earth at relatively low power. Hence, the receivers used in navigation systems are particularly susceptible to the many forms of radio interference that might occur. It is consequently vital to develop corrective measures for the NBI, and the adaptive filtering approach has been investigated extensively to centralise the NBI. This method is able to determine the characteristics of any frequency band that has interference.

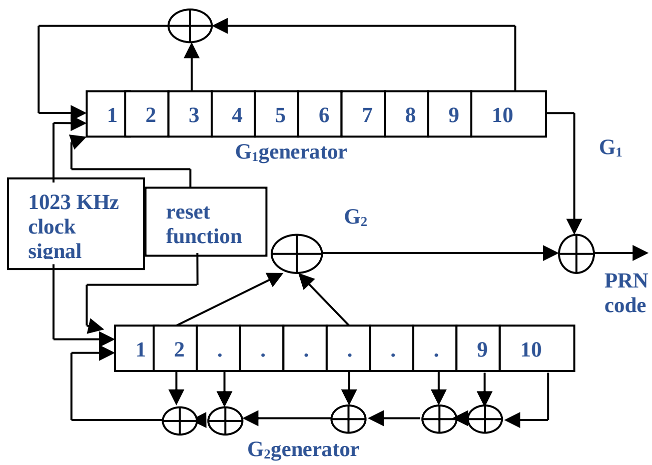

Fig. 11 PRN signal or C/A code generation of GPS system

3. Preliminary Development: GNSS C/A Code Generation

The procedure for generating C/A codes for the GPS and GLONASS satellite constellation is broken down and detailed in this section. First, the C/A code creation for the GPS system, which has a total of 32 satellites, is carried out, followed by the development of the C/A code generation for GLONASS.

3.1.Generation C/A codes for GPS system

The generation of the C/A codes comes under the gold code family, which can be seen in Figure 11. This generator consists of two Linear Feedback Shift Register (LFSR) called G_1 and G_2; these LFSR can generate a sequence of maximum length $N = 2^n - 1$ elements, in which n is equal to 10, giving rise to a maximum length of 1023 chips. The generated sequence is the result of the modulo-2 sum of a certain combination of the states of the two LFSRs.

In every 1023 chips, two LFSRs are reset by passing all their states to a value of 1, causing the code to start over. The feedback of the first LFSR, G_1, always has the configuration corresponding to the polynomial expression represented in equation (1).

$$f(x) = 1 + x^3 + x^{10} \quad (1)$$

This indicates that states 3 and 10 are transmitted back to the LFSR's input. Similarly, the LFSR G2 represents polynomial expressions as equations (2).

$$f(x) = 1 + x^2 + x^3 + x^6 + x^8 + x^9 + x^{10} \quad (2)$$

The generation of the different C/A codes of each satellite is done bit by bit as the modulo-2 sum of G_1 and G2. This modulo-2 sum is the combination of the G_1 output itself together with a combination of G_2 states unique to each satellite. This selection of states in G_2 is called phase selection. For example, to create the SV1 C/A code, the output of G_1 will be combined with states 2 and 6 of G_2.

3.2.Generation C/A codes for GLONASS System

In GLONASS C/A code generation, a nine-step shift register generates the sequence. The polynomial generator $G(x) = 1 + x^5 + x^9$ characterises the 9-step shift register. The code is timed at 511 kHz, which results in a repetition period of 1 millisecond. Unlike GPS, which gives each satellite a unique sequence, this system assigns each satellite the same sequence. All GLONASS satellites use the same code. The C/A code is modulated using Frequency Division Multiple Access (FDMA) because the receiver can discern the difference between signals coming from different satellites depending on the frequency allocated to each satellite. Each GLONASS satellite broadcasts the P code in the L1 and L2 bands, but the C/A code is exclusively sent in the G1 band. For each frequency band L, a channel is allotted to each satellite. The values of the central frequencies of the different channels are determined using equations (3) and (4): With n the channel frequency number (n 0. 1. 2 etc...).

$$G_1 = 1602\ MHz + (n \times 0.5625)MHz \quad (3)$$

$$G_1 = 1246\ MHz + (n \times 0.4375)MHz \quad (4)$$

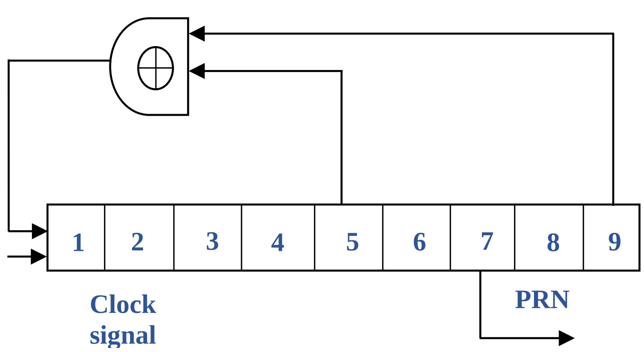

Fig. 12 PRN code or C/A code generator of GLONASS

The GLONASS C/A code generation block diagram is shown in Figure 12. GLONASS satellites are different compared to GPS satellites in that each GLONASS satellite transmits the same code for different frequencies. This means that GLONASS satellites transmit signals on their own frequency bands, and the center frequency of each of these bands is separated from the adjacent channel by 562.5 KHz in the L1 band and 437.5 KHz for the L2 band.

4. Simulation Results and Discussion

This section discusses the simulation results of C/A code generation of GPS and GLONASS systems. MATLAB and Verilog are the two programming languages used to generate PRN codes for GPS and GLONASS. The 32 satellites of the GPS PRN codes which generated by changing the phase points. Each set of 1023 chips is referred to as a C/A code and varies depending on the GPS satellite used. C/A codes are created by GPS satellites and have a chip rate of 1023 per millisecond at a clock rate of 1023 kilobits per second. The generation of the PRN code by GPS-SV6 with 1023 chips/ms is shown in Figure 13.

MATLAB was used to build 1023 chips of the GPS PRN code, as depicted in Fig.13. In GPS receivers, a GPS PRN code is referred to as a sequence of binary chips used to determine the receiver's location with an exceptionally high degree of accuracy. The code is a binary sequence that is 1023 chips long and has a chip rate of 1.023 MHz. The length of the code is 1023 chips. The binary sequence of 0s and 1s that serves as a representation of the PRN code was generated through the help of MATLAB. As a direct consequence, a total of 1023 chips that constitute the PRN code for the GPS were generated. This sequence is going to repeat itself after every 1023 chips, and each chip in the sequence will correspond to a single bit in the code.

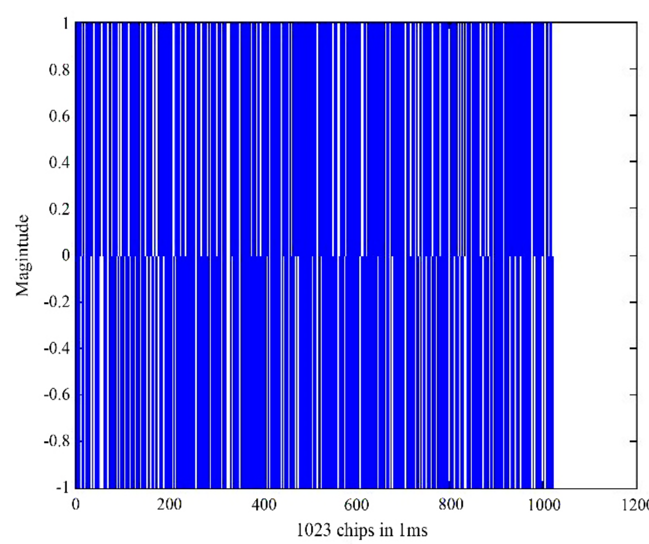

Fig. 13 The generation of GPS C/A codes for SV6

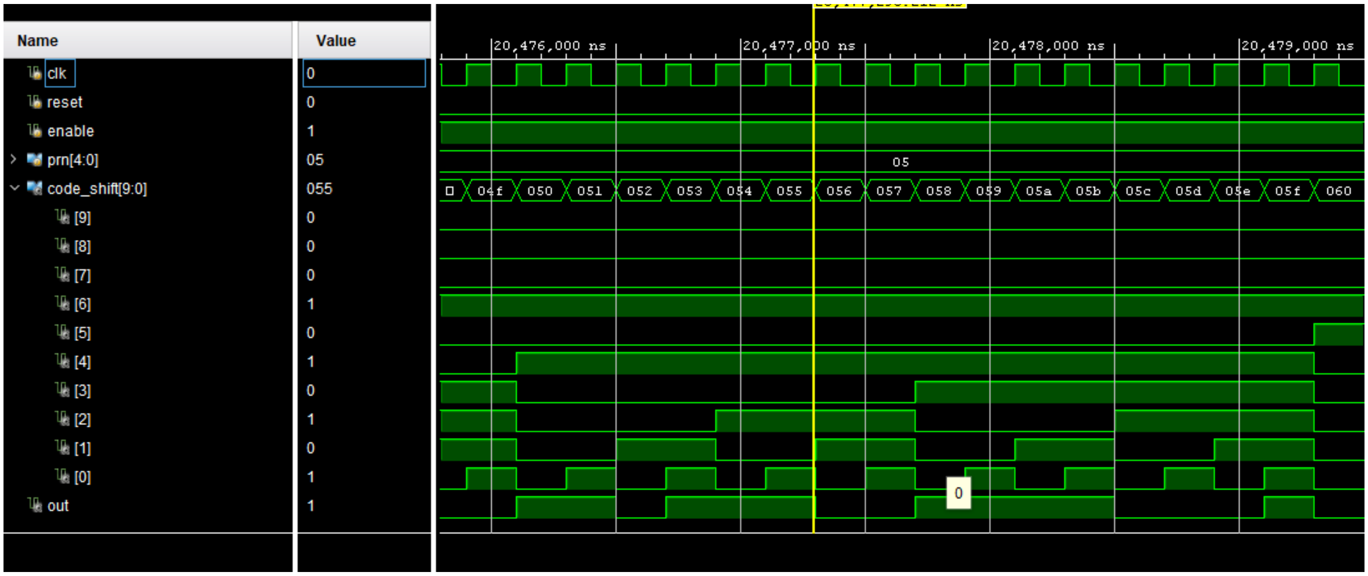

Fig. 14 GPS SV6 C/A code generation using the Xilinx Vivado tool

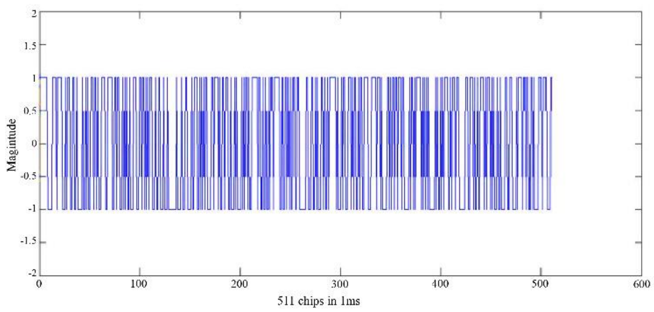

Fig. 15 Matlab results of GLONASS C/A code for 511 chips

Spread-spectrum signals are created when the PRN code is modulated into a GPS carrier signal to produce them. These signals are then delivered by GPS satellites. GPS receivers make use of the PRN code, which synchronises with the GPS signal which is being transmitted by the GPS satellites. This can be done to measure the time difference between the satellite-transmitted signal and the signal received by the receiver. This time can be known as the acquisition time. This time delay may then be used to calculate the distance between the receiver and the satellite, which is then used to identify the receiver's location. In other words, the time delay is utilised to determine the distance between the receiver and the satellite. Figure 14 illustrates the matching C/A code sequence produced by the same GPS SV-6 C/A code generation included in the Xilinx Vivado tool. This sequence was created in order to match one another.

In Figure 14, prn indicates the selection of a GPS satellite and code_shift net indicates the shifting of the C/A code based on the gold code polynomial expressions mentioned in equations (1) and (2). The corresponding C/A code is stored in the out net variable.

The GLONASS system makes use of something called a maximum length sequence, which may be thought of as a kind of pseudo-random binary sequence. This sequence is created using an m-stage shift register that uses linear feedback. An m-stage shift register will create a sequence with a length that is 2m -1 when the maximum length sequence mode is selected. In the case of the GLONASS range code, the shift register includes nine phases, which results in the generation of a 511-bit sequence ($2^9 - 1 = 511$). Figure 15 displays the results obtained from running the GLONASS C/A code LFSR in MATLAB.

This C/A code is transmitted in different frequency components to identify the satellite numbers. Similarly, the LFSR of GLONASS PRN or C/A code is generated in the Xilinx Vivado tool using the Verilog programming language, and corresponding results are shown in Figure 16.

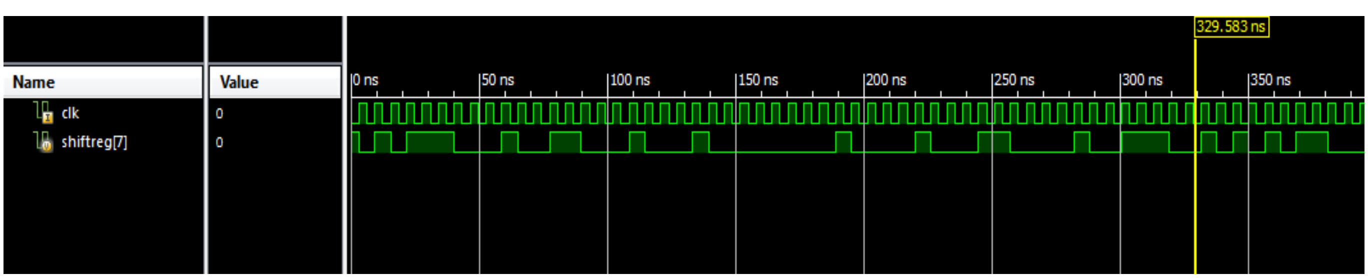

Fig. 16 511 chips of GLONASS C/A code implemented in Xilinx Vivado

Table 1. FPGA Resource Utilization comparison

Parameter	GPS [28]	GLONASS [28]	Proposed GPS	Proposed GLONASS
Slice LUTs	26	19	17	5
Slice Registers	46	32	21	11
Dynamic Power (W)	0.672	0.251	0.354	0.103

The correlation is carried out during the acquisition process, which means that the incoming signal is multiplied by the PRN code that was created locally. The digitised IF signal is multiplied with PRN code (locally generated) that has code phase 0 to 511 chips while performing the parallel code phase search acquisition. After the multiplication operation, the generated signal is subjected to a Fourier transform to be converted into the frequency domain. In conclusion, the modulo square operation is carried out to see the correlation findings. Further, the proposed GPS and GLONASS C/A code generations are ported on the Xilinx Zynq SoC board for real-time validation. The resource utilization of the proposed C/A code generation is compared with research work reported in [28]. The comparisons of the resource utilization report are shown in Table.1

As compared to research work reported in [28], the proposed technique produces superior results in terms of the number of Slice LUTs and Slice Registers, as well as the dynamic power consumption of the system. These findings are shown in Table.1. In addition to this, the proposed technique is evaluated in terms of Slice LUTs, Slice Registers, and dynamic power usage and compared to previously published work. In this instance, the proposed technique consumes 50% less dynamic power compared research work proposed in [28].

5. Conclusion

This paper discusses an analysis of the architectures of GNSS receivers from previous works. State-of-the-art GNSS architectures, their advantages and their disadvantages lead the end to propose low-power GNSS RF architecture are discussed. This review paper's major interest is defining an optimized architecture of an SDR-type. GNSS receiver comprising an integrable and reconfigurable. RF stage and a digital processing stage with a software implementation of baseband processing. In MATLAB and Xilinx environments, preliminary work is being done to generate C/A codes for the GPS and GLONASS.

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