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Original Article

Modelling and Design of Antenna Amplifier using an Active Loaded Differential Pair

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Abstract *- The following research paper forms the application of the Double-Gate (DG) MOSFET in High-Frequency (HF) applications, namely differential antenna design. The following design, implementation, and testing are based around the DG MOSFET and improve shortcomings previously exposed in literature, i.e., low input impedance, low output impedance, and poor gain values. Improvements in current supply and design considerations were made to improve low-noise signal integrity. The differential antenna amplifier provides a low noise spectral density of 188 pV/$\sqrt{Hz}$, with a flat-band response of 17 dB for a bandwidth of 40 MHz. The power efficiency of the antenna amplifier is 98 %.*

Keywords *- MOSFET, Double-Gate MOSFET, Differential amplifier, Microelectronics, Nanotechnology, VLSI.*

1. Introduction

Radio Frequency (RF) design and engineering and wireless communications have grown exponentially recently. The need for the expansion of cellular and wireless communications infrastructure has prompted the need for this development. This need stems from technological advancements, highlighted by the Fourth Industrial Revolution (4IR) and the Internet of Things (IoT) [1]. The exchange of media and data through devices has accelerated the development of directional antennas at base stations between mobile devices [2, 3]. All forms of RF signals are being used today, from LF (Low Frequency) (30 kHz – 300 kHz) signals in AM (amplitude modulation), used in aircraft communications to HF (High Frequency) signals (3MHz – 30 MHz) are used in military communications and are regarded as the most densely populated frequency bands. Ionospheric propagation catalyses long-distance communications, making HF viable and important [4].

From this, to propel further research and analyses into HF, one may consider the Double-Gate (DG) MOSFET in applications of HF to Ultra-HF [5, 6]. *Sood et al.* [7-9] have realised the DG MOSFET's S-Parameters and power gain and have concluded that the DG MOSFET is suitable for HF application. *Pillay and Srivastava* [10, 11] have described other application-based advantages over current planar single-gate (SG) MOSFETs, which include high noise immunity, improved gain, and Common-Mode Rejection Ratio (CMRR) in class AB amplifier and differential amplifier design. This work is a revision and improvement of work done by *Pakaree and Srivastava* [12], where the resistive-loaded differential amplifier was designed using the DG MOSFET. Improvements made by *Pillay and Srivastava* [10, 11, 13] included the addition of a current mirror and its NMOS current sources and reducing a differential output to a single-ended one. Using the differential topology, it has been shown that the noise and electrical interference can be reduced, given that the input signal is split among two input-signal transistors.

The differential topology was designed and tested by *Karpagam and Sampath* [14] in the design of a differential low-noise amplifier (LNA). The differential LNA design exhibited a high signal-to-noise ratio (SNR) of 68.109 and a gain of 27 dB. A high gain can still be achieved in these applications, given that a single-ended output is used.

A differential receiver for transient electromagnetic (TEM) systems were designed by *Wang et al.* [15], where the noise floor of TEM systems was reduced, given the use of the differential topology and a tail current source.

Following the work done by authors[10, 11, 13], important areas have been identified in antenna amplifier design, allowing one to characterise and improve current design philosophies by testing various other parameters such as S-Parameters, output noise, and matching-circuit capabilities. The active-loaded differential topology has been prototyped by *Pillay and Srivastava* [12] and shown to exhibit an improved CMRR and low-power capability compared to cited works. The active loading of the differential amplifier is given by adding further DG MOSFETs, used as current sources in unison with a current mirror.

Assessing the viability of the DG MOSFET operating at HF is pivotal in antenna design, as it preserves signal integrity, reduces noise, and offers performance using less power [16-18]. Most SG MOSFETs indicate higher V_{CB}, -$V_{CE,}$ and power dissipation than the DG MOSFET designed [40]. Due to the use of two gates of the DG MOSFET, authors vary the allowable signal level and bias the MOSFETs DC level independently.

In this research work, the authors have aimed to investigate the application of the differential topology and its active loading principles [13] in antenna amplifier design, where the antenna amplifier can form the input stage of a receiver or transceiver. As noted by *Varshney and Sharma* [20], ZigBee transceiver systems require low-power consumption, for low data rates supported by a wireless network, given its use in battery-powered applications. The application of the active-loaded differential antenna amplifier in this work will provide insight into the active-loaded differential amplifier designed by [10], mainly determining its behaviour at high frequency and maintaining a low current consumption. A comparative analysis will be completed against current receiver systems designed for various frequency spectrums. This will allow the antenna amplifier in this work to be compared to other applications and their frequency and power analysis and provide advantages and disadvantages of each. Performing this comparative analysis will also allow the DG MOSFET to be compared to the SG MOSFET and other CMOS technologies.

Section 2 of this research highlights the functional specifications of the designed antenna amplifier, and Section 3 highlights the design methodology and detailed analysis of testing, results, and a comparative analysis with existing models. Finally, Section 4 concludes the work and recommends future aspects.

2. Overview of the Design Specifications of the Antenna Amplifier in a Receiver (RX) or Transmitter (TX)

Bandwidth and Frequency response: Maintain a frequency range of 3 MHz – 30 MHz and closed-loop mid-band gain greater than 15 dB. Since an HF antenna is being designed, a mid-band gain must be achieved in this frequency band and maintained within 3dB of this mid-band gain. [8].

Noise spectral density: Maintain an output noise of less than 1 nV/√Hz. This is essential in designing systems for antenna and RF design, as signal integrity is key [18, 40]. Various approaches can be taken to ensure this, such as internal and external filtering, LC coupling, and component substitution.

The input and output impedance should be profiled to maintain signal integrity over the HF frequency range. This will also allow for easier input matching when connecting an antenna to the input of the amplifier. The peak voltage of the input signal V_{pk} of 1 mV should be considered for an antenna of the characteristic impedance of 72 Ω, modelled accordingly.

S-Parameter analysis and impedance calculations have been graphically represented from the noted requirements and specifications, allowing a comparison between the designed work and referenced literature. In designing the antenna amplifier, one may follow a similar process as to what has been done by *Pillay and Srivastava* [11, 13]. This includes using asymmetrically driven DG MOSFETs and sinking current from NMOS current sources. The system operates from a dual-rail power supply, allowing maximum voltage swing and output power for a dipole antenna. Figure 1 highlights a high-level structure of a receiver system using an antenna amplifier.

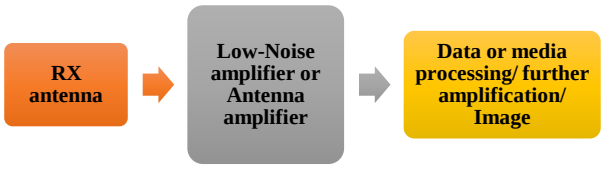


Fig. 1 System block diagram of antenna amplifier (The reverse structure of the above system would be utilised for a transmitter)

3. Design and Implementation of the Proposed Differential Antenna Amplifier

Using the differential-amplifier architecture, the following high-level schematic was designed for an antenna amplifier.

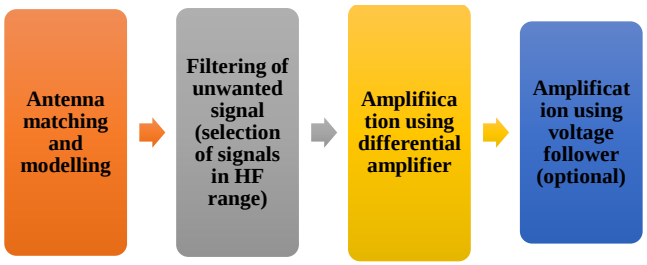


Fig. 2 High-level overview of the design process and requirements for the differential antenna amplifier

The theoretical dipole antenna exhibits a gain reduction, considering the antenna is an isotropic radiator. The antenna amplifier may also be known as an LNA since it's responsible for maintaining a low-noise output while preserving the signal integrity and sufficient amplification of low-power signals from a receive-antenna antenna [21-23]. Thus, assessing the amplifier designed in this paper, one should maximise power output and gain (dB), as a reduction in gain can be observed when an antenna is used with the amplifier. The gain of an amplifier can be given as [24-26]:

$$\text{Gain (Numeric)} = \frac{Vout}{Vin} \quad (1)$$

where V_{out} and V_{in} are the output-voltage and input-voltage peak values. However, it is obligatory to use the value dBi (decibels relative to an isotropic radiator) when discussing a propagation system, where the gain of such a system would be defined as [27]:

$$\text{GdBi} = 10\log\left(\frac{G_{NUMERIC}}{G_{ISOTROPIC}}\right) \quad (2)$$

where $G_{Isotropic}$ is the gain of the actual antenna specified by the manufacturer. In this work, two inductors are coupled in series to model a dipole antenna.

Considering the peak input voltage of 1 *mV* as discussed in section II and a minimum gain of 15 *dB*, the maximum output voltage is, using Eq. (2):

$$18 = 20\log\left(\frac{Vout}{1mV}\right)$$

$$V_{out} = 30\ mV$$

To model the dipole antenna, authors may consider its feed-point impedance. The NEC-2 model of a dipole antenna specifies a 72Ω-feedpoint impedance. The specifications of this model involve a lossless conductor using a wire height of 0.9 m. Using this, the dipole antenna with a feed-point impedance of 72Ω can be modelled by a four-element equivalent circuit proposed by *Tang et al.* [41]. The equivalent circuit consists of an RLC network in series with a capacitor, as shown in Fig. 3.

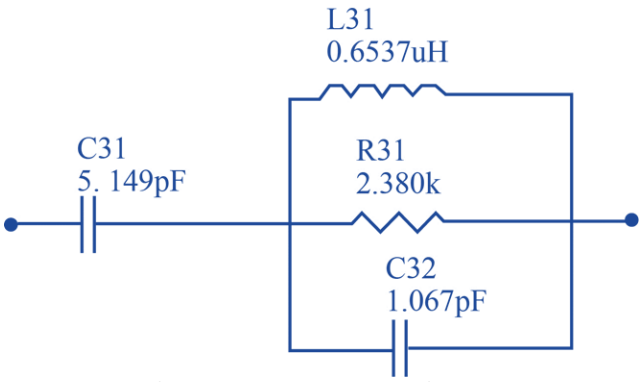


Fig. 3 Adapted from *Tang et al.*, showing the four-element circuit to model a dipole antenna for wire radius = 0.00264m

Using these specifications, authors determined the upper-frequency limit of 30 MHz, indicating the use of an antenna wire radius *a of* #28 AWG (0.00264m) and an antenna height *h* of 5.28 m. Using the expressions from [41] to determine C31, L31, R31 and C32, as depicted in Fig. 3:

$$C31 = \frac{12.0674h}{\log\left(\frac{2h}{a}\right) - 0.7245}pF \quad (3a)$$

$$C31 \approx 3.3\ pF$$

$$C32 = 2h\left\{\frac{0.89075}{\left[\log\left(\frac{2h}{a}\right)\right]^{0.8006} - 0.861} - 0.02541\right\}pF \quad (3b)$$

$$C32 \approx 3.3\ pF$$

$$L31 = 0.2h\left\{\left[1.4813\log\left(\frac{2h}{a}\right)\right]^{1.1012} - 0.6188\right\}\mu H \quad (3c)$$

$$L31 \approx 6\ \mu H$$

$$R31 = \{0.41288\left[\log\left(\frac{2h}{a}\right)\right]^{2} + 7.40754\left(\frac{2h}{a}\right)^{-0.02389} - 7.27408\}\ k\Omega \quad (3d)$$

$$R31 \approx 6.8\ k\Omega$$

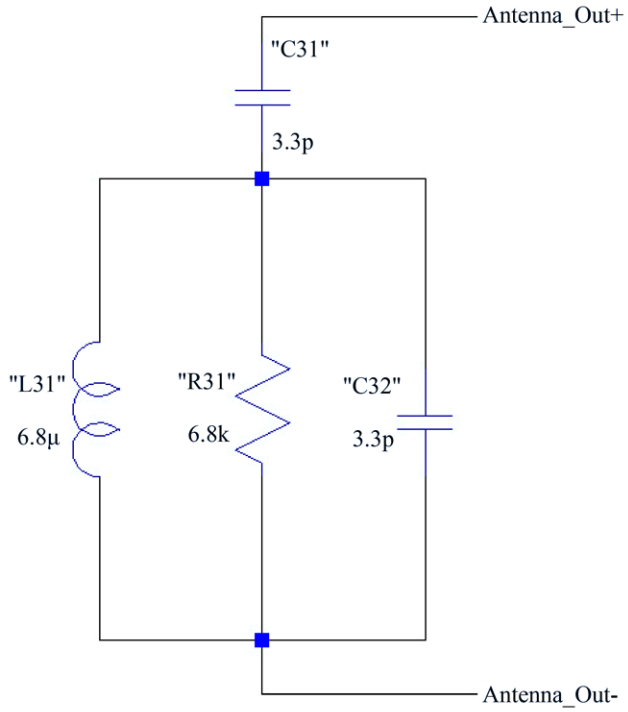


Fig. 4 Layout of antenna modelled with the four-element equivalent circuit [41]

3.1. Filtering and Selection of HF Signals

To adopt a bandpass-filter response, which would reject signals except for 3 – 30 MHz, a high-pass and low-pass filter has been cascaded at the input of the differential amplifier [29, 30]. LC 2nd order high pass filter, having a cut-off frequency $f_c \approx 3$ MHz, let C = 1 *nF*, thus:

$$L = \frac{1}{4\pi^2 C(fc)^2} \quad (4)$$

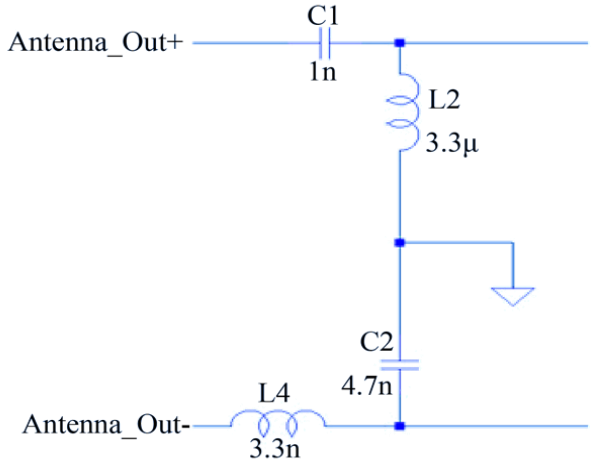


Fig. 5 Low-pass LC filter (given by C1 and L2) and high-pass LC filter (given by L4 and C2)

3.2. Amplification using a Differential Amplifier

Using the principle of a differential amplifier, a single-ended signal is split into a differential one and injected into the differential amplifier. For an amplifier, amplifying a signal from an antenna is made more accessible, given the antenna outputs can be injected as differential inputs. Considering the received signals of this amplifier, typical

voltage and received-power levels for 0 – 600 MHz signals are typically < 200 µV and 0.6 µW. The input signal will be injected into gate-1 of the DG MOSFETs. Thus, $V_{G1\text{-}S}$ can be approximated as 0.15 mV at maximum. This allows one to simulate the $V_{G2\text{-}S}$ values to improve the current draw by ensuring the MOSFET operates in the saturation region.

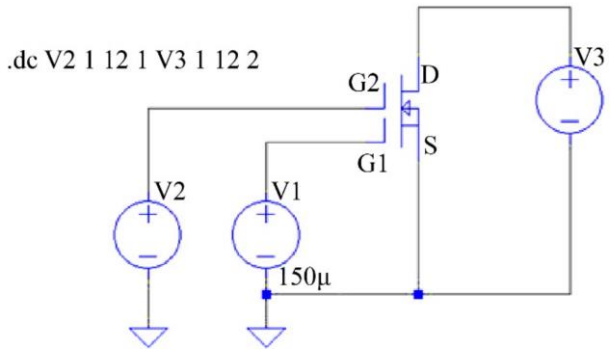


Fig. 6 Simulation setup of DG MOSFET to achieve DC operating current

From Fig. 7, an ideal V_{G2} (gate-2) voltage would be ≈ 4.7V for both DG MOSFETs of the differential amplifier, as the DG MOSFET operates comfortably in the saturation region for V_{DS} > 4V, consuming approximately 15 mA. This is adequate current consumption and shows a linear increase in the current consumption by the stand-alone differential amplifier designed in [10], where the drain current was designed to be 10 mA. The voltage bias for gate-2 of each DG MOSFET is taken from the schematic, where it is noted as "OUT_G2" (as shown in Fig. 8). U1 and U2 (shown in Fig. 9) are biased by the drain of U3 and U4 (As shown in Fig. 8), respectively. The following calculation can bias the current mirror designed in Fig. 8:

$$R = \frac{12}{15\ x\ 10^{-3}}$$

≈ 820Ω (E12 value, as shown by R7 in Figure 9)

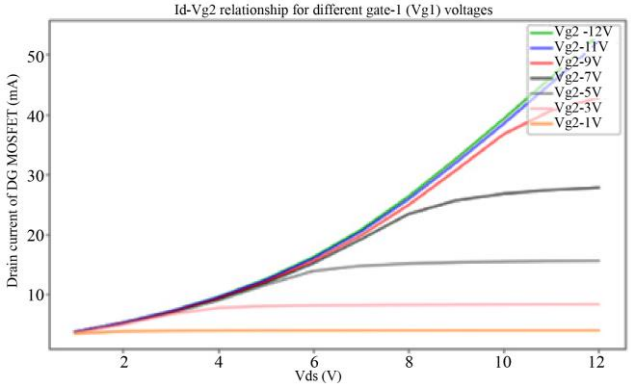


Fig. 7 Derived V_{DS} – I_D characteristics using V_{G1} = 150 µV

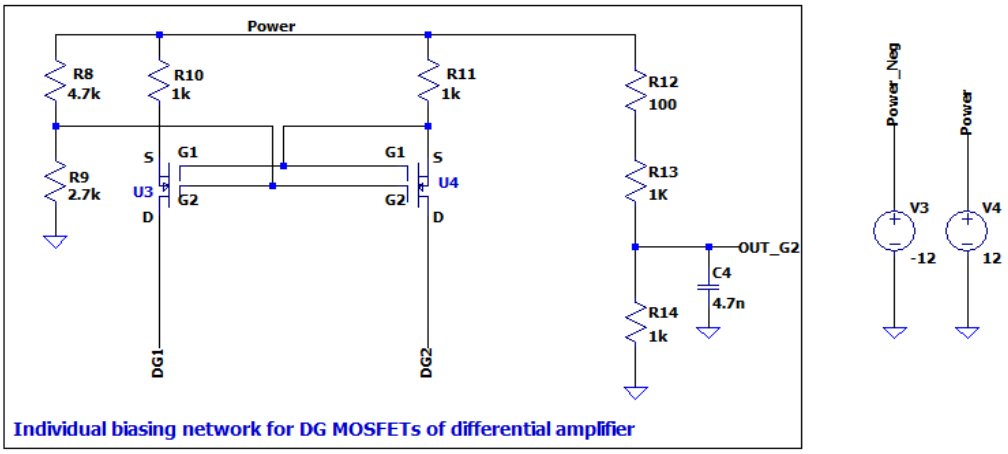


Fig. 8 Biasing network for differential amplifier's DG MOSFETs

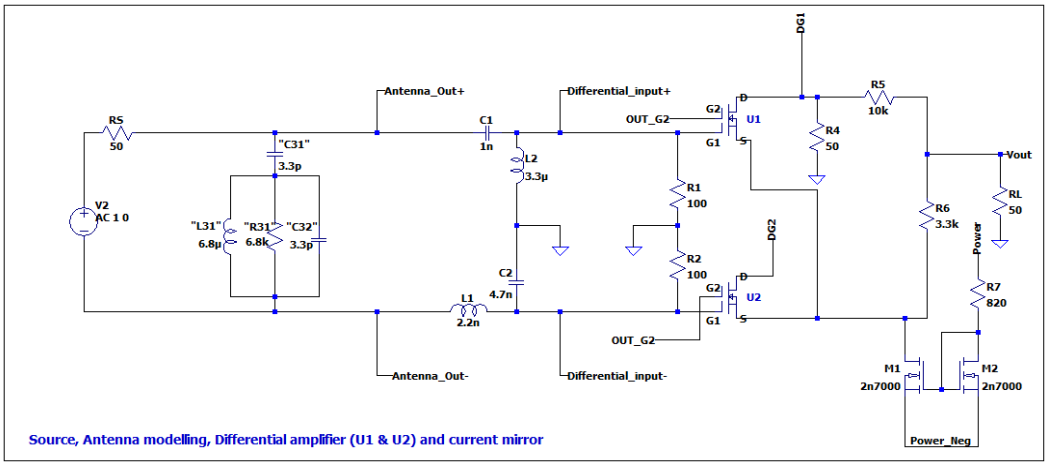


Fig. 9 Differential amplifier constructed using DG MOSFETs, biased by circuitry in Figure 8

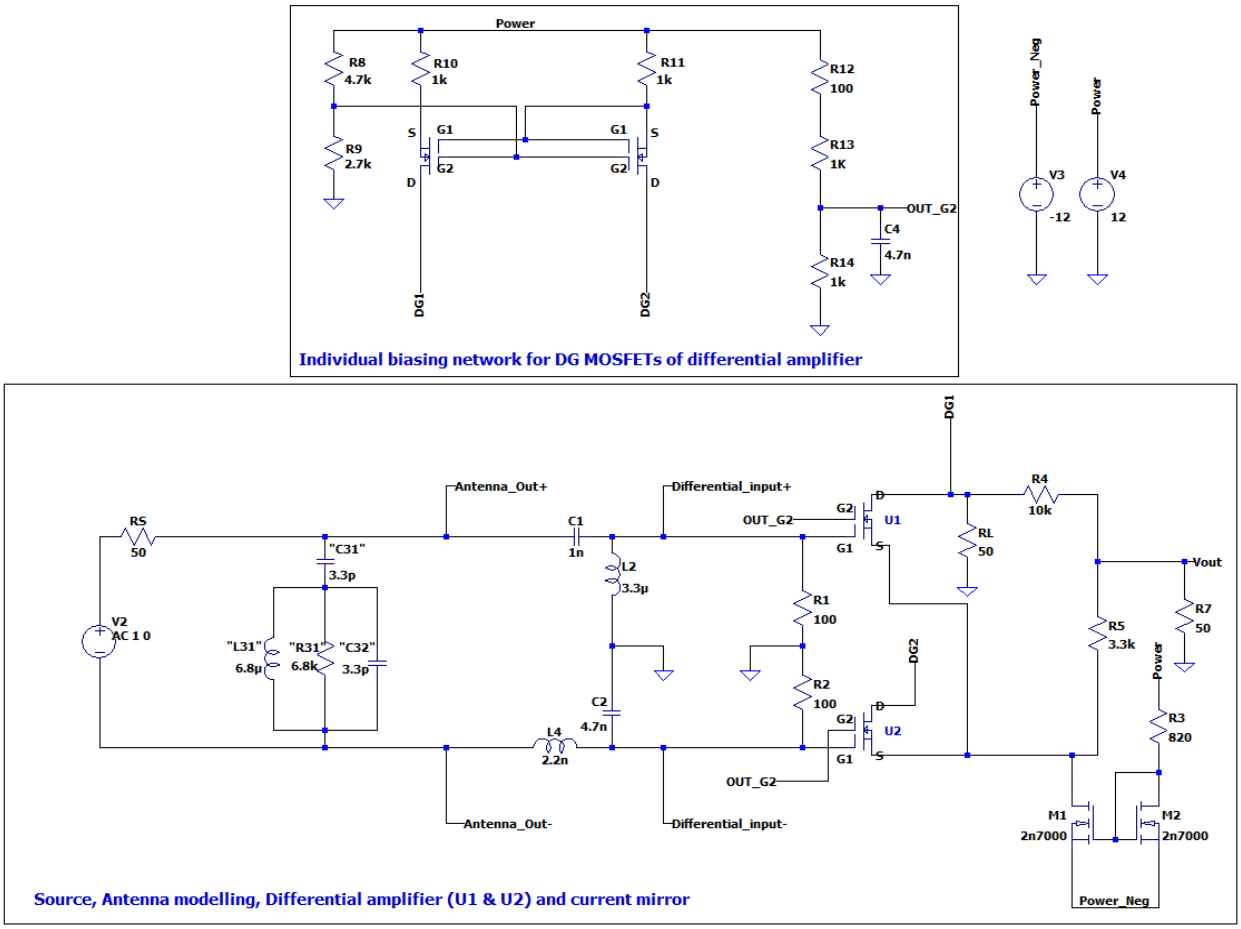


Fig. 10 Full schematic of antenna active-loaded differential amplifier

4. Analysis of Simulated Differential Antenna Amplifier

4.1. Frequency Response and S (Scattering) – Parameters

S-Parameters allow one to visualise circuit stability (checking if input impedances match, the ability of the circuit to avoid reflection) and power transmission from source to load (voltage, current, and power transfer, originating from the source to the load) [31-33]. Since the differential antenna amplifier is a two-port network, the S-Parameters for the amplifier can be depicted as such in Fig. 11:

Fig. 11 Two-port network visualised with S-Parameters

where ax is the normalised received signal at port x, and bx is the normalised reflected signal at port x [34].

S_{11} – Input reflection coefficient ($\frac{a_1}{b_1}$) is the ratio of the received signal at port 1 to the reflected signal at port 1.

S_{21} –Forward Transmission coefficient ($\frac{b_2}{a_1}$) is the ratio of the received signal at port 2 to the reflected signal at port 1.

S_{12} – Reverse transmission coefficient ($\frac{b_1}{a_2}$) is the ratio of the reflected signal at port 1 to the received signal at port 2.

S_{22} – Output reflection coefficient ($\frac{b_2}{a_2}$) is the ratio of the reflected signal at port 2 to the received signal at port 2.

The parameter S_{21} is equivalent to the frequency response shown in Fig. 11 for the designed differential antenna amplifier for a two-port network [35], as this is the forward gain of the amplifier, which should preserve its "flatness" and the desired bandwidth. The bandwidth of the antenna amplifier was designed to be approximately 30 MHz to provide an extensive range of "flatness" across the HF band. The frequency response can be attributed to the characterisation done in section III (A). S_{11} was obtained from simulation and is depicted in Fig. 13. The design considerations to improve S_{11} were to provide enough current and voltage drive for the antenna (where the four-element equivalent circuit was modelled) so that the antenna may radiate at a sufficient VSWR. The selection can see this of a larger power supply as opposed to work done in [11], allowing a greater input impedance and voltage at the gates of the differential amplifier.

The reverse transmission coefficient S_{12} and output reflection coefficient S_{22} can be shown in Fig. 14, along with S_{11} and S_{21}. A value of -46 dB is achieved for S_{12} and -23 dB for S_{22}.

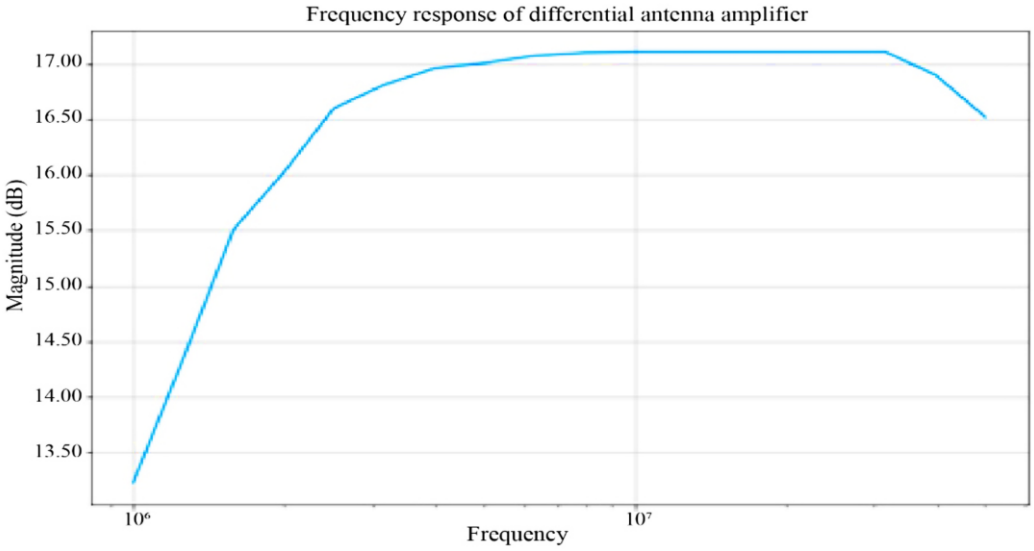


Fig. 12 S_{21} (Magnitude response) vs Frequency

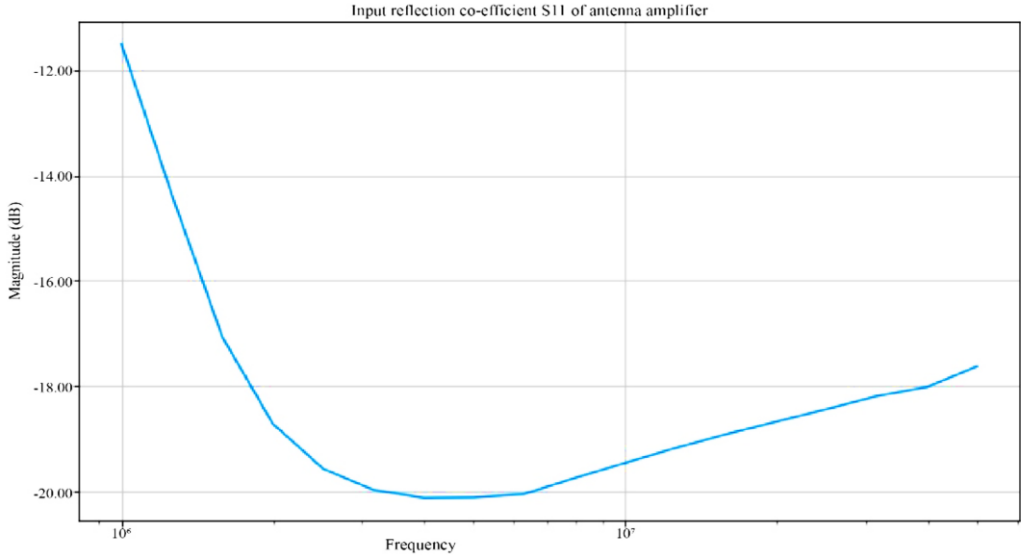


Fig. 13 S_{11} parameter vs Frequency

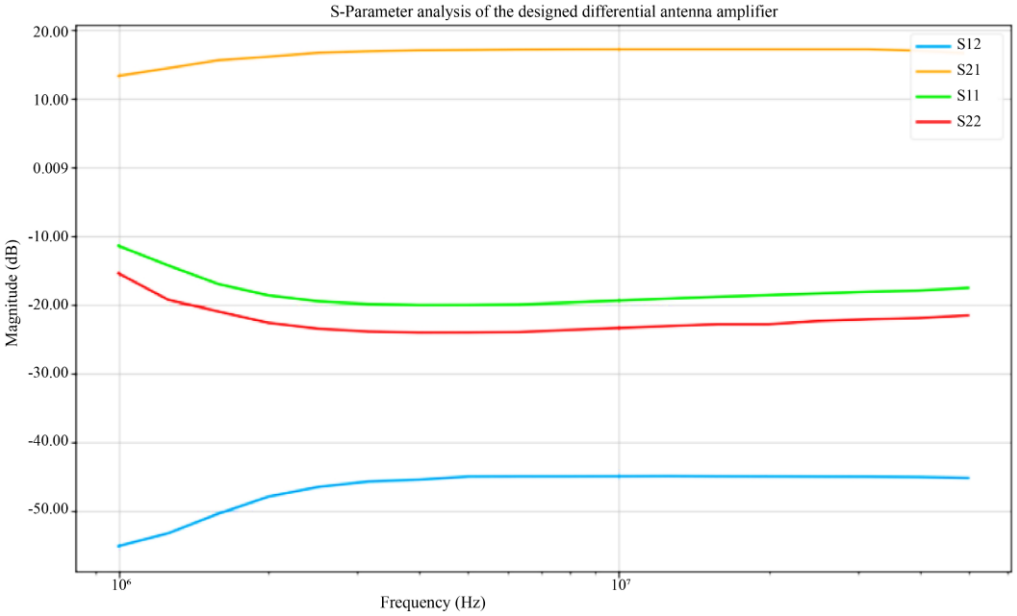


Fig. 14 Complete S-Parameter analysis of the differential antenna amplifier

Given the S-Parameters above, the insertion loss (using S_{21}) and input return loss (using S_{11}) can be computed [35]. The insertion loss IL can be given by:

$$IL = -20 \log |S_{21}| \quad (5)$$

For the designed antenna amplifier, the maximum S_{21} is 17.1 dB (shown in Fig. 12). Using Eq. (5), the maximum insertion loss is *-24.66 dB.*

The input return loss RL_{in} can be given by [35]:

$$RL_{in} = -20 \log |S_{11}| \quad (6)$$

Using Eq. (6), the minimum S_{11} is approximately -20 dB; thus, the minimum input return loss is *-26.02 dB.*

4.2. Noise Analysis and Methods of Reducing Output Noise

Using the *.noise* functionality in LTSpice, analysis of the total RMS output noise can be approximated for a given frequency [40]. The maximum output noise occurs at approximately the intended frequency band, receiving the typical gain of the amplifier. However, from the specifications in section II, the current design meets the specification. A few methods allow one to reduce noise in a circuit:

1. Reduce resistor values to 0 - 100Ω, which will reduce Johnson (thermal) noise. The formula for thermal noise that a resistor generates is:

$$\overline{V_n} = \sqrt{4kTR\Delta f} \quad (7)$$

Where R is a resistor's value, and other values are physical constants. Thus, this can help reduce the collective noise produced by a circuit.

2. For the high and low pass filters, designed in section III, a 2nd-order LC filter was used instead of a 1st-order RC filter. A 2nd-order filter provides a larger gain-reduction per octave [18].

3. The DG MOSFET exhibits an inherent noise figure of less than 1 dB at frequencies less than 200 MHz, given by the device datasheet

4. To approximate the total noise in an RF circuit, it is suggested that both the source and load resistance is 50 Ω, as shown in Fig. 15(a) by "RS" and "RL".

The test circuit shown in Fig. 15(a) can be used to find the resultant noise figure (NF) shown in Fig. 15(c), which is a maximum of 5.05 dB.

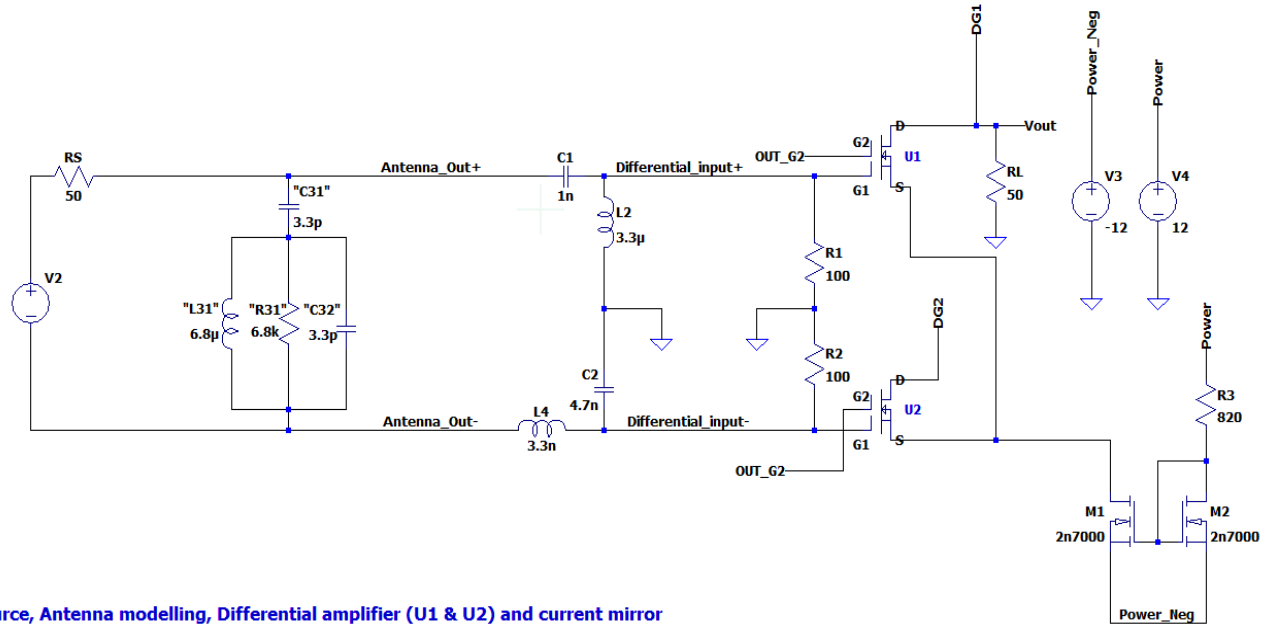
For a HF system, the noise figure is required to be less than 16 dB to achieve good signal integrity, given the frequency range is susceptible to external noise sources from the atmosphere. This is equivalent to a noise floor of -158 dBm/Hz or 4 nV_{pk}, for a 50 Ω load [35]. Given Fig. 15(c), the designed antenna amplifier exhibits good noise immunity.

4.3. Input and Output Impedance Measurement

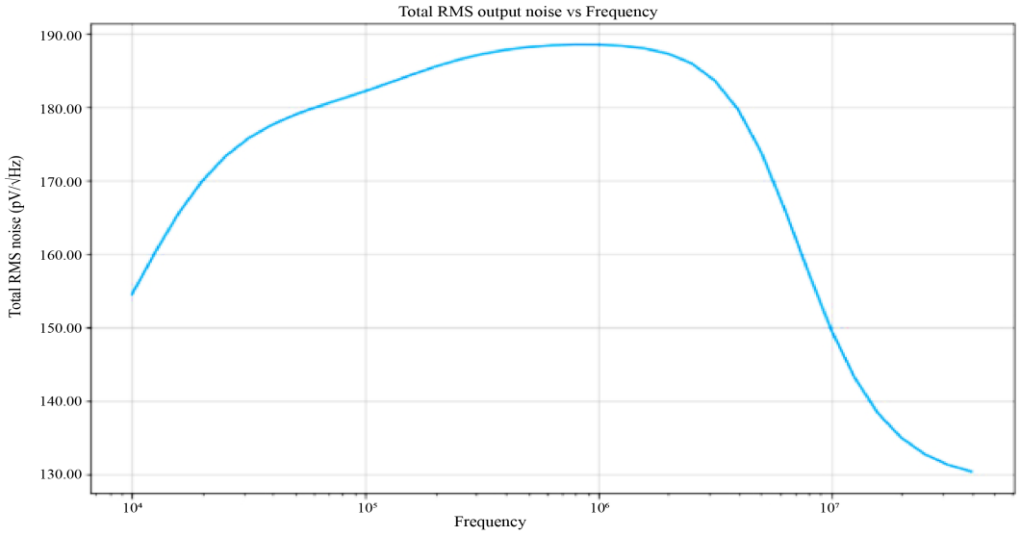
The antenna amplifier should have an output impedance R_L greater than an input impedance R_S. This comes from the graph in Fig. 16, showing the efficiency of power transfer in an amplifier relative to its input and output impedance [14]. The efficiency of an amplifier's power transfer from source to load can also be modelled as:

$$\eta = \frac{1}{1+(R_S/R_L)} \quad (8)$$

From the above efficiency computation using Eq. (8), the power efficiency given the input and output impedance is approximately 98%, which can be shown in Fig. 17 (a), (b), and (c) for the HF band.



(a)



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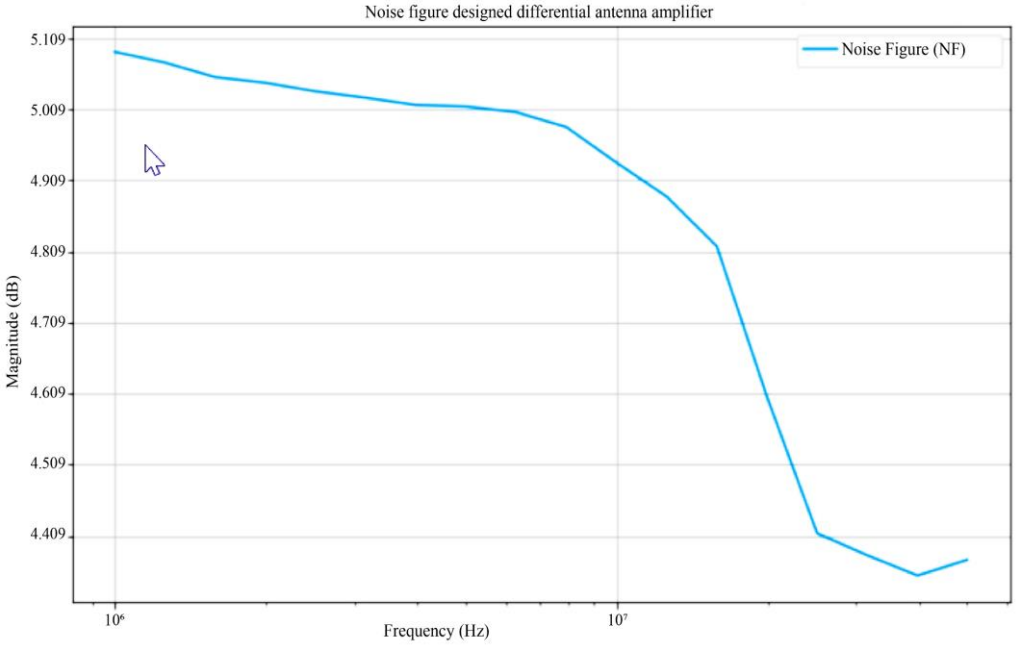


(c)

Fig. 15 (a) Schematic shown to calculate output noise; (b) Total RMS output noise vs frequency; (c) Resultant noise figure of designed differential antenna amplifier

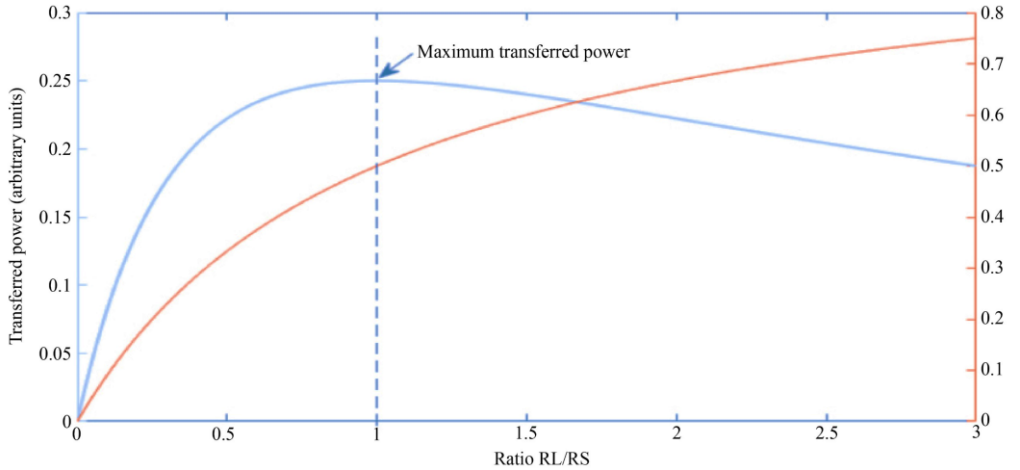
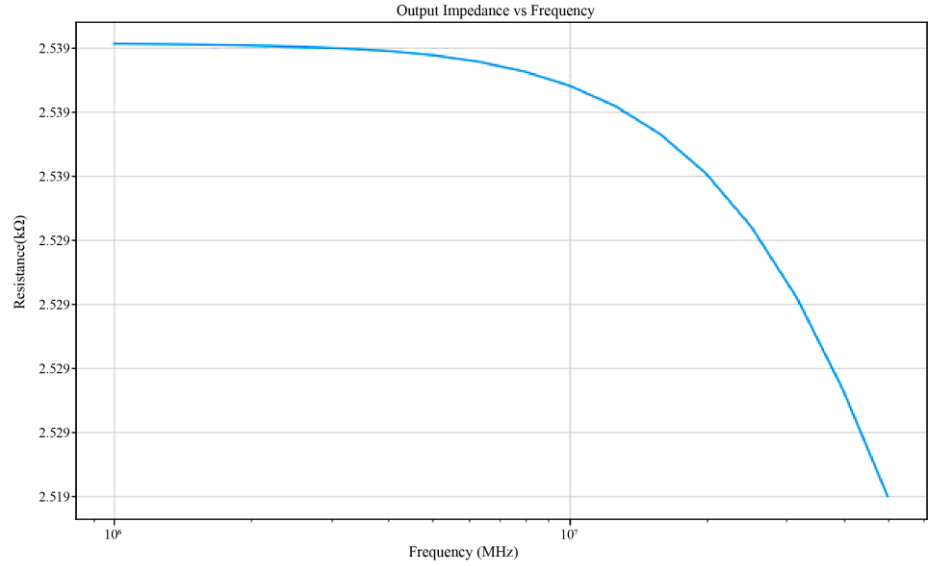
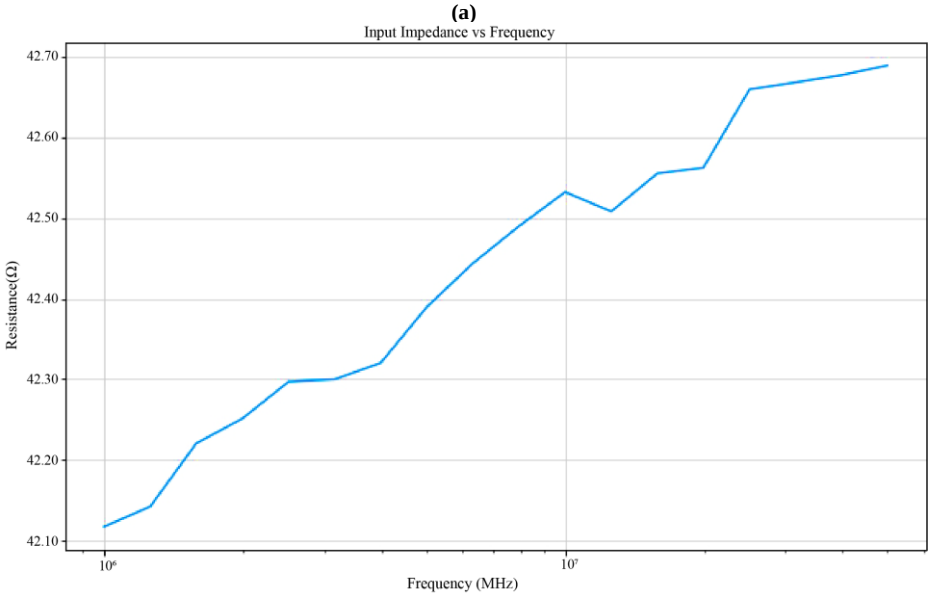


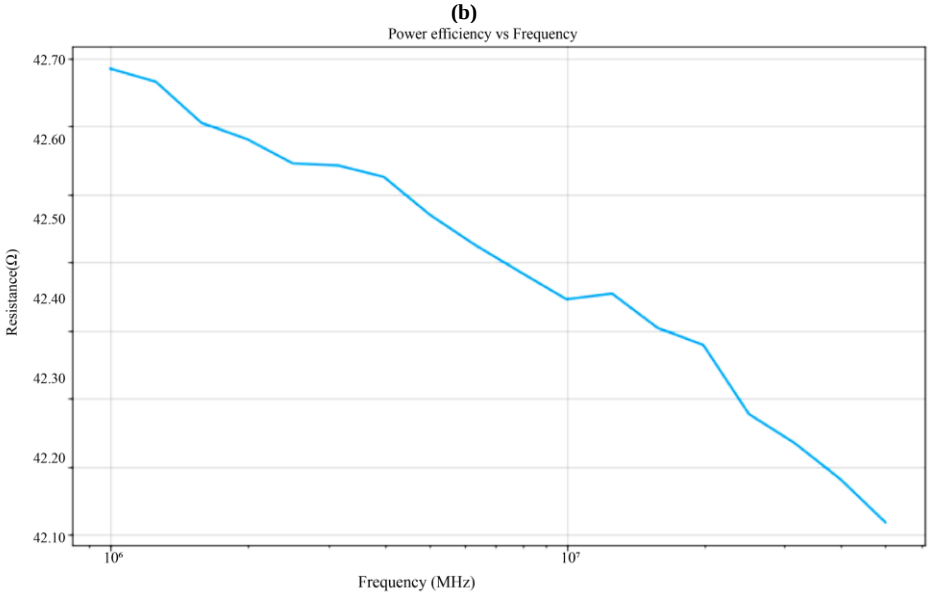
Fig. 16 Power efficiency relative to source and load impedance



(a)



(b)



(c)

Fig. 17 (a) Output impedance of designed antenna amplifier; (b) Input impedance of designed antenna amplifier; (c) Resulting power efficiency from input and output impedance

Table 1. Resultant parameters found by analysis of designed differential antenna amplifier

Parameter analysed	
Frequency spectrum	3 – 50 MHz
Bandwidth	≈ 40 MHz
Bias current	15 mA
Supply voltage	9 V
S_{21}	17.01 dB (midband for HF spectrum)
S_{11}	-20 dB
S_{12}	-50 dB (minimum, over HF spectrum)
S_{22}	-23 dB (minimum over HF spectrum)
Insertion loss	-24.66 dB (maximum over HF spectrum)
Return loss	-26.02 dB (minimum over HF spectrum)
RMS output noise	188pV/√Hz (maximum over HF spectrum)
Noise Figure	5.02 dB
Power efficiency	98%

5. Conclusion and Future Recommendations

From the initial specifications outlined in section III, the design of the antenna amplifier has met all of them. These specifications were outlined, in accordance with existing literature, specifically noted in this research work. An improved gain was noted for the high-frequency spectrum and was achieved by properly filtering the signal of choice, i.e. a 2nd order band-pass filter. The DG MOSFET utilised is also well-equipped, given its low noise figure at 1 GHz applications by the device specifications. Relative to the DG MOSFET, a high drain current was used (the maximum drain current for the BF998 DG MOSFET used in this research work is 24 mA).

The S-Parameter analysis shows that the designed differential amplifier has a high forward gain S_{21} of 17 dB at the midband. Cited literature shows that an improvement can be made in the forward gain. Still, given that these cited works use two-stage transistor architectures, the forward gain is shown to be optimised in such applications. The reverse transmission coefficient and input and output reflection coefficients S_{21}, S_{11} and S_{22} are kept to a minimum and are among the best-cited literature. This indicates that there is little to no loss of the input signal from the modelled antenna. S_{21} is also minimised and is shown to exhibit little reflection.

The resulting S-Parameters coincide with the low-power power-efficient nature of the designed antenna amplifier, given by the high power efficiency. Given the noise analysis of the designed antenna amplifier, the output RMS noise has been achieved, given the specifications in section II, i.e. an output RMS noise less than 1 $nV\sqrt{Hz}$, which also coincides with a low noise figure of 5.02 dB. The noise generated per Hz bandwidth has been minimised.

In seeing this, it may be concluded that the active-loaded differential amplifier, designed using a DG MOSFET, can support an inductive source being a dipole antenna while providing a low-noise, high-gain output. From the comparative analysis done in Table II, a respectable gain (forward transfer co-efficient) S_{21} can be seen, for a low-noise output, relative to a HF system. The proposed work has a smaller bandwidth than the comparable references, but this is such because of the outlined specifications.

This work aimed to exhibit the active-loaded differential amplifier in HF applications, which has been achieved by the design of the antenna amplifier from a simulation perspective. Possible antenna amplifier revisions could include an improved bandwidth and design improvements for improved gain and return loss characteristics.

Table 2. Comparison of antenna amplifier designed and their comparable parameters with the proposed work

Amplifier designed	Bandwidth	Gain (S_{21}, for this analysis)	S_{11} (Input reflection coefficient)	Noise figure	Bias current used
Differential LNA [15]	60 MHz	25.5 dB	-15 dB	1.07 dB	-
Compact wideband two-stage LNA [37]	3 GHz	24.8 dB	< -12 dB	3.4	9 mA
Microwave antenna amplifier [37]	≈ 40 MHz	14 dB at 2.45 GHz	-18 dB at 2.35 GHz	2	70 mA
RF antenna amplifier [37]	≈ 125 MHz	22.28 dB	- 12.77 dB at 2.35 GHz	2	-
Active antenna amplifier [37]	≈ 130 MHz	-	-11 dB at 2.35 GHz	2	-
Power antenna for 5G applications [38]	2 GHz	15.31 dB	-29.645 dB	-	-
RF Front-End Receiver for 5G applications [39]	400 MHz	15 dB	-32.128 dB	2.6 dB	-
This work	≈ 40 MHz	17 dB at midband (3 MHz – 35 MHz)	-20 dB at 3 MHz, minimum of 11.8 dB	5.05 dB (maximum)	15 mA

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