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Original Article

Prototype Design and Analysis of 4-Stage Operational-Amplifier using Double-Gate MOSFET

Joshua T. Ramdeo[1], Viranjay M. Srivastava[2]

[1,2]*Department of Electronic Engineering, Howard College, University of KwaZulu-Natal, Durban, South Africa.*

[2]*Corresponding Author : viranjay@ieee.org*

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Abstract *- This research work designs a 4-stage operational amplifier (op-amp) using Double-Gate (DG) MOSFETs. The DG MOSFET has various advantages over the traditional single-gate MOSFET. These advantages can provide the op-amp with more stability. A feasible solution has been proposed based on the design and analysis. Thereafter, a prototype has been fabricated and realized. The prototype has been tested, and various parameters have been analyzed, such as the output voltage, CMRR, slew rate, voltage losses, etc. The achieved voltage loss is 0.08 V, slew rate of 0.0549 V/µs, which is suitable for nanoelectronics device applications.*

Keywords *- Double-gate MOSFET, Operational-amplifier, Differential amplifier, Low energy device, Microelectronics, Nanotechnology, VLSI.*

1. Introduction

The scalability of technology is becoming smaller, as expected from Moore's law. The law states that the number of transistors on a microchip doubles every two years [1, 2]. Thus, with the increase in the number of transistors, the size of the microchips scaled down to accommodate this higher number of transistors. This decrease in the size of the transistors leaves the transistor devices susceptible to Short-Channel Effects (SCEs). These short-channel effects can become a greater problem as the transistors' size further decreases [3, 4].

Shi [5] has proposed a systematic g_m/I_D-based initial sizing method specifically customized for designing multiple-stage op-amp with a feature to use circuit-level design equations as constraints on the g_m/I_D—table lookup method to reduce the uncertainty in the sizing calculations substantially. The negative capacitance circuits can be systematically used to improve the gain-bandwidth product of the op-amp. Rasekh and Bakhtiar [6] presented a guide model deriving the conventional negative capacitance process. Finally, it designs a three-stage op-amp with a 15-nF capacitive load fabricated in a 0.18-µm CMOS technology. Kumar et al. [7] have designed a difference differential amplifier that used FinFET and CNT FET. This device is used for signal processing with the advantages of low-power dissipation and reduced device dimension. It realized the Power Supply Rejection Ratio (PSRR) of 2.53 dB with a dynamic range of 198 mV and 6 mV for CNT FET difference differential amplifiers operating at 0.6 V DC. Daryan et al. [8] have designed a multi-stage CMOS amplifier frequency compensation model using a single MOS capacitor. It has been simulated using MATLAB and HSPICE circuit simulator using TSMC 180-nm CMOS technology.

With the existing circuit topologies, the traditional multi-stage amplifiers can only achieve low gain bandwidths (*< 5 MHz*) and low slew rates *(< 10 V/µs*). These specifications are not satisfied by most op-amps. Therefore, *Kuo and Tsai* [9] have designed a multi-stage amplifier, including a recycling frequency cascade amplifier. This experiment showed that when driving a *5-pF/1-kΩ* load, the amplifier achieved *105.5 dB* DC gain, *231.77 MHz* gain bandwidth, and *13.25 V/µs* average slew rate. *Shi* [10] has analyzed the automation of distortion analysis of multi-stage op-amp by a symbolic analysis. The goal was to generate readable closed-form design equations that relate the frequency-dependent harmonic distortion features, such as DC level, corner frequency, peaking, and zero, to the circuit parameters (including the nonlinearity coefficients). A performance-boosting frequency-compensation technique was presented in by *Liu et al.* [11]. The proposed structure consists of three parts that ensure stability and significantly improve performance, such as gain-bandwidth product, slew rate, and sensitivity. It drives a *2-pF* load capacitance and achieves GBW of *2.41 GHz* with a phase margin of *82.6°* while consuming *12.6 mW* with a *1.2 V* supply voltage in a TSMC 65-nm CMOS technology.

Wang et al. [12] have proposed the Routh-Hurwitz stability criterion for the analysis and design of the op-amp stability, this can lead to explicit stability condition derivation for op-amp circuit parameters, and this is very effective, especially for the multi-stage op-amp. *Biabanifard et al.* [13] have presented a comprehensive approach to frequency-compensating multi-stage amplifiers. Different stage cases were considered, such as differential voltage and current blocks and general compensation blocks for

both voltage and current states. For demonstration, two circuits were designed in TSMC 0.18-µm CMOS technology. *Kumar and Vaithiyanathan* [14] have designed a simple three-stage class-A op-amp using indirect feedback compensation at 180-nm technology. It produced an open-loop gain of *84.7dB*, unity gain frequency of *45.65 MHz*, phase margin of *89°*, and slew rate of *14.45 V/µSec*, and it could drive a *30 pF* load. *Biabanifard et al.* [15] have analyzed a frequency compensation for three stages amplifiers based on the revered nested Miller compensation structure. Simulations were performed using HSPICE and TSMC 0.18-µm CMOS technology to verify the robustness of this circuit. It shows a DC gain of *114 dB*, a gain bandwidth product of *6.66 MHz*, and a power consumption of *360 µW*.

Omoru and Srivastava [16] have designed a MOSFET-based absorber active integrated antenna. This antenna operates at frequencies ranging from *2 GHz* to *3 GHz* and from *4.6 GHz* to *6.1 GHz*, thus providing a bandwidth of *1 GHz* and *1.5 GHz* at a resonance frequency of *2.5 GHz* and *5.3 GHz*, respectively. This antenna has a radiation efficiency of *84%* has been observed. The idea and application of that work have been extended here in this present research work to design a 4-stage op-amp using DG MOSFET.

Operational amplifiers are commonly implemented with the use of single-gate MOSFETs. These single-gate MOSFETs are susceptible to short-channel effects as the size of the MOSFET decreases. Hence, this research work aims to design and build a 4-stage operational amplifier using a Double-Gated MOSFET. The double-gate MOSFET should be able to overcome the problems experienced by the single-gate MOSFET. The second gate provides greater control over the channel and, by extension, greater control over the current that flows through the channel. The design must be compared to 4-stage op-amps available in the market to show its ability to compete. This is achieved by looking at the parameters used to test the products on the market, such as the output voltage, amplification/gain, time taken to produce output voltage (settling time), voltage loss, CMRR, and losses (conduction losses or switching losses). This paper has been organized as follows: Section 2 has the basic component selection, and Section 3 has the design methodology for this device. Section 4 has a full circuit design and its analysis with simulation. Section 5 is about prototype design and its analysis. Finally, Section 6 concludes the work and recommends future aspects.

2. Basic Components Selection

2.1. Operational Amplifiers

Operational amplifiers are one of the building blocks of analogue circuits. Figure 1 shows the op-amp as the basic unit. The op-amp is, however, created with internal circuitry using transistors, resistors, and capacitors to achieve the desired output voltages. The op-amp is used to amplify the voltage, and the amplification factor is determined by the gain (A) of the amplification. The output voltage of an operational amplifier is [17]:

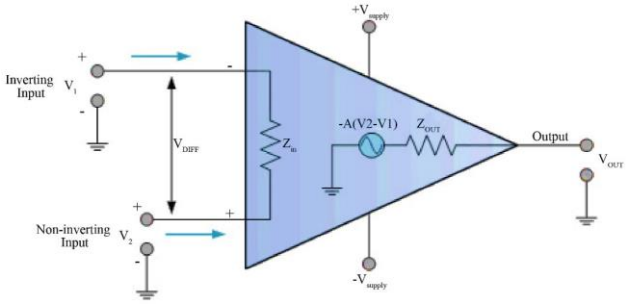


Fig. 1 Equivalent circuit of an operational amplifier [17].

$$V_{out} = A(v_{in1} - v_{in2}) \tag{1}$$

By Eq. (1), the output voltage is calculated by taking the product of the gain and the difference between the input voltages. The efficiency of the op-amp is one of the parameters used to judge the quality of the operational amplifier [17]:

$$n = \frac{\text{Power out}}{\text{input power}} \times 100\% \tag{2}$$

The op-amps are used in analogue computers and various other applications such as Very Large Scale Integration (VLSI). Operational amplifiers are very versatile components as they can be used in several different circuits, such as active filters, waveform converters, DAC, and ADC converters, to name a few [18, 19]. The Common Mode Rejection Ratio (CMRR) is another parameter used when comparing the various op-amps. This is the measure of how well the op-amp is able to eliminate the common signals in the input. The most common source of the common mode input signal is the noise (about *50 Hz* to *60 Hz*) present at both inputs. Another source is the electromagnetic interference coupled to the circuit, which is present at the input when the op-amp is operated in a high electromagnetic field. Ideally, the op-amp should keep this common mode signal at a minimum at both inputs. The CMRR is determined by taking the ratio of the differential gain over the common mode gain (in dB):

$$CMRR = 20\,log(\frac{A_d}{A_{CM}}) \tag{3}$$

There are cases when a single op-amp cannot output the amount of gain required. This is the purpose of the multiple-stage amplifiers used in this present research work. By cascading amplifiers, the gain can be increased exponentially. In cascading amplifiers, the output of one amplifier becomes the input of the following amplifier [20, 21]. Multi-stage amplifiers are achieved by cascading amplifiers. Cascading amplifiers are done to achieve higher voltage or current gains. The gain represents the ratio of the output signal to the input signal:

$$A_V = \frac{V_{output}}{V_{input}} \tag{4}$$

The cascaded amplifier gain is calculated by taking the product of the individual stages. The gain of the individual stages is determined by their configuration:

$$A_V = A_1 \times A_2 \times A_3 \ldots \tag{5}$$

2.1.1. Dual-Gate (DG) MOSFET

The Dual-Gate (DG) MOSFET has two gates. This additional gate (compared to the traditional MOSFET) provides better isolation between the drain and gate [22, 23]. The introduction of the additional gate reduces the amount of feedback capacitance between the input and the output circuits. Thus, allowing them to be more stable amplifiers [24, 25]. The additional enable the channel to become larger and accommodate a larger current between the source and the drain. In DG MOSFET, the second gate also creates a channel within the body of the MOSFET, allowing for a greater number of electrons to flow through [25-27,49].

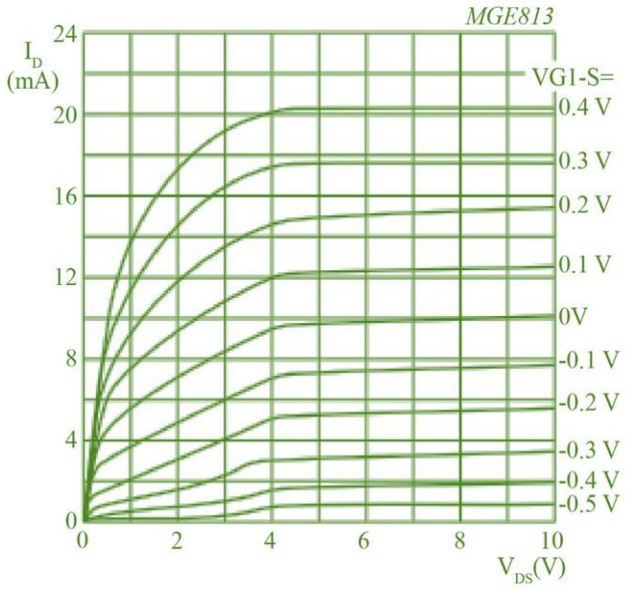


Fig. 2 V-I Characteristics of the DG MOSFET (BF998) [29]

As seen in the graph of Fig. 2, when the applied voltage is above 3 V to 4 V, it remains in the saturation region. The BF998 double-gate MOSFET has better power efficiency and switching capabilities than the single-gate MOSFETs [29-32]. The double gates also provide greater channel control compared to the traditional MOSFET. This will allow for the amplifier to be more stable. This MOSFET is ideal for Very High Frequency (VHF) and Ultra-High Frequency (UHF) applications. The coupling capacitance between the conducting channel and the substrate is smaller on Silicon-on-Insulator (SOI) MOSFETs compared to the technology used in single-gate MOSFETs (bulk CMOS). Since the same process is experienced from the second gate as the first, w.r.t. the formation of the channel to connect the drain and source, this will result in a higher current drive from the devices created using the SOI technology. The downsizing of the MOSFETs will increase SCEs, such as subthreshold slope, drain induced barrier lowering, which is present in the bulk CMOS technology [33, 34].

3. Design Methodology

The first stage of the operational amplifier is a differential amplifier. This differential amplifier takes in the two inputs and can output a single or double output, depending on the biasing used to create the circuit. The differential amplifier is the first stage in constructing the 4-stage op-amp; this stage will contain the DG MOSFETs (BF998), as this is the stage receiving the input signal [35-37].

When analyzing the circuit, the input signal can be seen as 2 linear combinations. The differential mode and the common mode. The differential mode is defined as:

$$v_{idm} = v_1 - v_2 \tag{6}$$

And the common mode is defined as:

$$v_{icm} = \frac{v_1+v_2}{2} \tag{7}$$

Therefore, taking these into account, the actual input signal can be expressed as:

$$v_1 = v_{icm} + \frac{v_{idm}}{2} = \frac{v_1+v_2}{2} + \frac{v_1-v_2}{2} \equiv v_1 \tag{8}$$

$$v_2 = v_{icm} + \frac{v_{idm}}{2} = \frac{v_1+v_2}{2} - \frac{v_1-v_2}{2} \equiv v_1 \tag{9}$$

The total response of the differential amplifier is taken as the superposition of the 2 input signals. This is how the common mode is eliminated from the output signal. CMRR ideally should be infinite; however, this is not the case for real op-amps, and instead, the CMRR is aimed to be as high as possible [38, 50]. A high CMRR value implies that the amplifier can amplify the differential signal in the presence of a large common mode input.

As in Fig. 4(a), there is a box in place holder (device-1 and device-2) where the transistor will be placed. The differential amplifier is usually made using MOSFETs or BJTs. The brilliance in the design s that devices-1 and 2 are a matched pair. The upper terminals of the transistor pair are connected to the positive power supply ($+V_{cc}$) through a passive series element (such as a resistor), and the lower terminals are connected. A current source pulls down current toward the negative rail of the power supply ($-V_{cc}$) [40-42]. The current source is used to affect the biasing of the circuit. The control ports (gates/bases) are connected to the input signals. A DC current source cannot be bought; rather, this is created using transistors or can be done using a resistor. The method of using transistors to make the current source is known as a current mirror.

The differential amplifier in the circuit is also responsible for taking in the double input and producing a single output; this signal is then sent as an input to the next stage of the multi-stage op-amp. Here the BF998 double-gate MOSFET has been used. The 4 V DC supply is connected to gate-2 of the DG MOSFET, used to turn on the transistor, keeping the MOSFET in the saturation region. This value is seen in Fig. 2, which is the relationship between the drain-to-source voltage and the drain current. It begins to level out, thereby entering the saturation region at approximately 4 V. The 4 V at gate-2 is used to keep the MOSFET in saturation mode, which is the region the MOSFET needs to be in be suitable for amplification. The AC signal is then sent to gate-1.

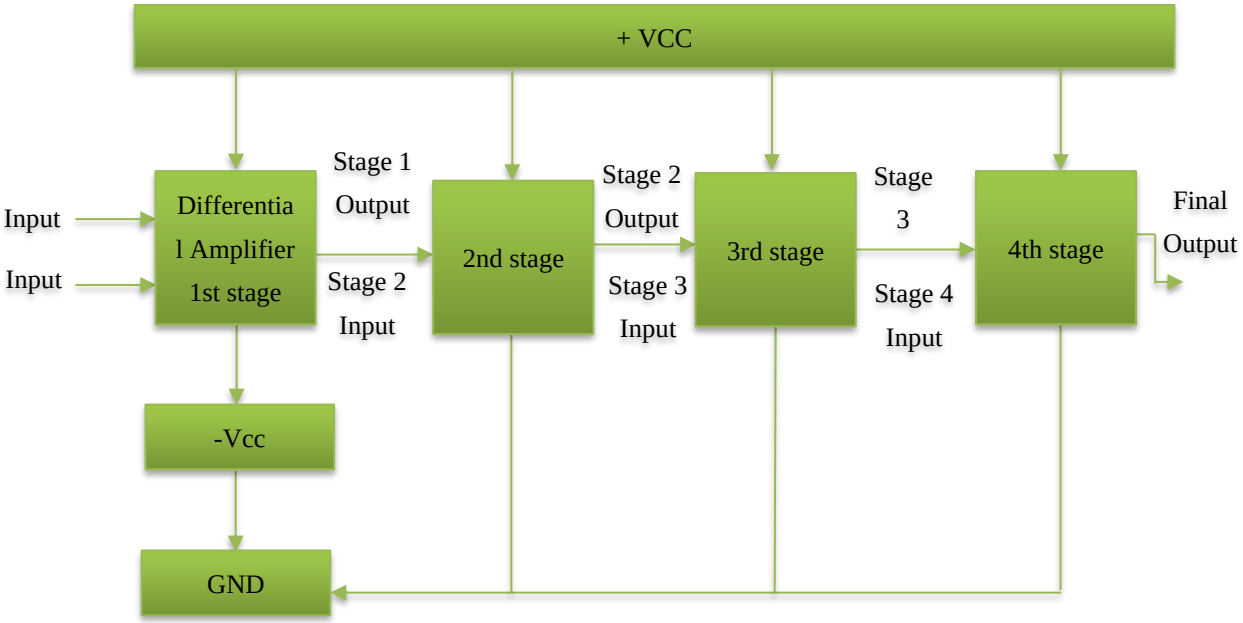
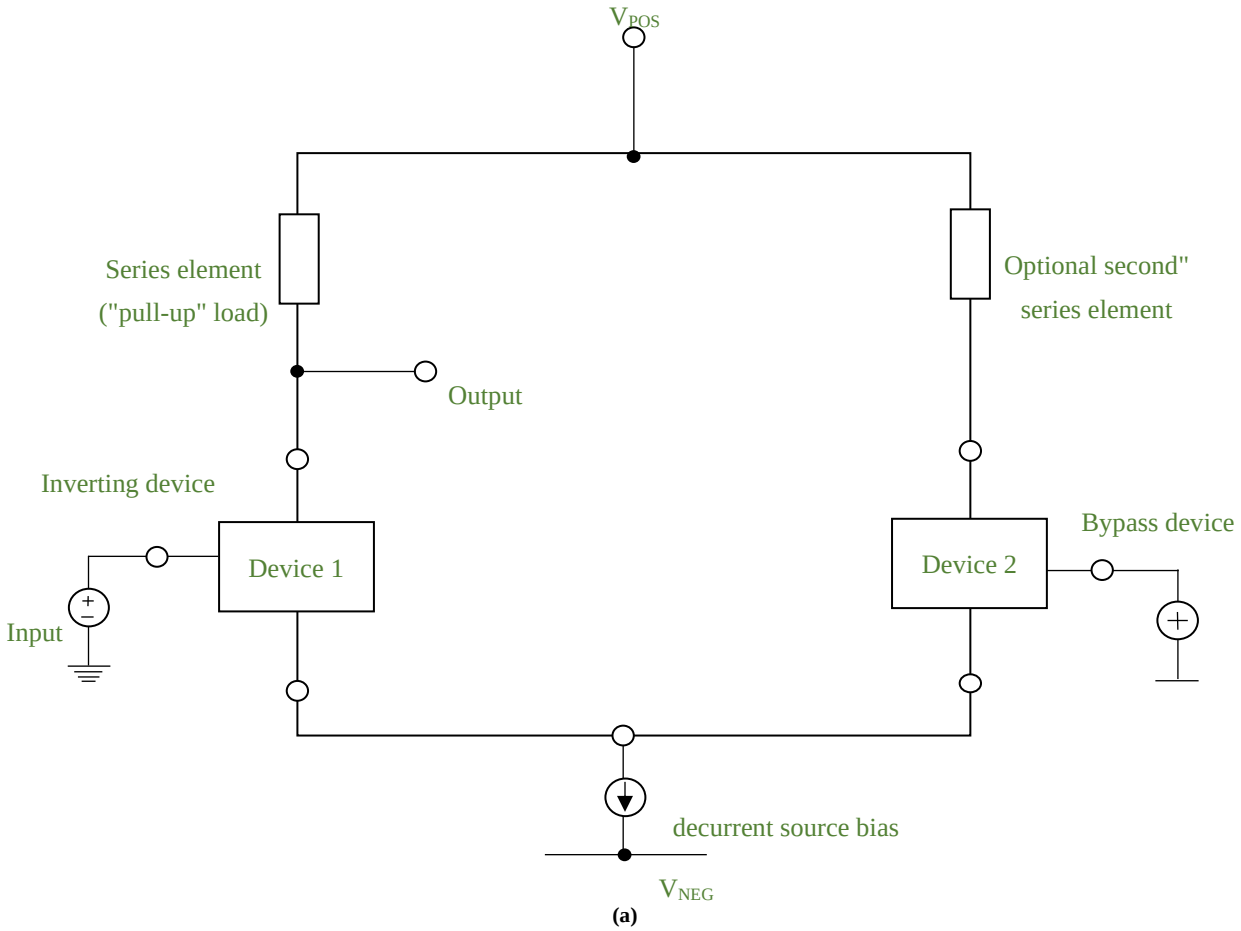


Fig. 3 Block Diagram shows the low-level solution of the 4-stage op-amp

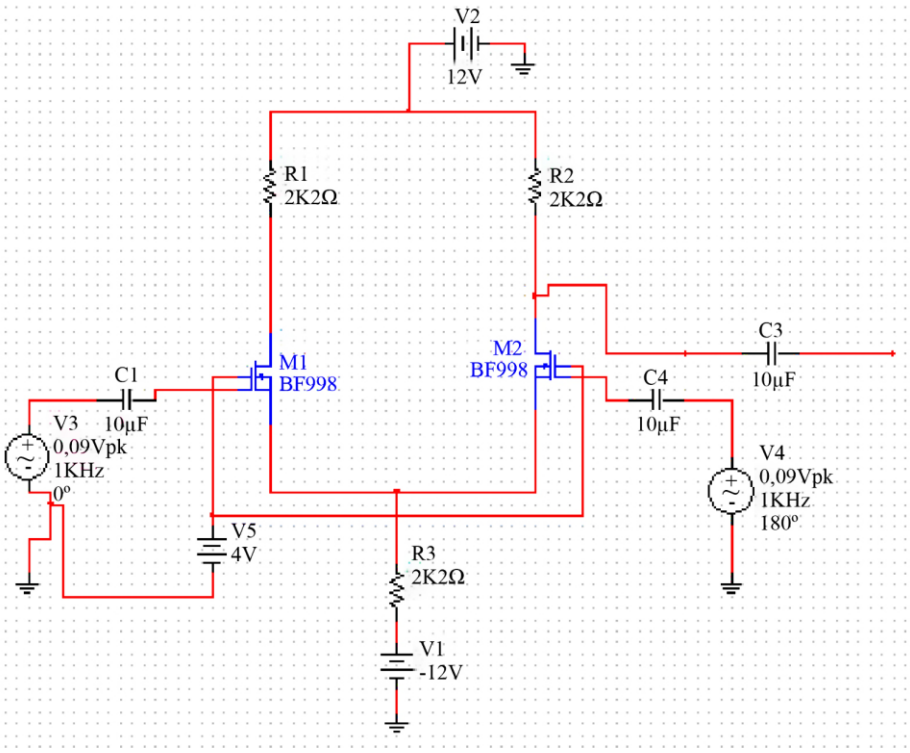
The working principle of the differential amplifier describes that the current at the node between the two current sources is split evenly between the MOSFETs. Keeping this assumption, the calculation for the differential circuit (Since the current is split evenly):

$$I_{D1} = I_{D2} = \frac{I_{SS}}{2} \tag{10}$$

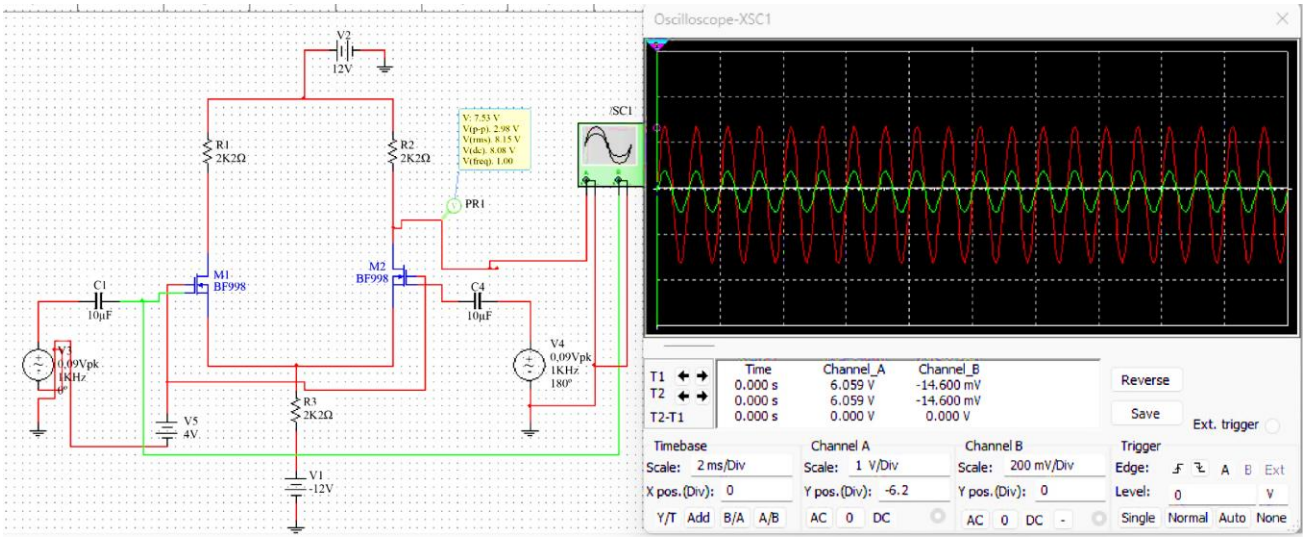
$$I_{SS} = \frac{V}{R} = \frac{12}{2k2} = 5.45mA \quad \text{and} \quad I_{D1} = I_{D2} = \frac{I_{SS}}{2} = \frac{5.45}{2} = 2.73mA$$



(a)



(b)



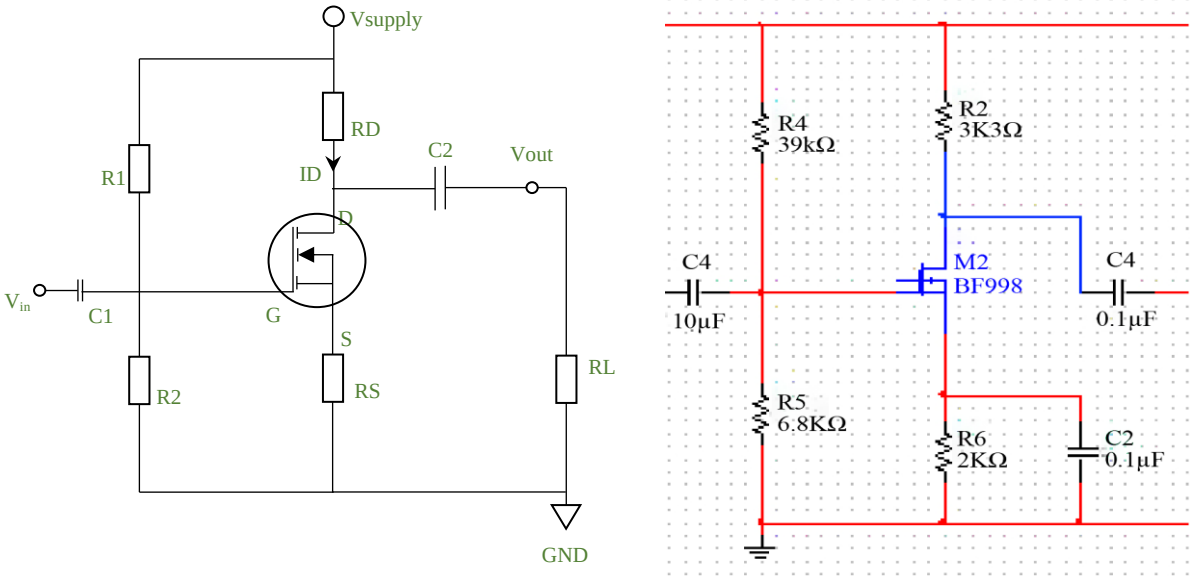
(c)

Fig. 4 (a) Block diagram, (b) Circuit, and (c) Output of differential amplifier using DG MOSFET

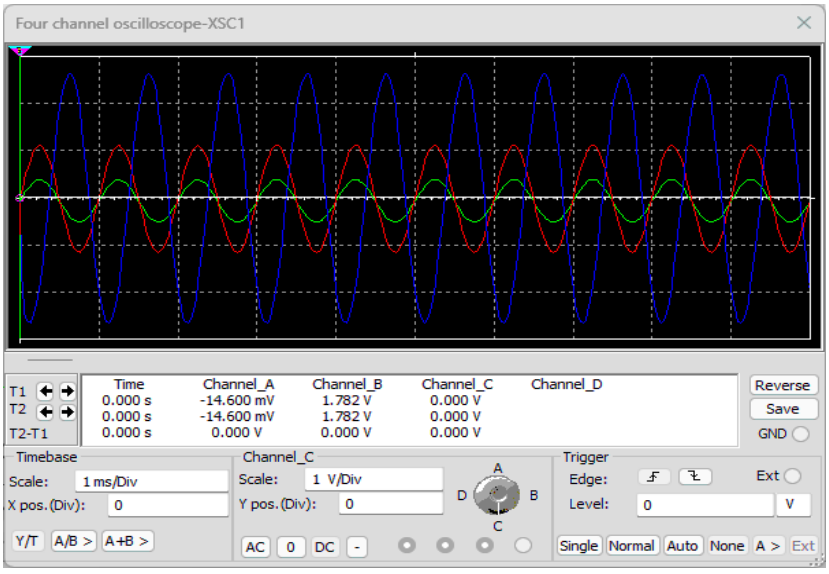
Therefore, the voltage supplied to gate-2 of the MOSFET is equal and will become common mode signals. However, these will keep the MOSFET in the saturation region; thus, gate-1 will just be needed for the signal that must be amplified. The output voltage of the differential amplifier will serve as the input to the second stage. The output voltage is then determined using

V_{DD} = 12 V, I_{ss} = *5.45 mA* and R_D = *2.2 KΩ*; then, using $V_{out} = V_{DD} - \frac{I_{ss}}{2} R_D$, the output voltage is achieved *as 6 V*.

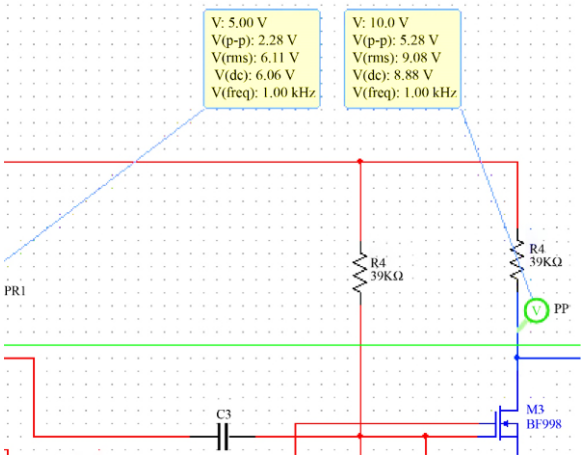
Figure 4(c) shows the differential stage output (stage-1 of 4). There is significant gain experienced in this stage. This is depicted in the signal analyzer, where the green waveform shows the input signal at one of the gates. This green waveform is shown with a *200 mV/Div* scale. The red waveform shows the output of the differential stage. The red waveform is shown with a *1 V/Div* scale. The output of the differential amplifier is then connected to the next stage's input. The red output waveform is sent to the input stage of the second stage of the 4-stage op-amp. The first stage is used to accept the 2 inputs as to be expected in the operational amplifier and produces a single output.



(a) **(b)**



(c)



(d)

Fig. 5 (a) Block diagram of a MOSFET amplifier, (b) Amplifier circuit using the BF998, (c) Outputs waveform, and (d) output voltage of the 1st and 2nd stage

Figure 5(a) shows one of the topologies for a MOSFET amplifier. The voltage divider (R_1 and R_2) is used to bias the circuit. The R_1 and R_2 values are usually large to maximize the amplifier's input impedance. Another advantage of choosing the higher resistors is to reduce the ohmic power losses. Capacitors C_1 and C_2 are used as coupling capacitors which are needed to protect the DC biasing voltage from the AC signals. The resistor R_L is used to depict the load, where the output voltage is sent after being amplified.

$$V_G = (\frac{R_2}{R_2+R_1}).V_{SUPPLY} \quad (12)$$

For the 2nd stage:

$$V_G = (\frac{6.8K}{6.8K + 39K}).12 = 1.78V$$

For the 3rd stage:

$$V_G = (\frac{2.3K}{2.3K + 10K}).12 = 2.24V$$

For the 4th stage:

$$V_G = (\frac{15K}{15K + 39K}).12 = 3.33V$$

Here V_G gives the bias voltage due to the resistors creating the voltage divider circuit. This is used to bias the MOSFET to be used for amplification. The amplifier configuration used in creating the second to fourth stage is a common source amplifier configuration. This configuration provides a high input impedance and low noise output. These characteristics make them more suitable to be used for amplifier circuits. Adding the resistor between the source and the ground creates a more efficient amplifier.

$$v_o = -g_m v_{gs} R_D \quad (13)$$

The stages after the differential amplifier, stages 2 to 4, are used to increase the gain of the amplifier. In Fig. 5(c), the simulation shows the waveforms of the input signal (green), the output of the 1st stage or the differential stage (red), and the output of the second stage (blue).

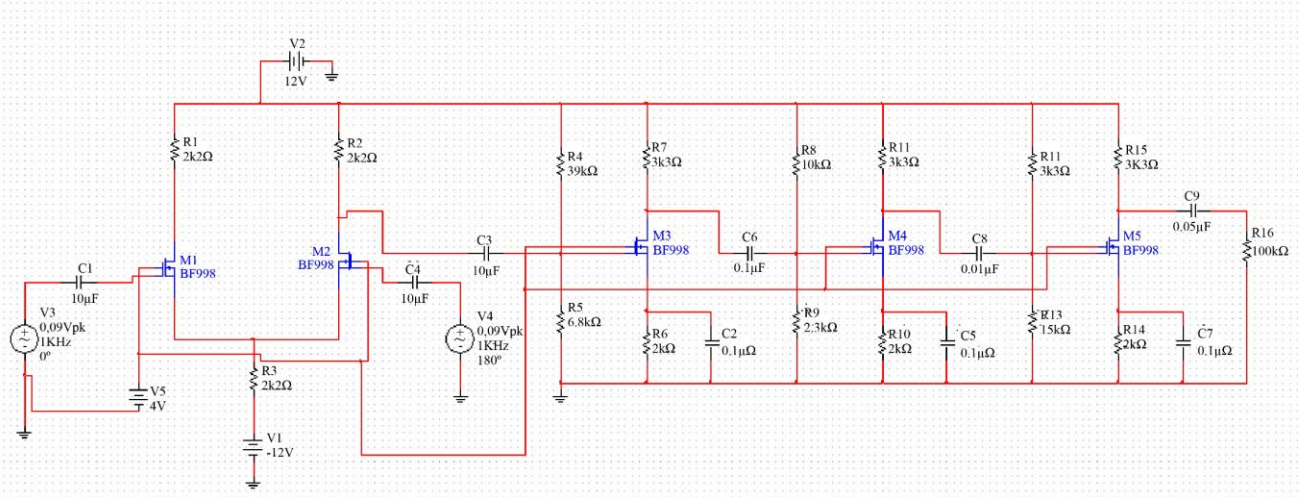
The scale for the input signal is kept at *200 mV/Div*, like in the differential stage. The scale of channels *b* and *c*, which show the waveforms of the outputs from the differential and 2nd stage of the 4-stage op amp, are set to *1 V/Div*. The increase in amplitude between the red to the blue is clearly visible. Figure 5(d) shows the output voltages achieved moving from the 1st and 2nd stages of the 4-stage op-amp. As with the differential stage, the free pin will be connected to the 4 V DC voltage to keep the MOSFET in the saturation region.

4. Circuit Design and its Analysis with Simulation

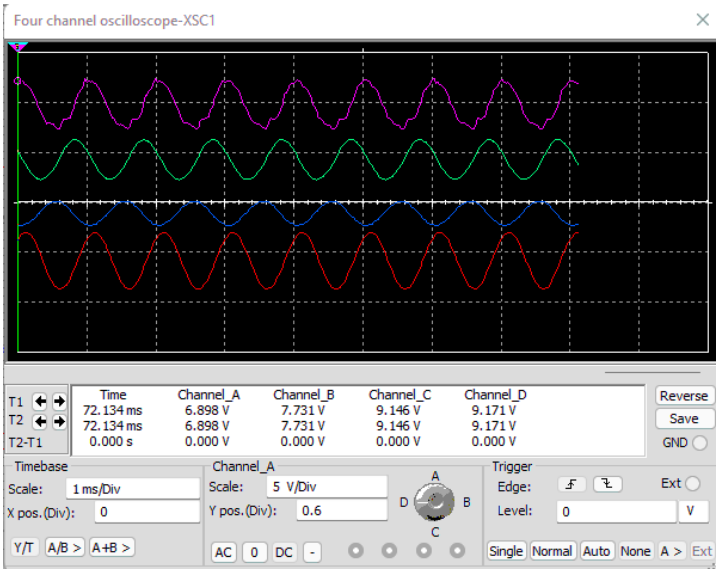
On the basis of the previous section modeling, the full circuit of the 4-stage op-amp has been designed, as shown in Fig. 6(a), using BF998 DG MOSFETs. The analyzed parameters have been compared with the traditional Single-Gate (SG.) MOSFET. Figure 6(b) shows the outputs of the 4-stage op-amp. The increase in voltage can be seen as the op-amp movies through the stages. Channel-A (red line) is taken from the output of the differential amplifier all the way to channel-D (pink line), which is taken at the final output.

The input signal needs to be *180°* out of phase. This ensures no common mode signals and, thus, no losses in the input signal due to CMRR. In simulations, two input sources were used, with one set to have an offset of *180°*. The input signal setup can be seen in Fig. 8. This shows the shift in the input signal to be offset by *180°*, as seen next to the phase heading.

The inverting op-amp can be used to achieve this 180 ° phase shift. During the building process, a single-function generator is used for both inputs. The input is sent to the inverting pin of the op-amp, which inverts the signal. Figure 9(a) the general configuration of an inverting op-amp.



(a)



(b)

Fig. 6 (a) Designed 4-stage op-amp circuit using double gate MOSFET, and (b) its output.

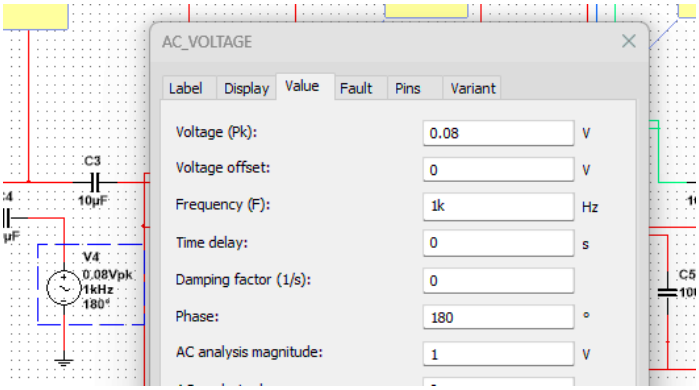
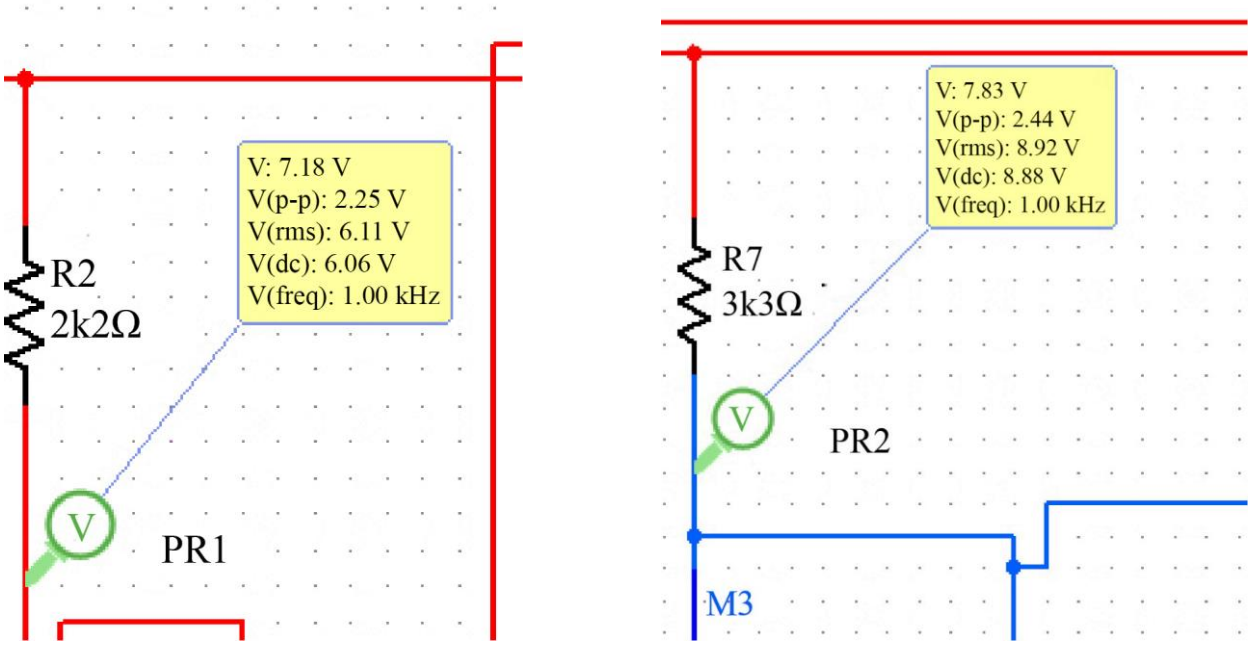
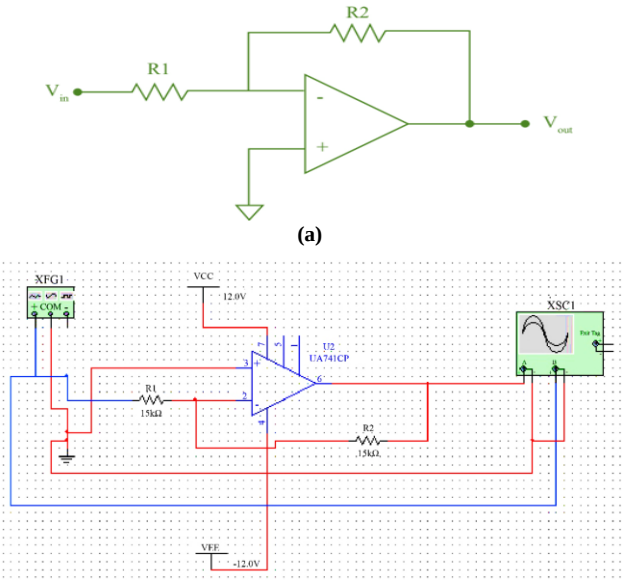


Fig. 7 Setting the phase shift for the input signal during the simulation



(a) **(b)**

Fig. 8 (a) Output from the differential amplifier, and (b) Another output from the 2nd stage (showing the increase in voltage)



(a)

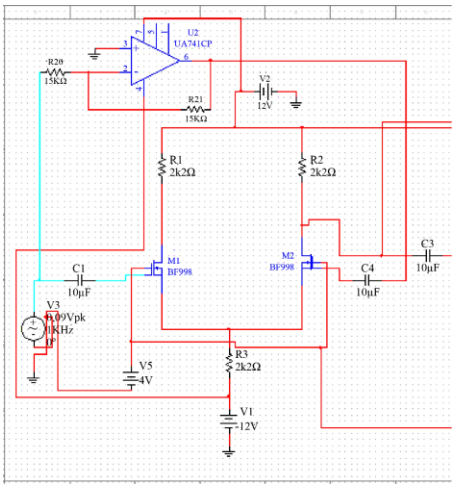
(b)

Fig. 9 (a) Basic configuration [17], and (b) Schematic of the inverting op-amp

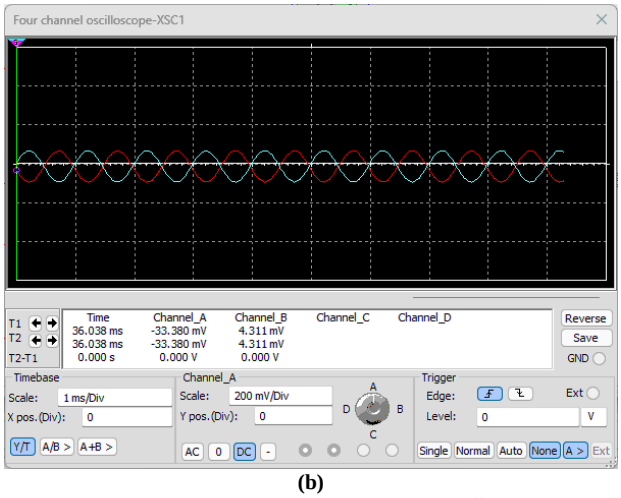
This is due to the working of the operational amplifier. The output voltage of the op-amp is determined:

$$V_{out} = -V_{in} \times \frac{R_2}{R_1} \tag{14}$$

If $R_1 = R_2$, then the circuit's gain will be 1. Thus, allowing to keep the same input voltage amplitude but with an inverted waveform. The schematic in Fig. 9(b) shows an inverting op-amp using the basic op-amp (the LM741) [43, 44]. The circuit is used to invert the input signal coming into the differential stage. This is needed to ensure the input signals were *180º* out of phase. This provides the best input as there should be no loss due to common mode signals—the function generator used during the testing of the circuit allowed for a single waveform only. Thus, the inclusion of the inverting op-amp allows for the signal, going to the first DG MOSFET at the differential stage, to be inverted before going to the second DG MOSFET in the differential stage, such as $V_{out} = -0.08 \times \frac{1K}{1K}$= - 0.08 V.



(a)



(b)

Fig. 10 (a) The inverting op-amp is used with the differential amplifier stage, and (b) Outputs of the normal signal and the inverted signal

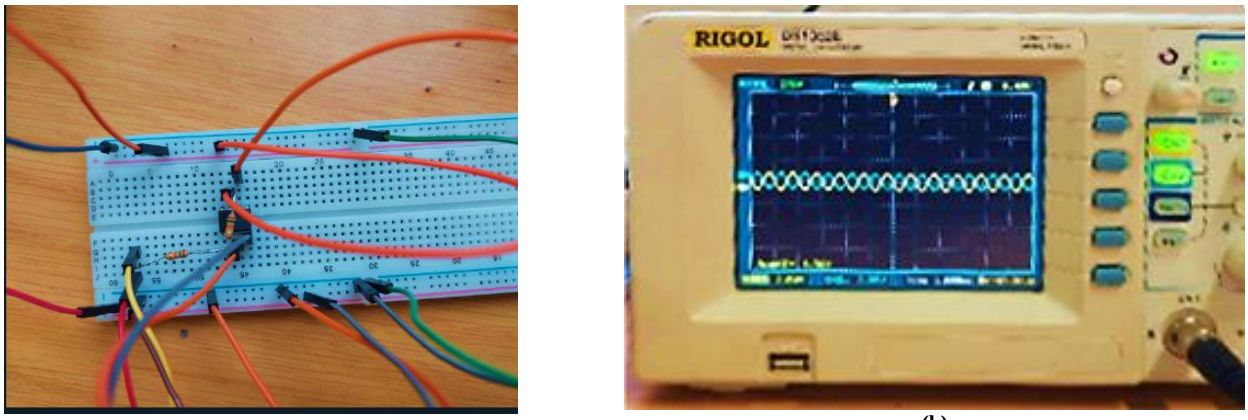
Fig. 10(a) shows the inverting op-amp being connected with the main solution; here, the output of the inverting op-amp is sent to the second DG MOSFET in the differential stage. The expected output of the inverting op-amp circuit is shown in Fig. 10(b). The input signals are going to the gate 1's of the DG MOSFETs that make up the differential stage. It can be seen in the simulated output that the waveforms are *180º* out of phase.

5. Prototype Design and its Analysis

The implementation of the full system has been designed as a prototype. A 4-stage op-amp device with the DG MOSFET has been designed to allow for isolated testing of the individual stages. The breadboard circuit has been designed in compliance with highlighted requirements with regard to drilling sizes, track sizes, and the overall circuit size. Connections have been made for the 4-stage op-amp and its associated component and equipment, according to Fig. 11 and Fig. 12, at various stages [45-47]. A prototype of the differential stage of the 4-stage operational amplifier using a DG MOSFET has been designed as in Fig. 11(a), with the input signals that are applied to the differential stage. Its output waveform is shown in Fig. 11(b), where the yellow waveform is from the function generator, and the blue waveform is the output from the inverting op-amp circuit.

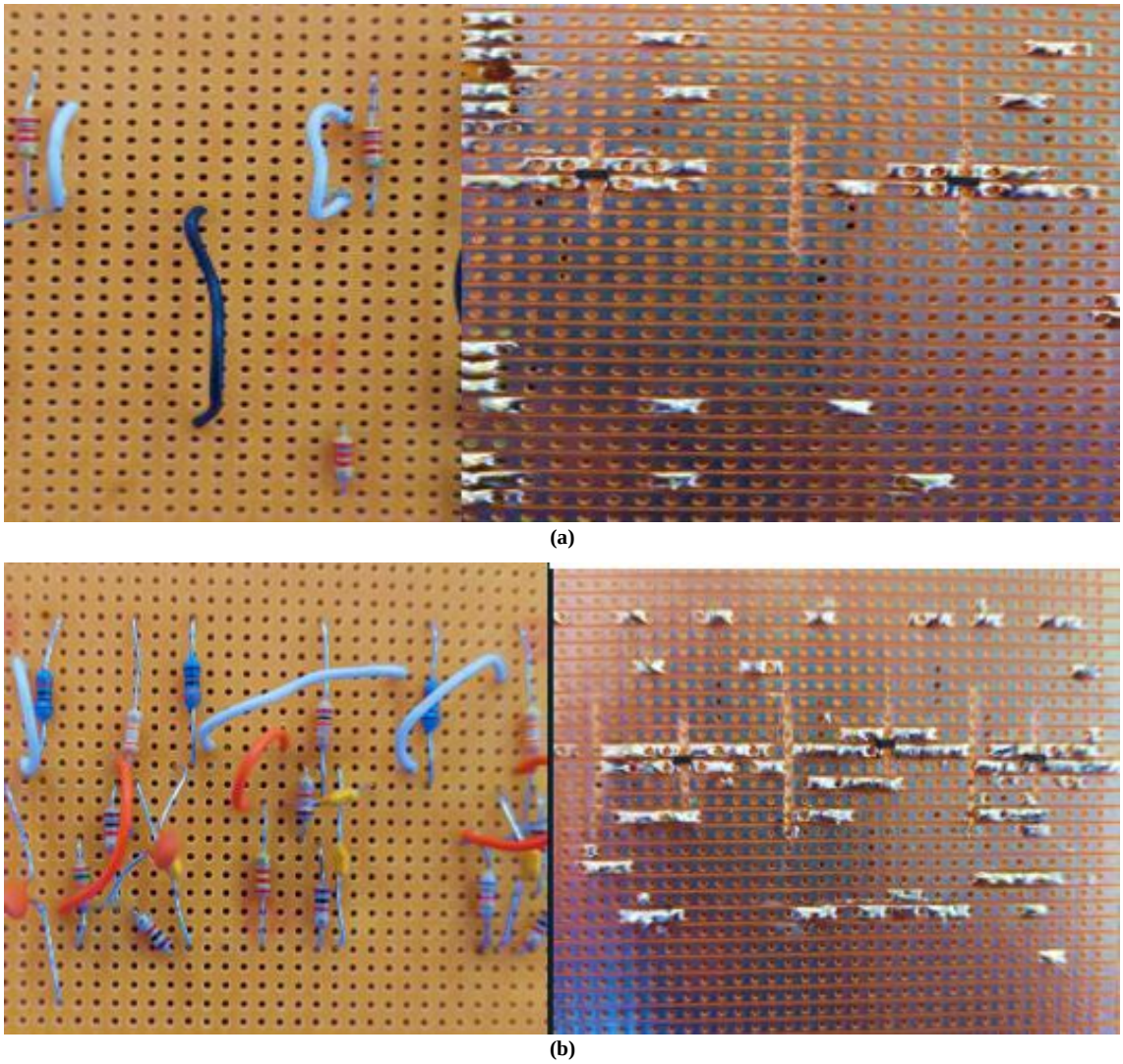
Fig. 12 shows the design methodology of the 4-stage op-amp at the different stages with a view of both sides of the prototype board. The DG MOSFET used are surface mount components. This was soldered underneath the strip prototype board. A line is drawn, which is then used to create isolation between the pins of the BF998 [46-48]. This is required since the strip board would automatically connect the pins on the same line together. Once isolation was established, the DG MOSFETs were soldered while ensuring the pins remained isolated. Figure 13(a) shows the designed prototype; the stages go from right to left. The differential stage uses the black wire to connect the source gates of the two BF998 MOSFETs that create the

differential stage to the negative rail through the 2k2 Ω resistor. When building the circuit, the use of white wire was used to connect all gate-2 of the BF998 MOSFETs to the 5 V power supply line. This connection to the 5 V enables the BF998 to remain in the saturation region. The orange wire was used to make the connection between the various stages. The green connector terminals on the far right are used for the different Vcc and ground rails.



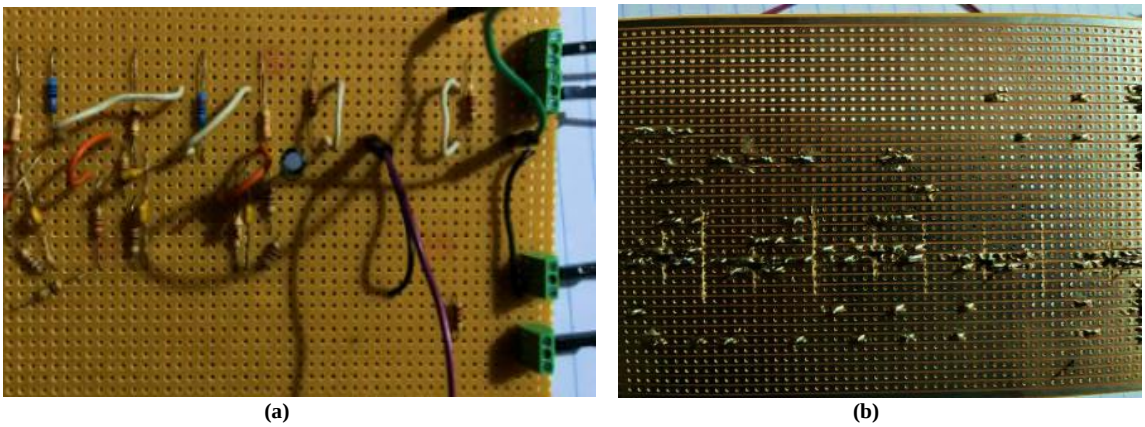
(a) **(b)**

Fig. 11 (a) Prototype of the inverting circuit, and (b) Output with input and inverted signal.



(a) **(b)**

Fig. 12 Prototype of the (a) differential stage and (b) Stages 2 to 4 of the 4-stage op-amp.



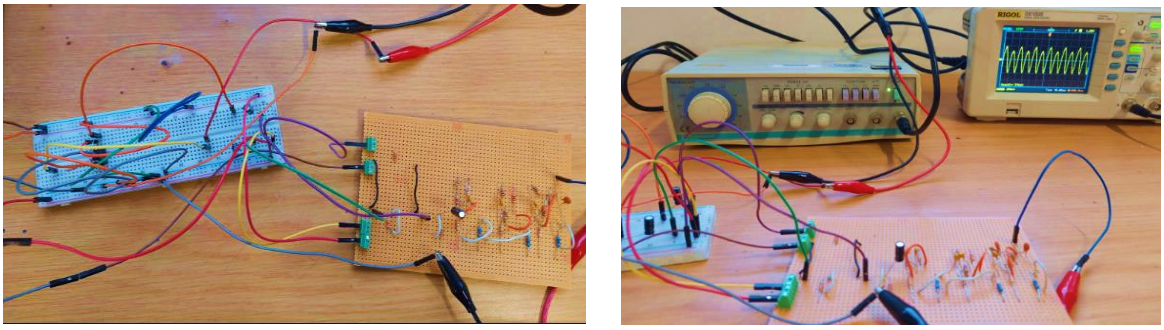
(a) (b)

(c)

Fig. 13 Prototype (a) Top view, (b) Bottom view, (c) fabricated structure of the 4-stage op-amp using DG MOSFET

Figure 13(b) shows the bottom view of the prototype board with connections. The way the Veroboard is set up allows all the connections on the same line horizontally to be connected. The fabricated layout (Fig. 13(c)), where the under-printed part of the board is used for connecting gate-2 to the 5 V, required keeping the MOSFET in the saturation region for amplification. Fig. 14 shows the voltage the circuit is supplied with from the voltage supply; the split rail supply within the simulation is ±12 V, where the power supply is giving a +12.03 V and -11.24 V. The voltage to gate-2 is 5.11 V. This will keep the MOSFET in the saturation region to create a more stable channel.

Fig. 14 Voltages for the power supply needed by the circuit



(a) (b)

Fig. 15 (a) Inverting op-amp being connected with the 4-stage op-amp, and (b) Its output testing

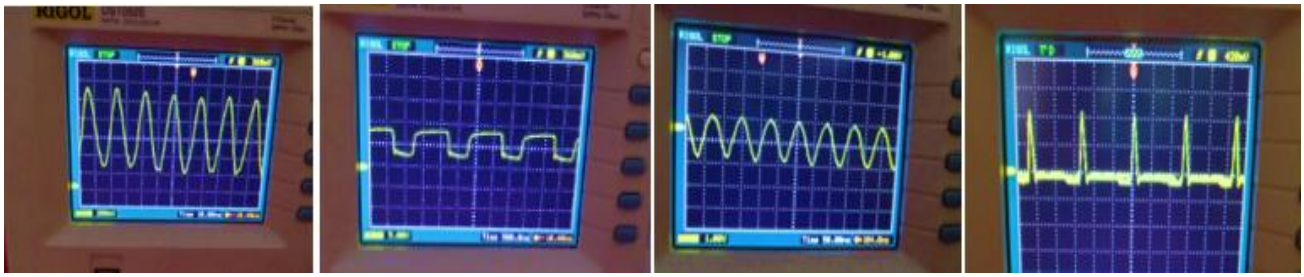


Fig. 16 Outputs of the different stages (stage-1 output on the left to final output on the right)

Figure 16 shows the output achieved at the various stages. Looking at the produced waveforms from left to right. Where left is the output of the differential stage (the 1st of the 4 stages), the waveform's amplitude has increased. The output of the 2nd stage is clipped. This is due to the amplifier reaching saturation. The final output is seen to saturate the Vcc supply. This is due to the input voltage being high. Inputting a smaller input voltage, such as those in the µV range, would allow more of a range for the amplified voltage at the different stages. The overall gain of the 4-stage op-amp has been determined by multiplying the gain of the individual stages. Common Mode Rejection Ratio (CMRR) has been calculated using the overall gain divided by the common mode gain. The differential stage has two types of gain: (i) common mode gain and (ii) differential mode gain. Overall gain has been determined using:

$$V_{out} = V_{in}A_{DM} + V_{in}A_{CM} \tag{15}$$

where A_{DM} and A_{CM} are the differentials and common mode gain, respectively. The CMRR value is the ratio between the differential and common mode gain. Taking the V_{out} 8.74 V, the common mode gain can be determined by:

$$A_{CM} = \frac{V_{out}}{V_{in}} - A_{DM} \tag{16}$$

$$A_{CM} = \frac{8.74}{0.08} - A_{DM}$$

Switching losses occur when the MOSFET turns-ON and OFF. This is because power dissipates when the MOSFET transitions between an ON-to-OFF or OFF-to-ON state occurs. The voltage loss is determined by looking at the expected output voltage via the calculations and the simulations. Taking this theoretical output voltage and looking at it against the measured output voltage. The variation in the voltages will give the voltage loss that has occurred throughout the circuit. The expected output voltage from simulation and calculations is *8.82 V*, whereas the measured output (from prototyped) voltage is close to this simulated voltage of 8.74V. Therefore, the voltage loss will be V_{loss} *= 8.82 V - 8.74 V= 0.08 V*.

The slew rate is also related to the recovery time. The change in the output of the op-amp is limited by a certain amount of time. When the slew rate is too high, it can distort the output. The slew rate is determined using Slew rate $= 2 \times \Pi \times f \times V$, where f is the frequency, and V is the peak voltage. Therefore, using this, the slew rate is at least *0.0549 V/µs*.

6. Conclusion and Future Recommendations

The designed 4-stage op-amp using a DG MOSFET is a viable solution for high-performance applications. It provides stable output with low noise. This design amplifies the voltage consistently through the 4 stages. The tested result matched the simulated/theoretical analysis. The acheived voltage loss is *0.08 V*, and the slew rate is *0.0549 V/µs*, which are suitable for nanoelectronic device applications.

In this work, one of the reasons for the voltage loss could be the variations of the external components (resistors and capacitors) from their value used during the simulation. To resolve this issue, other types of components can be used in the future. Also, there are losses due to energy conversion, where the electrical energy is converted to heat energy, such as heat energy that would be present in the resistors. This heat can impact the total losses experienced at the circuit's output. To resolve this issue, this DG MOSFET can be replaced with various other structures such as MultiGate MOSFET, FinFET, CSDG MOSFET, etc.

Author Contributions

Conceptualization, JTR and VMS; methodology, JTR; software, JTR; validation, JTR and VMS; formal analysis, JTR; investigation, JTR; resources, JTR; data curation, JTR and VMS; writing—original draft preparation, JTR; writing—review and editing, VMS; visualization, JTR; supervision, VMS; All authors have read and agreed to the published version of the manuscript.

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