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Original Article

Design and Implementation of Digital Low Pass FIR and IIR Filters Using VHDL for ECG Denoising

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Abstract *- ECG (electrocardiogram) signals are affected by different noise sources, such as Baseline Wander, EMG interference, and power line noise. These noise sources affect the reliability of diagnoses in the medical field. Digital filters can be used to remove these noises. In this paper, digital low pass FIR (Finite Impulse Response) and IIR (Infinite Impulse Response) filters are designed using VHDL to reduce high frequency and power line noises from ECG signals. Xilinx ISE Vivado 2015.2 tool is used to design and implement various FIR and IIR filters for ECG denoising. FIR filter of order first, third, tenth, and IIR filter of order first, second, third, fourth, and tenth are selected for ECG denoising. In this research,16- bit Carry Increment Adder (CIA) based on Ripple Carry Adder (RCA) is proposed for building adder circuits and an 8X8 vedic multiplier circuit is used for building multiplier circuits in FIR filters for improving area, speed, and power consumption. Synthesis results are used for evaluating the performance of FIR and IIR filters for ECG denoising. MATLABR2023a tool is used for displaying ECG signal waveforms and for calculating filter coefficients.*

Keywords *- FIR, IIR, VHDL, CIA, Vedic, ECG.*

1. Introduction

The QRS segment of the ECG signal gets distorted due to high-frequency muscular contraction noise and power line interference [1]. Most abnormality information related to the heart is occupied in the QRS segment. Frequency range of 0.5Hz to 100 Hz contains important information in the ECG signal [2]. Filtering of the ECG signal is required for correct diagnosis. As digital filters are more accurate and precise compared to analogue filters, they are widely used to remove noise from ECG signals. FIR and IIR are important digital filters. In this paper, low-pass window-based FIR and Butterworth-based IIR filters of various orders are designed and implemented for nose removal from the ECG signal, and their performance is compared in terms of area, speed, and power results. In the last fifteen years, many researchers have been working on ECG denoising by using digital filters. Kaustubh Gaikwad and Mahesh Chavan [3] have used the IIR digital Butterworth filter to remove noise from the ECG signal. In this research, an IIR filter of order 2 is designed using a Matlab tool and implemented in a Xilinx system generator. A well-designed filter shows good filtering response and provides better performance in terms of area, speed, and power. Authors in paper [4] have designed Butterworth, Notch, and Chebyshev type II IIR filters for removing power line interference from the ECG signal. In this work, the original ECG signal is taken from the MIT-BIH database, and 50 Hz power line interference is added to the original ECG signal to generate a noisy ECG signal.

The Matlab tool is used to analyse the time and frequency domain properties of noisy and filtered ECG signals. This research proved that the Notch IIR filter performed better than other IIR filters for removing power line interference from the ECG signal. Ms. Chhavi Saxena et al. [5] have used FIR and IIR digital filters to remove high- and low-frequency noise from the ECG signal. This research shows that the FIR filter gives more accurate results compared with the IIR filter. In the paper [6], the authors have done an analysis of different types of FIR and IIR filters by using coefficients of various transform methods. In this research, the original ECG signal is mixed with AWGN noise, and then various transform methods are applied to the noisy ECG signal. After this, coefficients of various transforms FIR and IIR filters of different orders are applied to do filtering and the performance of filters is compared based on time consumption and order of the filter. V. Vittal Reddy et.al [7] have implemented window techniques based on minimum order FIR and IIR filters to match fixed specifications for ECG signal. In this work, FIR and IIR filters used different sampling frequencies for doing comparison for processing ECG signals. Jayashree S et.al [8] have used an 8-Tap FIR filter using peer reversible logic gates for ECG denoising.In this work, low power consumption for the proposed 8-Tap FIR filter is achieved by using Vedic multiplier and carry adder architectures. Speed is improved by using reversible logic gates in FIR filter architectures.

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FIR filter is designed using Matlab software and implemented in FPGA (Field Programmable Gate Array) by using Verilog HDL language. Implemented FIR filter performed better with existing architectures in terms of Mean Square Error and Signal to Noise Ratio. M. Sumalatha et al. [9] proposed a vedic design - Carry Lookahead Adder FIR filter architecture for ECG denoising. Here, by using Matlab software, the ECG signal is read from the arrhythmia database, and then White Gaussian Noise is added to this ECG signal.Then, this noisy signal is converted to a binary text file for doing filtering. Verilog HDL language is used to read the text file and do filtering, and the filtered output is written in a text file. K. Sravan Kumar et al. [10] have implemented FIR and IIR filters of different methods to remove noise from ECG signals. FIR filter of orders 56, 300, 450, and 600 and for IIR filter of orders 1, 2, and 3 are taken to perform the experiments. Here, experimentally, it was found that the FIR filter of order 56 based on the Kaiser Window method performs better than other filters.

Manoj et al. [11] have used Matlab software to implement FIR and IIR filters of different window techniques to remove baseline noise from ECG signals. In this work, a wavelet transform is applied to a filtered signal to refine the signal. For performance analysis, power spectral density and average power are compared for filters of different window techniques. Navdeep Prashar et al. [12] studied different existing techniques to develop biomedical systems. Also, the authors in this work have implemented different low-pass IIR filters to remove Electromyography noise from the ECG input signal. Signal-to-noise ratio and power spectral density are considered for performance comparison among different low-pass IIR filters for noise removal from the ECG signal.

V. Supraja et al. [13] have used Wavelet transforms, Fuzzy logic, FIR filtering, and empirical mode decomposition to denoise ECG signals that are corrupted by various noise sources. Saumendra Behera et al. [14] have implemented a fixed window technique method for filtering ECG. The signal-to-noise ratio, mean square error, and PRD are used to evaluate the performance of different filters. Ngoc-Thang Bui and Gyung-su Byun [15] have used an IIR and symmetric FIR filter to compare the properties of the ECG signal at different sampling frequencies. MIT/BIH database was used to conduct the experiment. Kavita Baghel and Brijendra Mishra [16] combined the FIR and IIR filters to remove random noise from the nosy signal. They used Matlab software for simulation. Gandham Sreedevi and Bhuma Anuradha [17] have implemented FIR and IIR filters for removing baseline noise from the ECG signal. They have also done a performance comparison among filters for proper understanding and display of the ECG signal. A. I. Al-Shueli [18] used FIR and IIR filters to remove high- and low-frequency noise from the ECG signal. From the experimental results, this author found that the FIR filter performs better than the IIR filter. Mahesh S. Chavan et al. [19] have used an equivalent FIR notch filter to remove power line interference from the ECG signal. MA Mneimneh et al. [20] have used an adaptive Kalman Filter to remove Baseline Wandering interference from the ECG signal. To conduct the experiment, the authors used the PTB Diagnostic ECG database. In this research, sample ECG inputs are taken in text format from the www.fpga4student.com website, and modified FIR filters of various orders and IIR filters of different orders are implemented by using the Xilinx Vivado 2015.2 tool for reducing high-frequency and power line noises from the ECG signal.

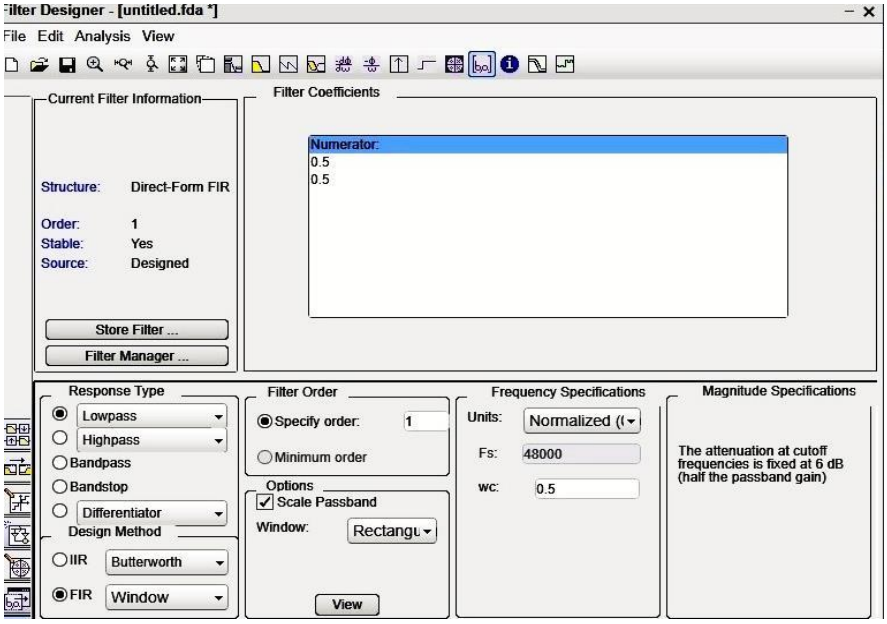

Fig. 1 FIR filter 1st order filter coefficients calculation by using Matlab FDA tool

2. Proposed FIR and IIR Filter Architectures for ECG Denoising

FIR and IIR filters are commonly used filters in the field of digital signal processing applications. FIR filter is recursive and always stable FIR filters consume more amounts of memory and arithmetic operations as compared with IIR filters. In this paper, the Digital low pass window-based FIR filter of orders 1st, 3rd, and 10th order and the Butterworth-based IIR filter of orders 1st, 2nd,3rd,4th, and 10th order are designed using VHDL.

For calculating coefficients of FIR and IIR filters, the MATLAB FDA tool is used [22, 23]. FIR and IIR filter equations are written below.

$$y(n)=\sum_{i=0}^{N} \boldsymbol{b_i x(n-i)} \quad (2.1)$$

$$y(n)=\sum_{i=0}^{N} \boldsymbol{a_i\ x(n-i)} - \sum_{i=1}^{N} \boldsymbol{b_i\ y(n-i)} \quad (2.2)$$

Equation (2.1) represents the FIR filter equation, and Equation (2.2) represents the IIR filter equation; in this equation, N represents filter order, and a_i and b_i represent filter coefficients.

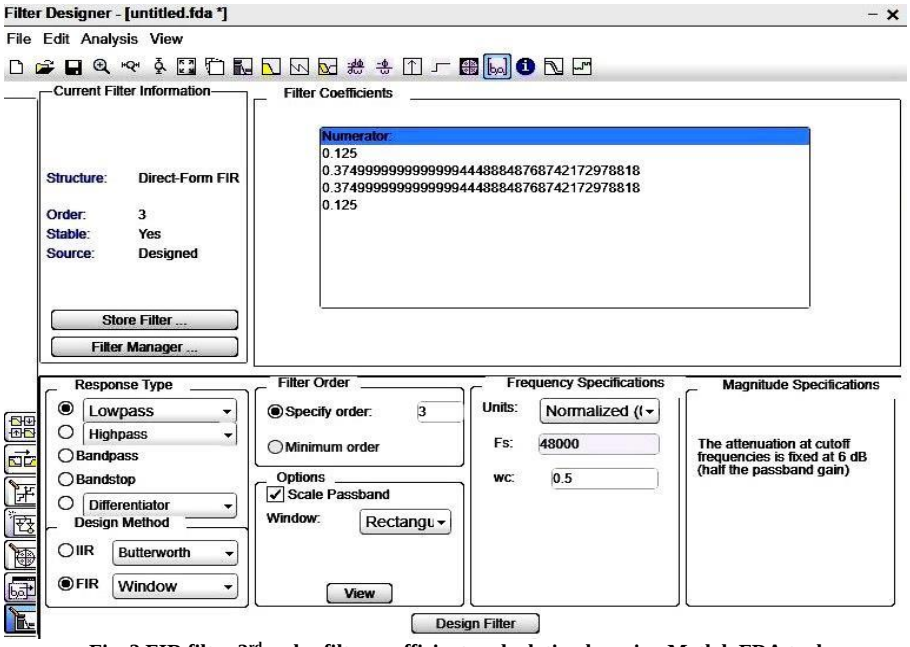

Fig. 2 FIR filter 3rd order filter coefficients calculation by using Matlab FDA tool

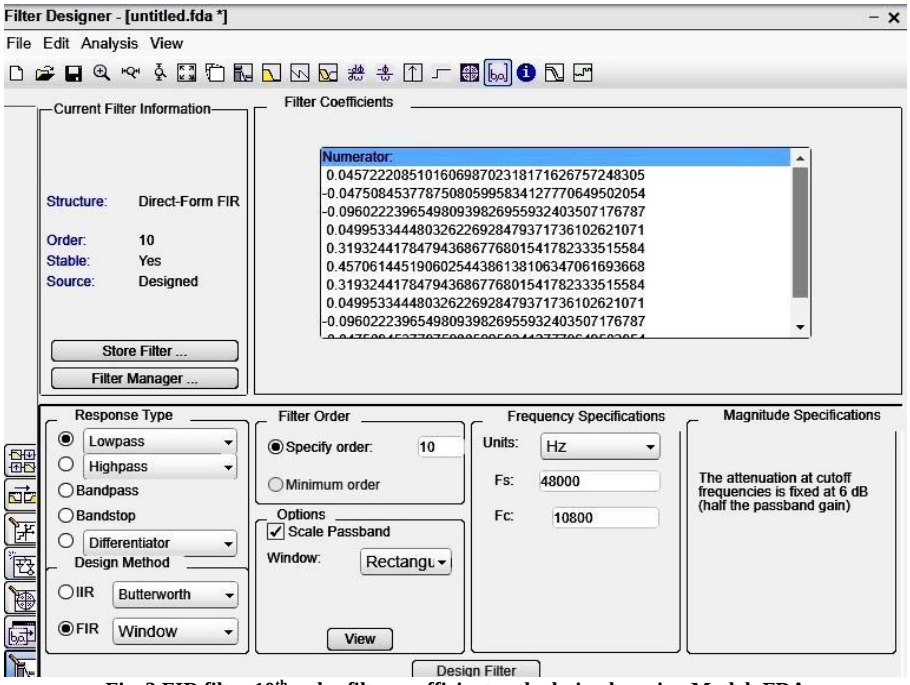

Fig. 3 FIR filter 10th order filter coefficients calculation by using Matlab FDA

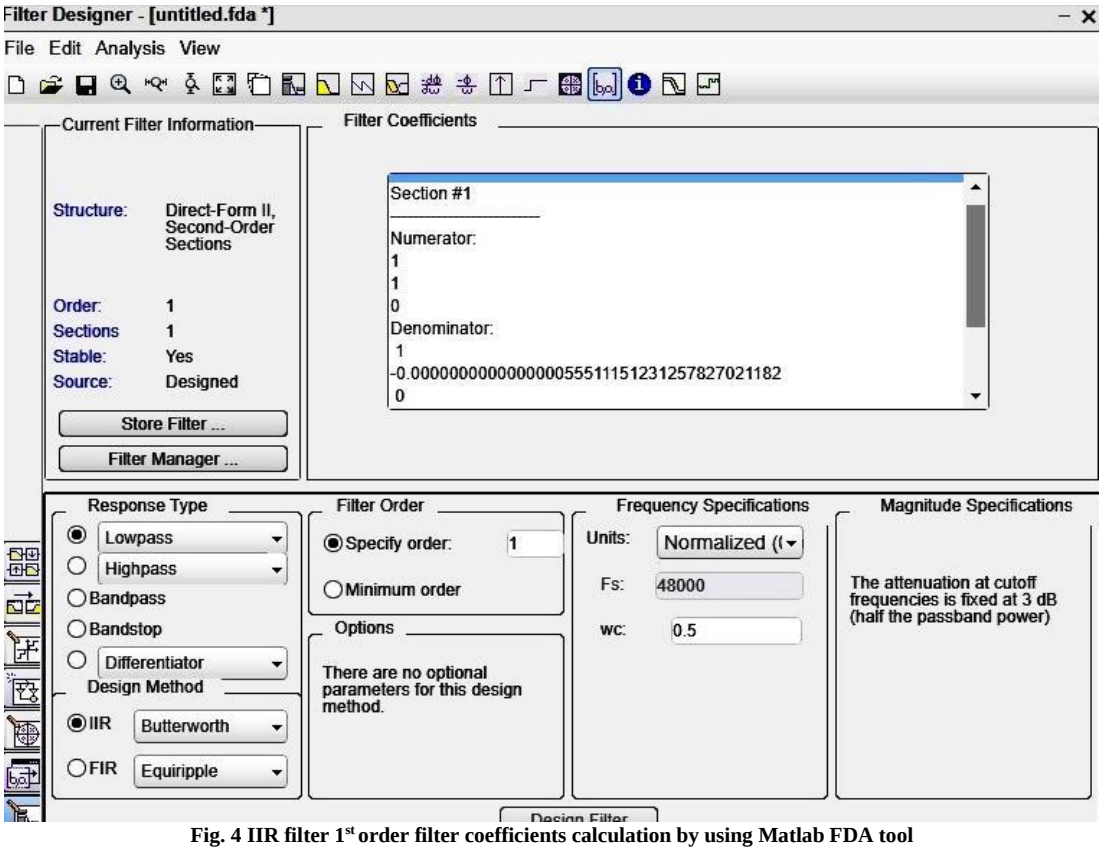

Fig. 4 IIR filter 1st order filter coefficients calculation by using Matlab FDA tool

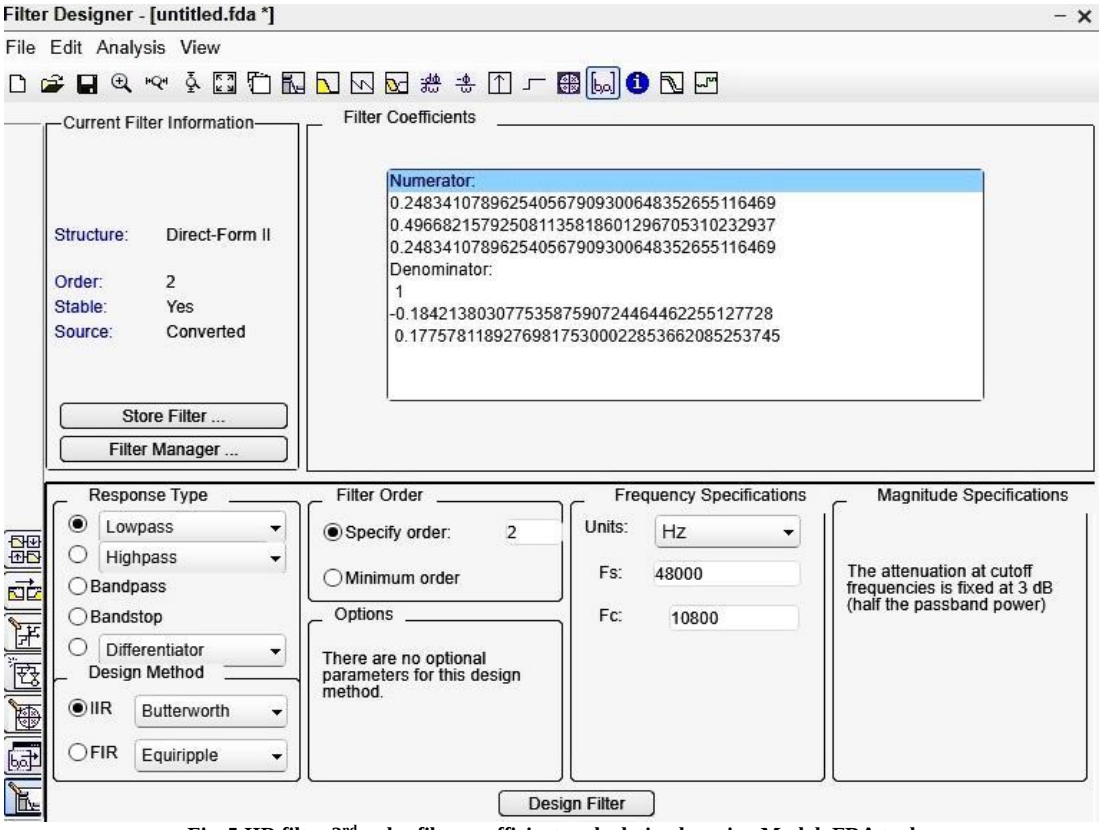

Fig. 5 IIR filter 2nd order filter coefficients calculation by using Matlab FDA tool

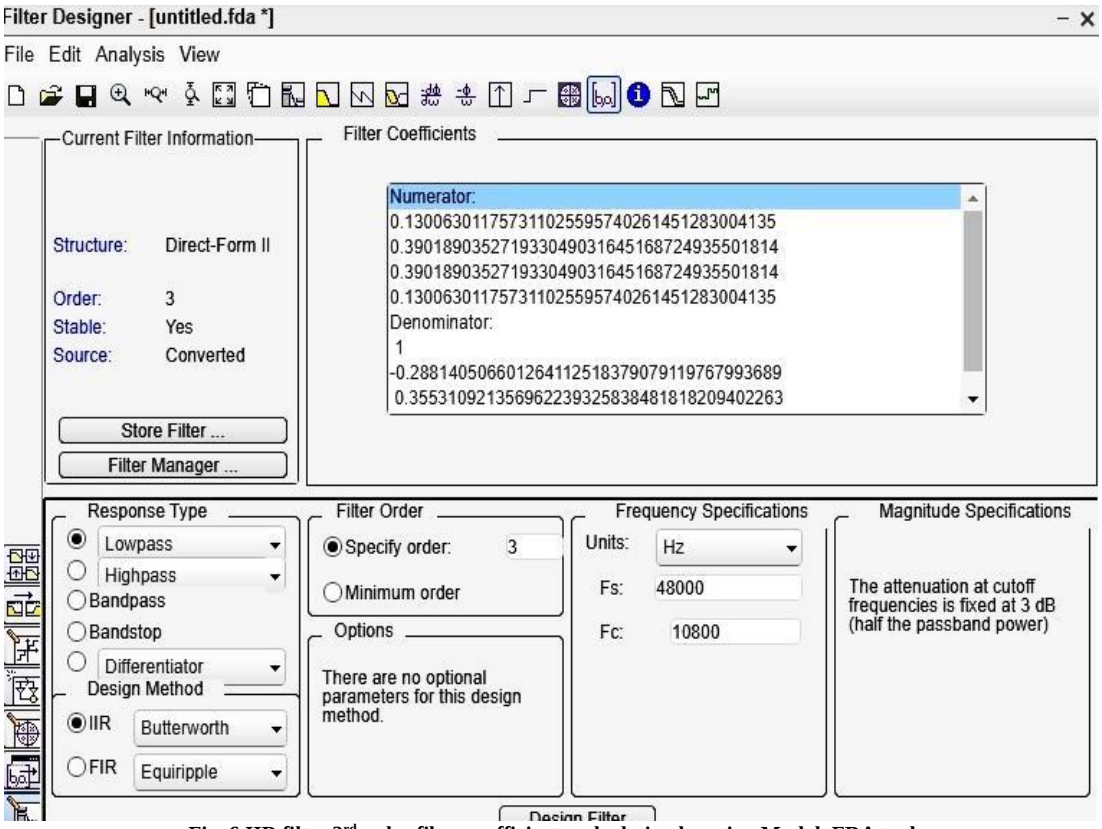

Fig. 6 IIR filter 3rd order filter coefficients calculation by using Matlab FDA tool

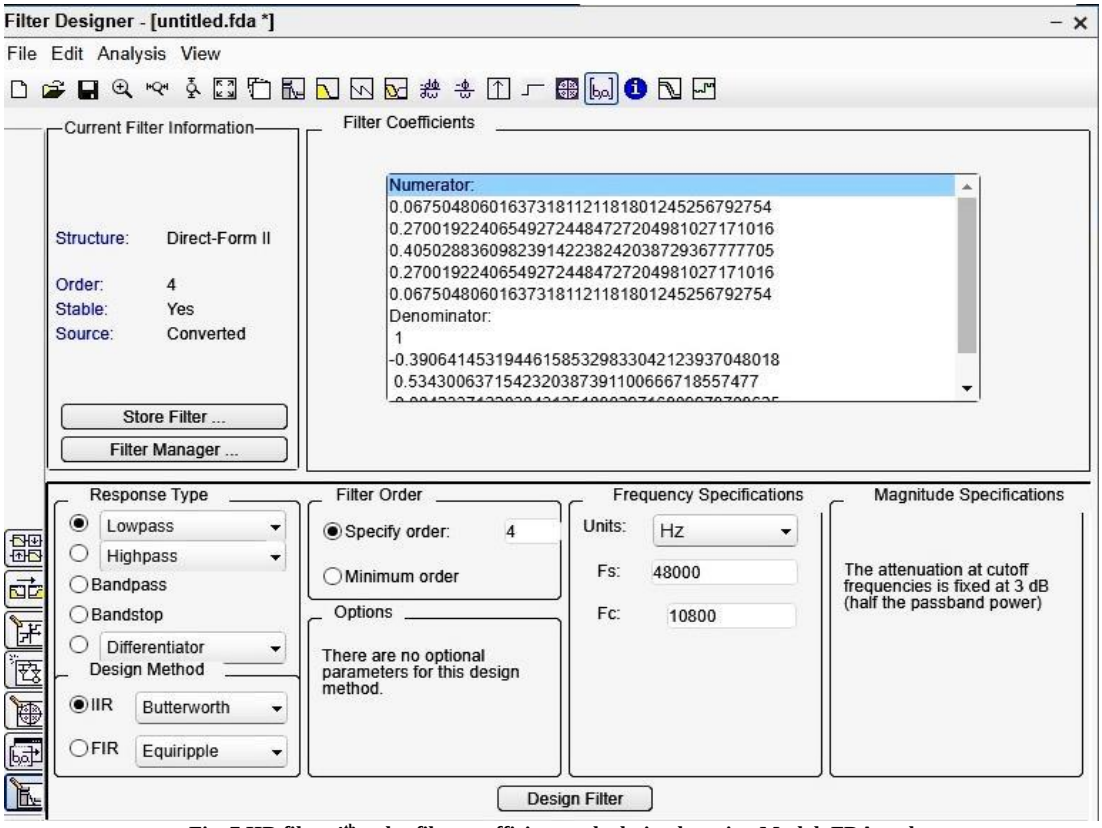

Fig. 7 IIR filter 4th order filter coefficients calculation by using Matlab FDA tool

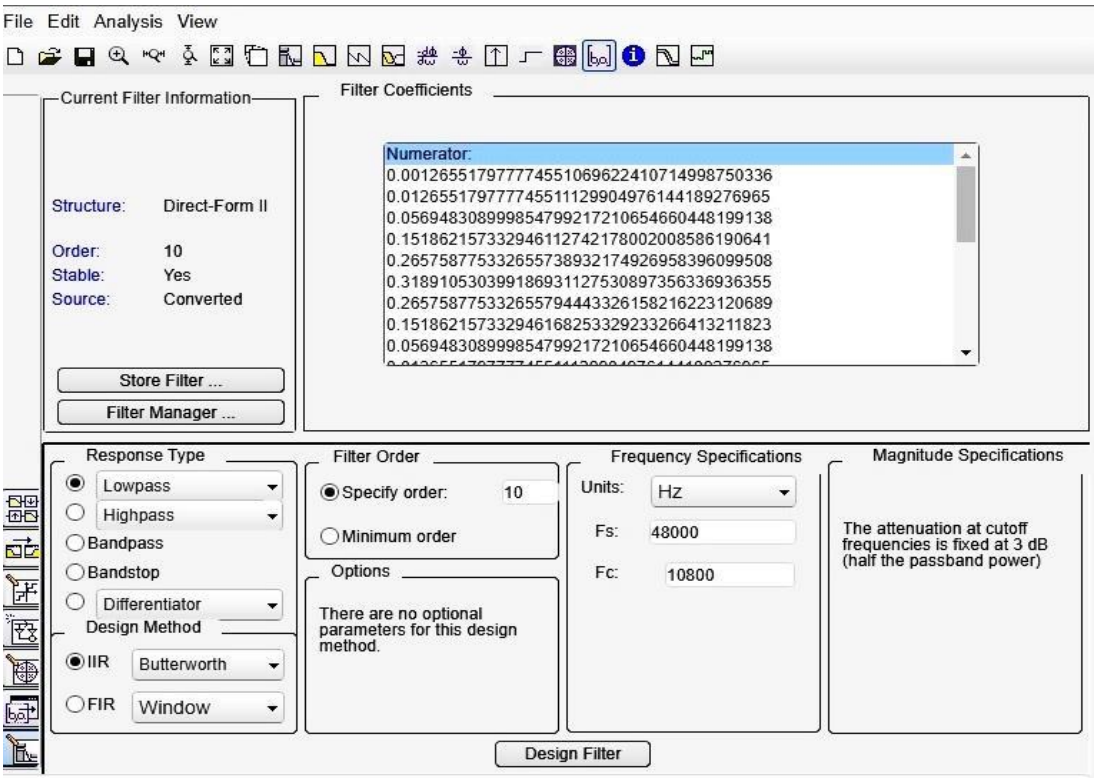

Fig. 8 IIR filter 10th order filter coefficients calculation by using Matlab FDA tool

Figure 1, Figure 2, and Figure 3 represent the FIR filter design window of the Matlab FDA tool for calculating filter coefficients for orders 1st, 3rd, and 10th. Figure 4, Figure 5, Figure 6, Figure 7, and Figure 8 represent the IIR filter design window of the Matlab FDA tool for calculating filter coefficients for order orders 1st, 2nd, 3rd, 4th, and 10th. Figure 9 represents the proposed 16-Bit Carry Increment circuit (CIA) diagram for improving the performance of the FIR filter. This circuit contains two 8-bit Ripple Carry Adder(RCA) for doing addition here, C_{int}(input carry) is always zero for both RCAs and output carry for the first RCA adder is fed to the input of the first half adder circuit.

In this circuit, the incremental circuit contains 8 Half adders(HA) and one OR gate. S_0, S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8, S_9, S_{10}, S_{11}, S_{12}, S_{13}, S_{14}, S_{15} represents final sum signals and C_{out} represents final output carry signal for the purposed 16-Bit CIA adder. Figure 10, Figure 11 and Figure 12 represent the circuit diagram for the FIR filter of order 1st,3rd and 10th order respectively. An 8x8 Vedic multiplier [24] is used to improve the performance of the FIR filter. Figure 13, Figure 14, Figure 15, Figure 16 and Figure 17 represent circuit diagrams for the IIR filter of order 1st, 2nd,3rd, 4th and 10th order, respectively.Calculated FIR and IIR filter coefficients are converted into Signed Integer coefficients to make the multiplication process simpler. Then, these filter coefficients are converted into Hexadecimal format and stored in a constant array for filtering operation.

In the FIR filter circuit diagram, x(n) represents an 8-bit input signal, y(n) represents a 16-bit output signal, DFF represents D Filp-Flop, and b_i represents filter coefficients. Similarly, in the IIR filter circuit diagram, x(n) represents an 8-bit input signal, y(n) represents a 16-bit output signal, DFF represents D Filp-Flop and b_i,a_i represents filter coefficients.

In IIR filter circuit diagrams, b_i coefficients are multiplied with output signal y(n) to generate 24 bits of data. These 24 bits of data are truncated into 16 bits in addition to generating the final output signal y(n).

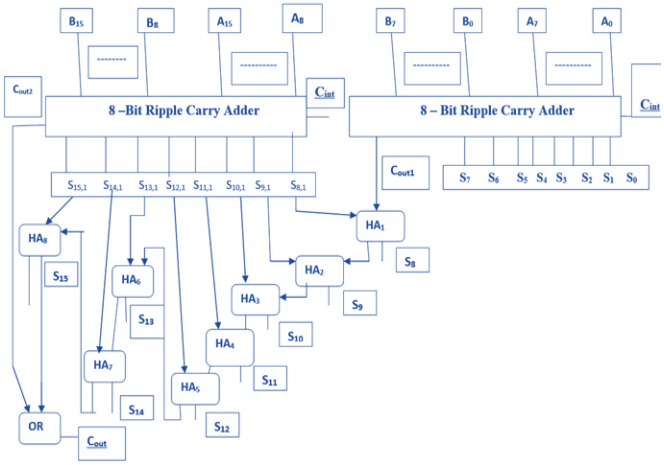

Fig. 9 Proposed 16-Bit carry increment adder circuit diagram

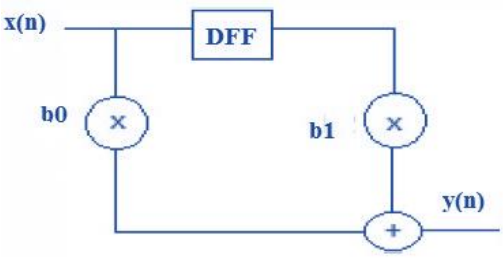

Fig. 10 FIR filter circuit diagram for 1st order

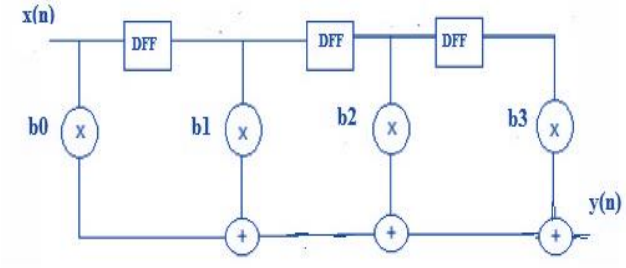

Fig. 11 FIR filter circuit diagram for 3rd order

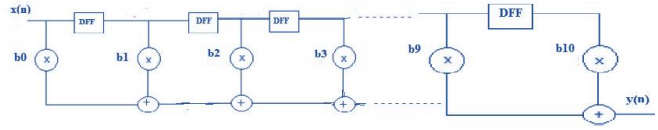

Fig. 12 FIR filter circuit diagram for 10th order

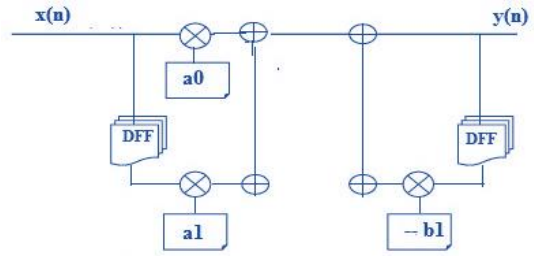

Fig. 13 IIR filter circuit diagram for 1st order

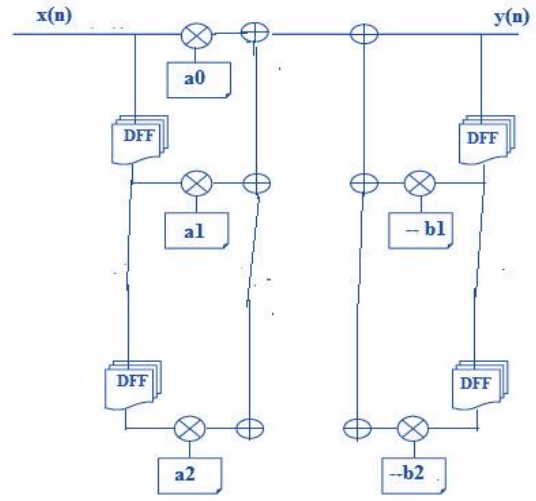

Fig. 14 IIR filter circuit diagram for 2nd order

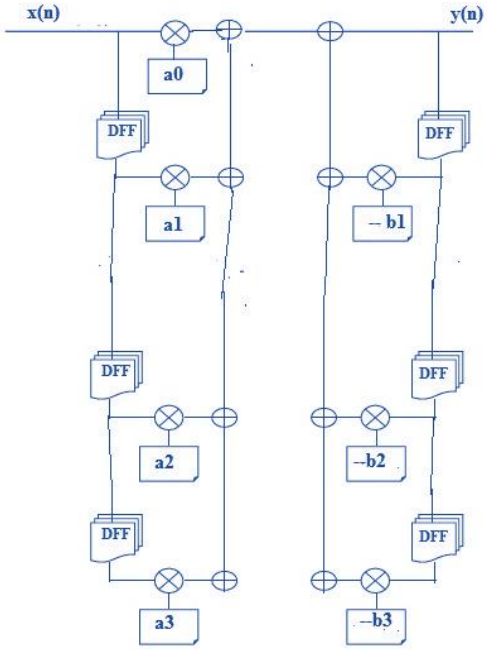

Fig. 15 IIR filter circuit diagram for 3rd order

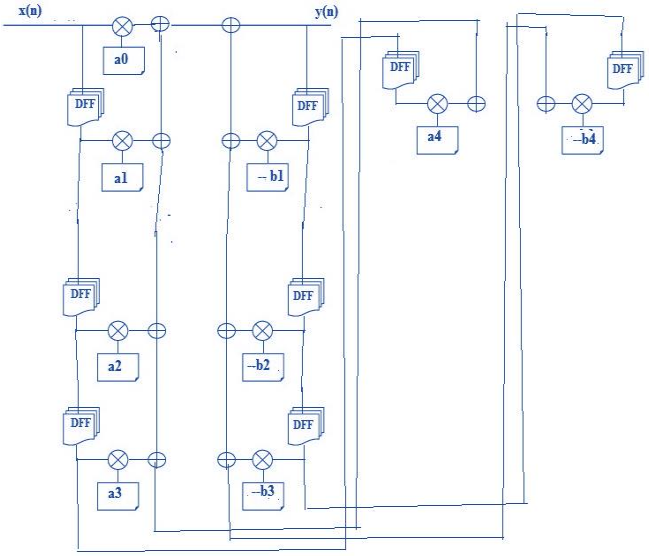

Fig. 16 IIR filter circuit diagram for 4th order

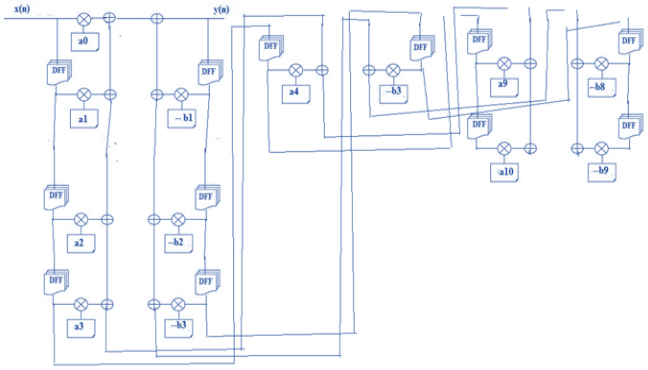

Fig. 17 IIR filter circuit diagram for 10th order

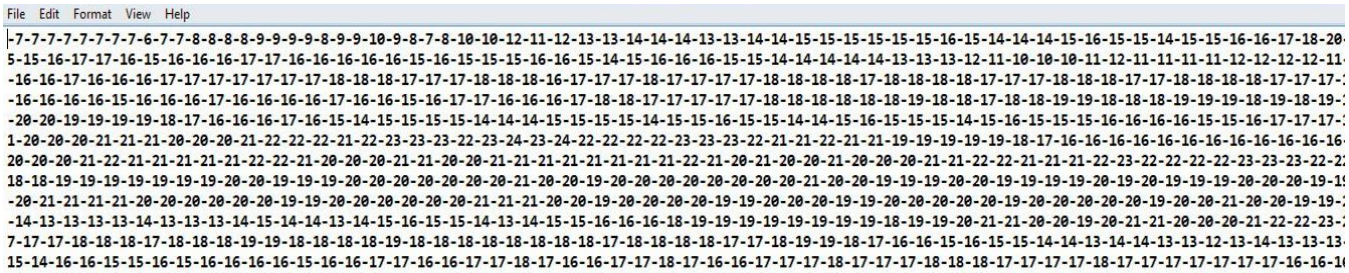

Fig. 18 Sample noisy ECG(text format) input taken from fpga4student.com websites for ECG denoising

3. Experimental Results and Discussion

In this research, various orders of FIR and IIR filters are designed by using VHDL (Very High-Speed Integrated Circuit Hardware Description Language) and Implemented on target Device 7a35t-cpg236 (Artix7 Series FPGA) by using Xilinx Vivado 2015.2 tool. Sample ECG noisy signal is taken from the www.fpga4student.com website.

For conducting the experiments for ECG denoising, ECG sample data of 8 bits are stored in a text file. This text file is read by the VHDL testbench program to do the filtering and 16-bit outputs are written by the VHDL testbench program and stored in a text file.

The Matlab tool is used to read the text file for noisy 8-bit ECG signals and 16-bit filtered ECG signals for drawing them graphically.

Figure 18 represents a sample ECG noisy signal in text format, and Figure 19 represents a sample noisy ECG signal plotted graphically using Matlab.

Figure 20, Figure 21, and Figure 22 represent filtered ECG signals by using the FIR filter of order 1st, 3rd and 10^{th,} respectively.

ECG signals filtered by IIR filter of order 1st, 2nd,3rd, 4th and 10th are shown in Figure 23, Figure 24, Figure 25, Figure 26 and Figure 27, respectively.

Figure 28, Figure 29, and Figure 30 represent the simulation waveform for the FIR filter of orders 1st, 3rd, and 10th, respectively.

In these figures, input and output signals are represented in signed format.

Simulation waveform for the IIR filter of order 1st, 2nd, 3rd, 4th and 10th are shown in Figure 31, Figure 32, Figure 33, Figure 34 and Figure 35, respectively.

In these figures, input and output signals are represented in signed format.

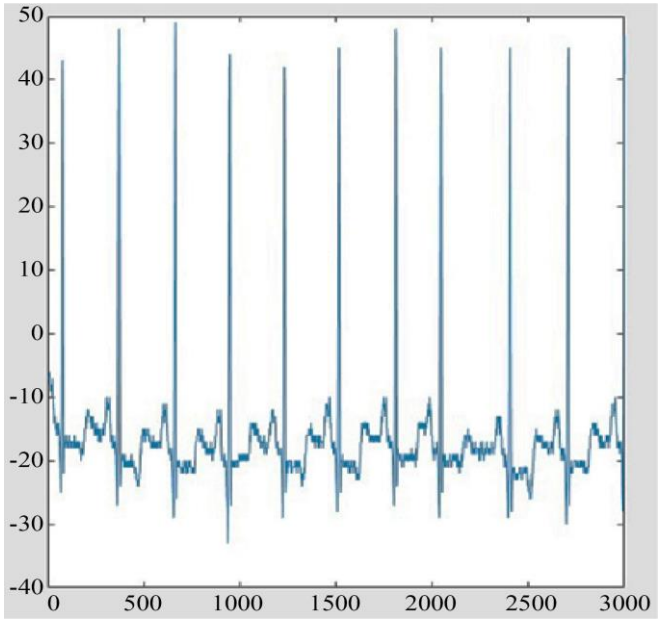

Fig.19 Sample noisy ECG(in graph format) input taken from fpga4student.com websites for ECG denoising

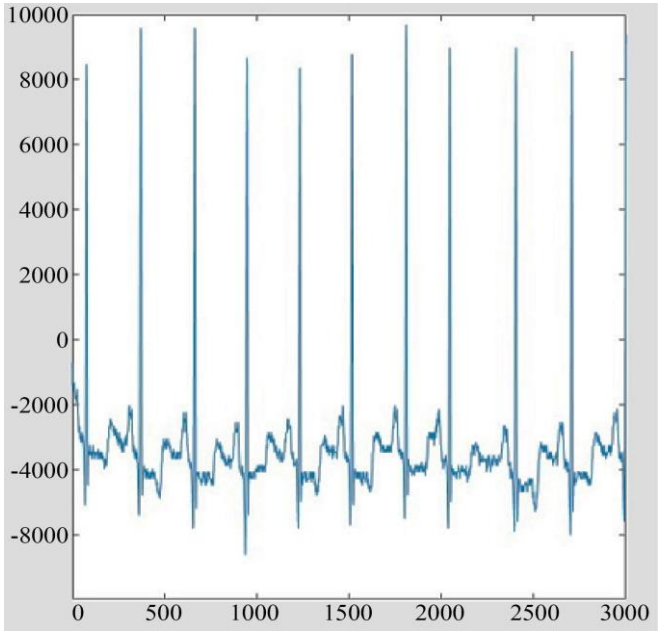

Fig. 20 Filtered ECG(in graph format) output for 1st order FIR filter

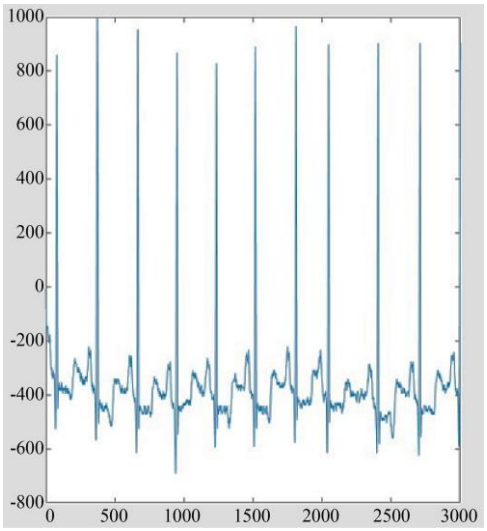

Fig. 21 Filtered ECG(in graph format) output for 3rd order FIR filter

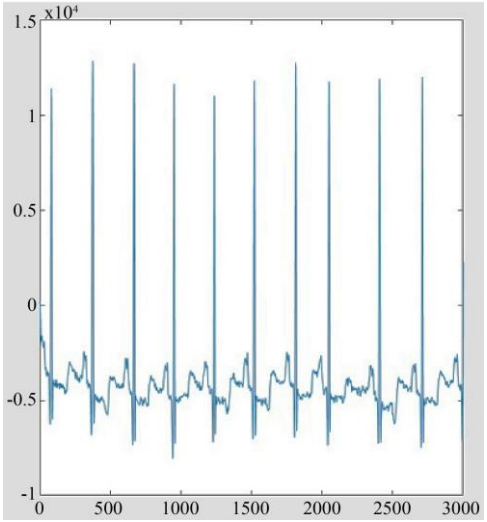

Fig. 22 Filtered ECG(in graph format) output for 10th order FIR filter

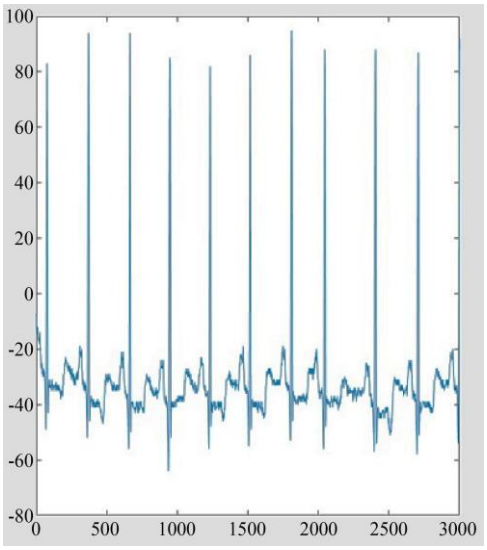

Fig. 23 Filtered ECG(in graph format) output for 1st order IIR filter

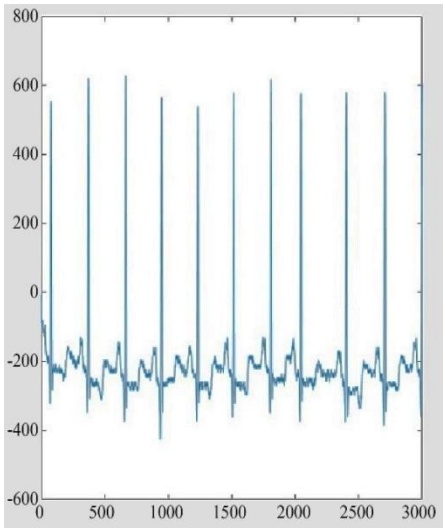

Fig. 24 Filtered ECG(in graph format) output for 2nd order IIR filter

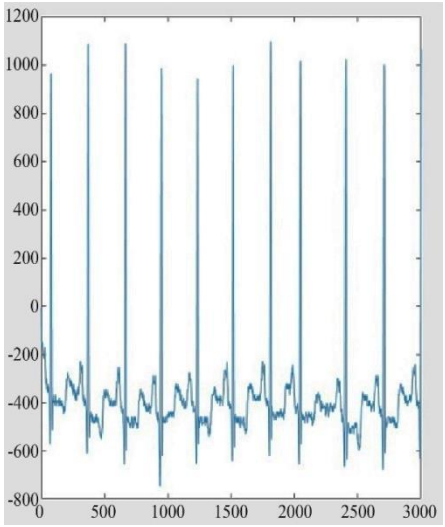

Fig. 25 Filtered ECG(in graph format) output for 3rd order IIR filter

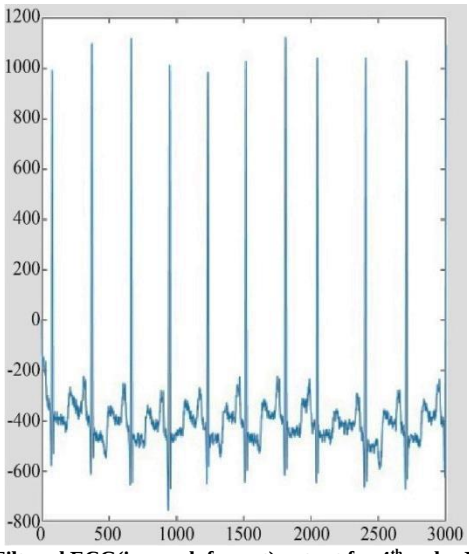

Fig. 26 Filtered ECG(in graph format) output for 4th order IIR filter

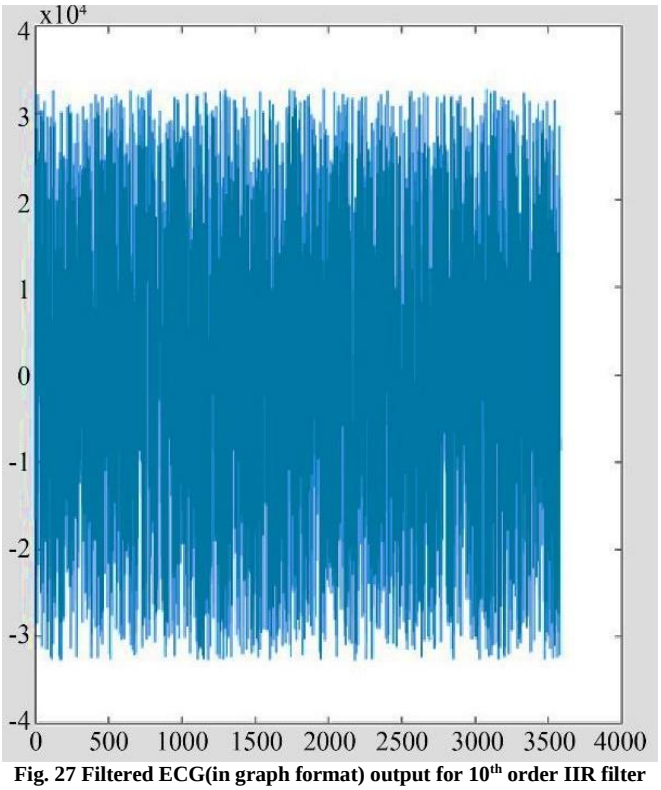

Fig. 27 Filtered ECG(in graph format) output for 10th order IIR filter

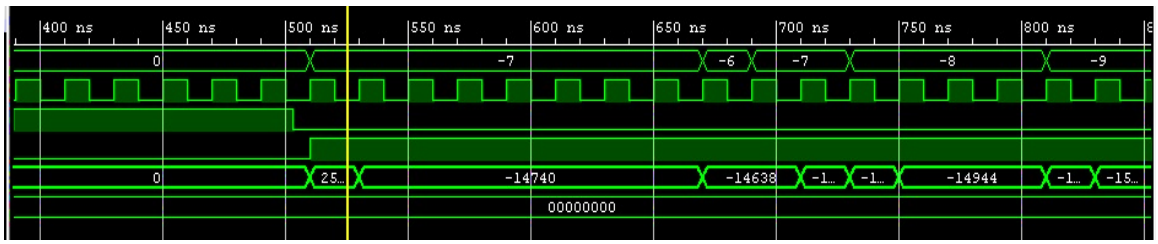

Fig. 28 Simulation waveform for ECG denoising by using 1st order FIR filter

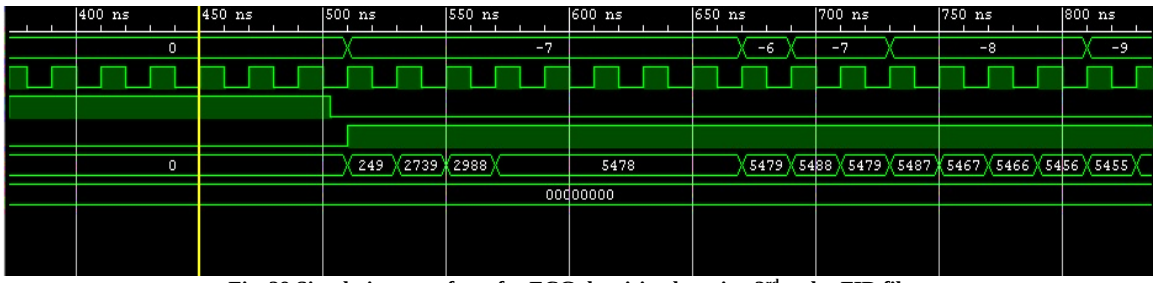

Fig. 29 Simulation waveform for ECG denoising by using 3rd order FIR filter

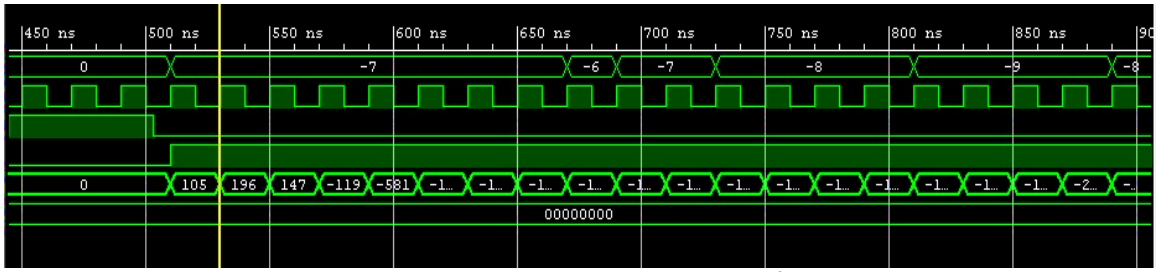

Fig. 30 Simulation waveform for ECG denoising by using 10th order FIR filter

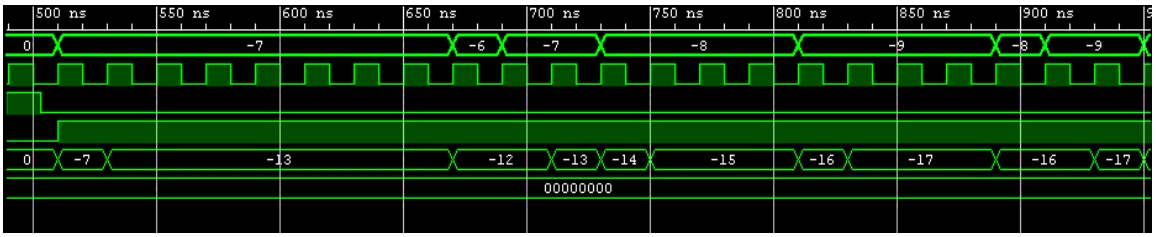

Fig. 31 Simulation waveform for ECG denoising by using 1st order IIR filter

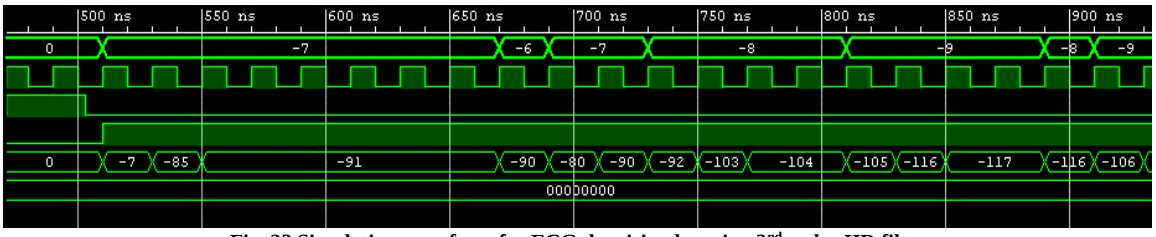

Fig. 32 Simulation waveform for ECG denoising by using 2nd order IIR filter

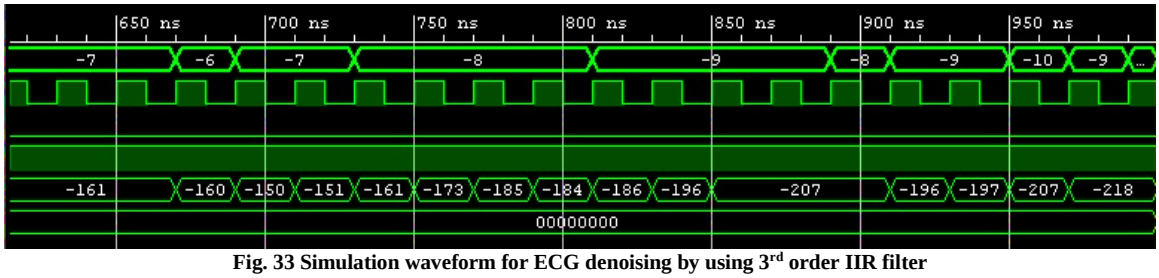

Fig. 33 Simulation waveform for ECG denoising by using 3rd order IIR filter

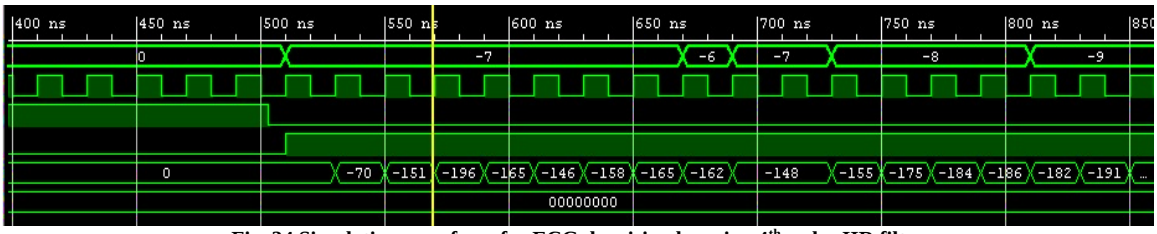

Fig. 34 Simulation waveform for ECG denoising by using 4th order IIR filter

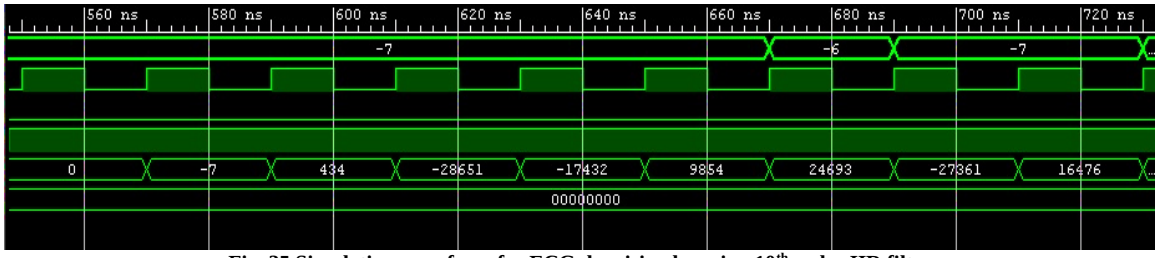

Fig. 35 Simulation waveform for ECG denoising by using 10th order IIR filter

Table 1. Synthesis results for the implemented FIR filters in Artix7 Basys3 FPGA

Implemented FIR Filter (in this work)	Area (LUT)	Delay (ns)	Power Consumption (Watt)
1st order FIR Filter	68	13.622	14.863
3rd order FIR Filter	44	13.622	15.436
10th order FIR Filter	322	25.427	20.704
1st order FIR Filter based on CIA adder and 8X8 vedic multiplier	68	16.155	14.863
3rd order FIR Filter based on CIA adder and 8X8 vedic multiplier	69	14.496	12.939
10th order FIR Filter based on CIA adder and 8X8 vedic multiplier	32	5.396	6.618

Table 2. Synthesis results for the implemented IIR filters in Artix7 Basys3 FPGA

Implemented IIR Filter (in this work)	Area (LUT)	Delay (ns)	Power Consumption (Watt)
1st order IIR Filter	10	10.346	10.298
2nd order IIR Filter	44	12.508	9.27
3rd order IIR Filter	149	14.421	16.152
4th order IIR Filter	159	15.844	13.471
10th order IIR Filter	272	17.394	19.136

Table 3. Synthesis results comparison among FIR filters in terms of area and speed

Implemented FIR Filter	Area(LUT)	Delay(ns)
1st order FIR Filter	68	13.622
3rd order FIR Filter	44	13.622
10th order FIR Filter	322	25.427
1st order FIR Filter based on CIA adder and 8X8 vedic multiplier	68	16.155
3rd order FIR Filter based on CIA adder and 8X8 vedic multiplier	69	14.496
10th order FIR Filter based on CIA adder and 8X8 vedic multiplier	32	5.396
Paper[18]	1214	
Paper[25] 8 –Tap LC-CSLA-FIR	184	8.66
Paper[26]	5766	
Paper[27] 182 order FIR Filter	774	
Paper[28] 2-Tap FIR Filter (Virtex-4 (XC4VFX12))		22.924
Paper[28] 2-Tap FIR Filter (Virtex-5 (XC5VLX110T))		16.841
Paper[28] 3-Tap FIR Filter (Virtex-4 (XC4VFX12))		24.648
Paper[28] 3-Tap FIR Filter (XC5VLX110T)		18.696
Paper[29] (SPARTAN 3E FPGA)		15.458

Table 4. Synthesis results are compared among IIR filters in terms of area

Implemented IIR Filter	Area(LUT)
1st order IIR Filter	10
2nd order IIR Filter	44
3rd order IIR Filter	149
4th order IIR Filter	159
10th order IIR Filter	272
Paper[18]	420
Paper[3] IIR filter of order 2	72
Paper[21] IIR filter of order 14	4832
Paper[1] IIR filter of order 4	967

Table 1 represents synthesis results for the implemented FIR filter of order 1st, 3rd and 10th in Artix7 Basys3 FPGA. From this table, it is clear that the 10th order FIR Filter based on CIA adder and 8X8 vedic multiplier performs better than other FIR filters. Table 2 represents synthesis results for the implemented IIR filters of order 1st, 2nd, 3rd, 4th and 10th in Artix7 Basys3 FPGA. Table 3 represents the comparison of the synthesis results among various FIR filters in terms of area and speed. From this table, it is clear that the 10th order FIR Filter based on CIA adder and 8X8 vedic multiplier performs better than other implemented FIR filters. Table 4 represents the synthesis results in comparison among IIR filters in terms of area. From this table, it is clear that the proposed IIR filter consumes less area than existing IIR filters. This study shows that if the order of FIR increases, better-filtered ECG signals are obtained. Also, if the order of IIR filters increases, ECG signals won't be filtered correctly.

4. Conclusion

In this research, FIR and IIR filters of various orders are designed and implemented. To improve the FIR filter performance, a 16-bit carry increment adder and 8X8 vedic multiplier are used for the addition and multiplication process. Input noisy ECG signals and filtered ECG signals are stored in text format. Matlab tool is used for finding the filter coefficients and plotting noisy and filtered ECG signals. All simulation waveforms for the implemented FIR and IIR filters are shown. The 10th order FIR Filter, which is based on CIA adder and 8X8 Vedic multiplier, consumes 32 LUTs, has a data path delay of 5.396, and consumes a total on-chip power consumption of 6.618 watts. Among implemented IIR filters, 2nd order IIR filter consumes the lowest power. When the order of filters is increased, FIR filters have a better filtering operation than IIR filters.

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