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Original Article

Performance Comparison of Different Buck-Boost Converters for Power Factor Correction in an SMPS for PC Applications

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Abstract *- In the conventional power supplies used for PC applications, the supply current's Total Harmonic Distortion (THD) ranges up to 80%, and the power factor goes as low as 0.55. When a large number of such power is used for powering up many electronic appliances, the power quality of the distribution system deteriorates drastically, simultaneously increasing the neutral current considerably. This affects the performance parameters and efficiency of the distribution system adversely. This paper aims to provide an improved model of SMPS (Switched Mode Power Supply) with a power factor correction stage, which could look into the reduction of harmonic content and improve the quality of supply. Three types of buck-boost converters are explored here, namely, a conventional buck-boost, Cuk and SEPIC, which are employed for PFC. All three converters have been analyzed, and their design equations are derived and used to design each component in these converters in Discontinuous Conduction Mode (DCM). Then each one of them has been modeled in MATLAB-Simulink environment. The performance of the modeled power supply with three different types of PFC converters is compared in terms of settling time, overshoot, power factor, and current harmonic content at the utility interface point stress across the devices, number of components and capability to regulate the voltage output during supply voltage and load variations. From this objective comparison, it would be easy for any user to make a judicious choice for the SMPS application as per the user requirements.*

Keywords *- Converters, Power quality, Simulation, SMPS, THD.*

1. Introduction

Conventional computer SMPS have highly distorted input currents with a high range of harmonics, and hence, these do not abide by international standards. In the present day SMPS, it is usual to have the input circuit consisting of a full wave rectifier along with a filter for maintaining the voltage by application of storage of charges by a capacitor. In such a case, the current that the input is drawing occurs at the peaks of the input waveform and the pulse of current contains enough energy to maintain the load till the next input current peak arrives [1]. This is done by dumping a large amount of charge in the capacitor in a shorter amount of time, after which the capacitor starts slowly discharging the charge to the load until the next peak comes, and the cycle begins to repeat itself. As a capacitor is used at the front end of SMPS at the rectifier output, it leads to uncontrolled charging of the DC capacitor and thereby results in a pulsed current waveform with the peak of the waveform going beyond the amplitude of fundamental AC mains current and causing very high THD. In order to overcome these shortcomings, research is being done in this area extensively. The aim is to draw a unity power factor sinusoidal current and make a system which follows international standards. In the past, for the improvement of power factor in SMPS, various researchers have done work. [2] introduced a canonical switching cell converter for PFC.

A control strategy was introduced for boost converters for PFC in SMPS. The evaluation and investigation of various converter topologies in terms of PFC was done in [4] for single stage power supplies. This work aims at reducing the harmonic content at the front end of the PSU used for personal computers, which normally can go as high as upto 80%, and the power factor in the conventional systems can be much less than unity.

The basic objective is designing SMPS for a PC while incorporating a power factor correction converter in the existing design to optimize the performance of SMPS by improving the quality of the power at the utility interface point [5]. For this purpose, various PFC converters are analyzed and their performances are compared so that a proper choice can be made as per the requirement for SMPS application.

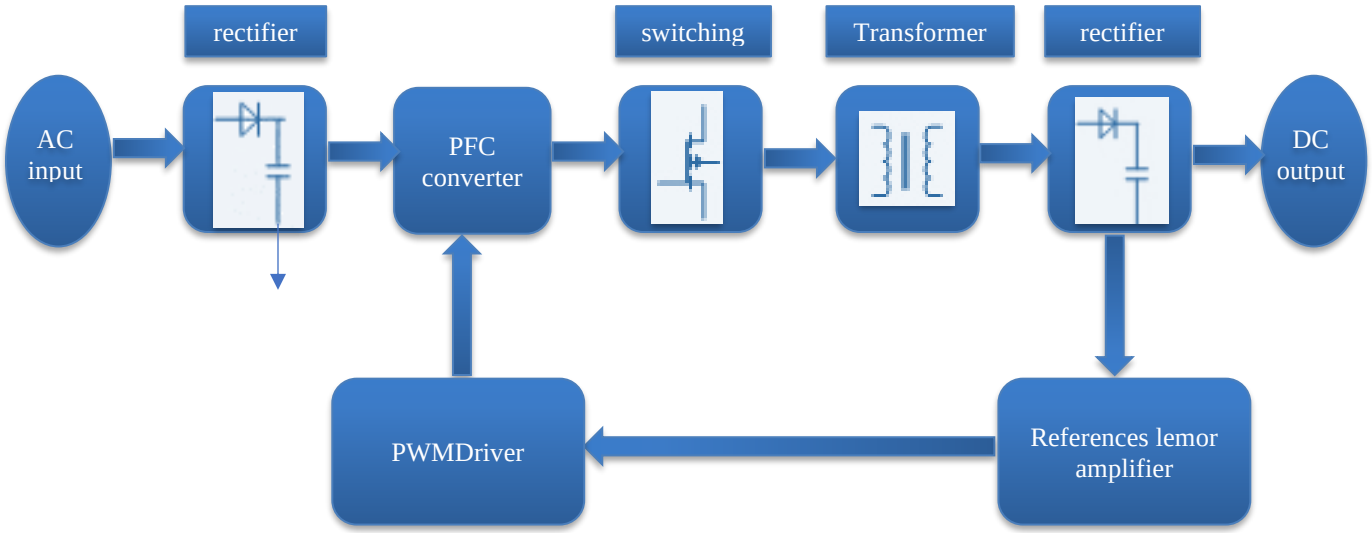

Fig. 1 Block diagram of the proposed model

2. System Configuration

The model is proposed for a power rating of 350W, with voltage ratings of ±12V, ±5V and +3.3V. The complete system is comprised of three stages. The first stage includes the conversion of the AC mains supply (230V rms) to a DC supply using the conventional full-bridge diode rectifier. The output DC voltage of the full-bridge rectifier is input to DC-DC PFC converter which will step it down to 50V. In the third stage, a half-bridge inverter is used because the power requirement of a PC is approximately up to 350W, and a half-bridge converter is best suited for this requirement, which includes a high-frequency transformer with multiple taps in the secondary to provide for the required voltage levels as per the PC requirements. Figure 1 shows the block diagram of the proposed system. In order to get a regulated supply irrespective of the input voltage or load variations, feedback control is employed.

3. Design of Proposed SMPS

Multiple DC voltages are required at the output stage of SMPS for PC. This is achieved by using a multi-tap transformer in conjunction with a diode rectifier and a filter circuit. In order to regulate the output voltage and improve the power factor of the system, different control strategies are employed. Controlling can be achieved by the weighted error approach, or the relative sensitivity approach can also achieve it. In the weighted error approach, the weights of all the output voltages and output currents are sensed, and the distribution of energy stored in the transformer to all the different outputs is then based on the relative weights that were recorded for power quality improvement. In the relative sensitivity approach, the loads having the highest power ratings, their respective voltage and currents are sensed, and then the controlling is done based on the errors recorded by the highest power rating outputs while neglecting the lower ratings, thereby reducing the circuitry and making the system circuitry less complex. In order to improve the power factor, a PFC converter is used at the front end and for the next stage, a half-bridge converter is a preferred choice as it has the benefits of high frequency isolation for multiple DC outputs and improved core utilization. Table 1 provides the design specifications.

3.1. Cuk Converter

The transfer of energy in a Cuk converter depends on the capacitor C1(Figure 2). A non-isolated Cuk converter comprises two inductors, two capacitors, a diode and a switch [7]. Figure 2 shows the complete SMPS system with PFC as a Cuk converter.

Cuk converter operates in two states [6]-

- During the off state, the capacitor C1 gets charged through the inductor L1 from the input source.
- During the on state, the capacitor discharges and then transfers the energy through the inductance L2 to the output capacitor.

The Cuk converter operates in both Continuous(CCM) and Dis-Continuous Current Mode(DCM), as well as in discontinuous voltage mode, where the voltage across the capacitor drops to zero during the commutation cycle[7].

Table 1. Design specifications of single phase SMPS system

AC input voltage	230V(rms)
Output voltage for PFC DC-DC converter	50V(DC)
Available output voltages at the load-end	12V/18A
	5V/30A
	-5V/1A
	3.3V/1.5A
	-12V/0.8A
Switching frequency	50kHz

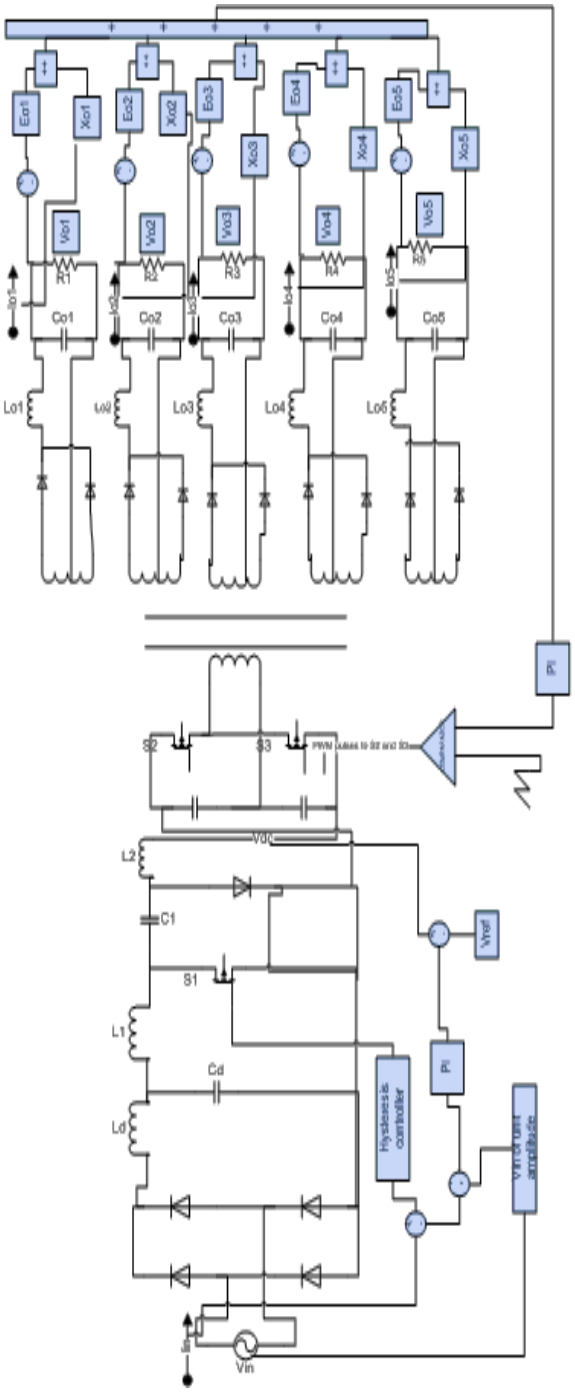

Fig. 2 Cuk PFC based SMPS complete model block diagram

3.2. SEPIC

Single Ended Primary Inductor Converter (SEPIC) is a DC-DC converter, similar to a traditional buck-boost converter, but the output for SEPIC is non-inverted [6]. The exchange of energy takes place between the inductors and the capacitors so that voltage can be converted from one level to another[3]. SEPIC also has CCM and DCM conduction modes. The exchange of energy between the inductors and capacitors depends on the controlling of the switch.

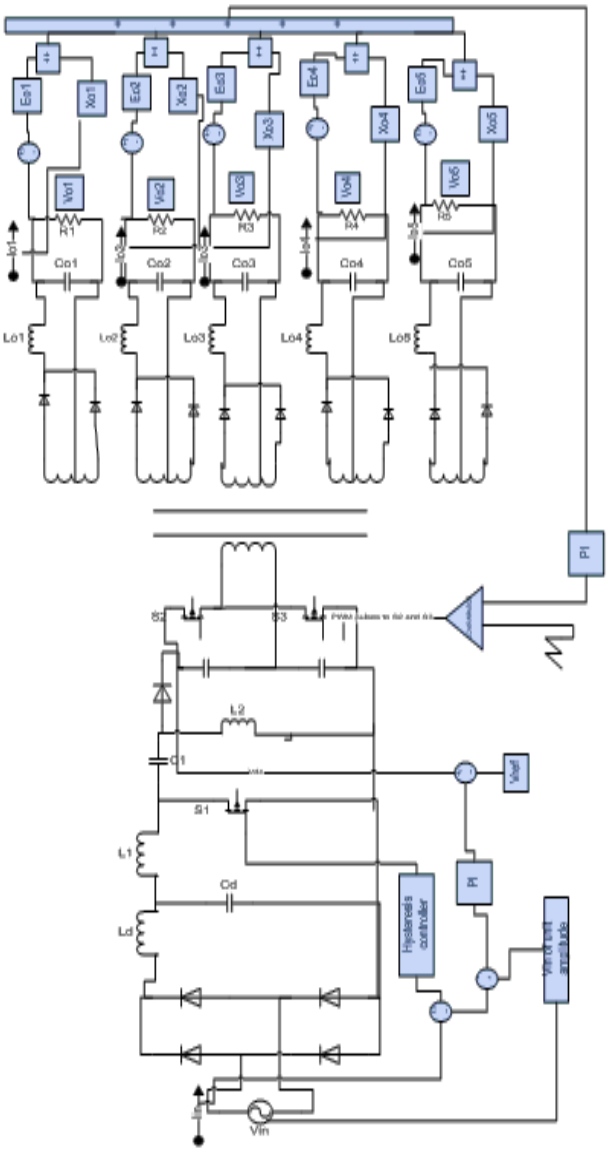

Fig. 3 SEPIC PFC based SMPS complete model block diagram

3.3. Buck-Boost Converter

The principle of operation of the buck-boost converter is as explained below-

- During the on state, the input voltage source is directly connected to the inductor, thereby transferring the energy to inductor L shown in Figure 4. During this stage, the load gets the supply of energy through the capacitor.
- During the off state, the inductor connects to the external load and capacitor, and hence, the energy transfer takes place from the inductor to the capacitor and load.

It is observed that the voltage gain for the CCM mode is more complicated as compared to the DCM mode. Also, in DCM mode, the output voltage not only depends on the duty cycle but also depends on the inductor value, the input voltage and the output current.

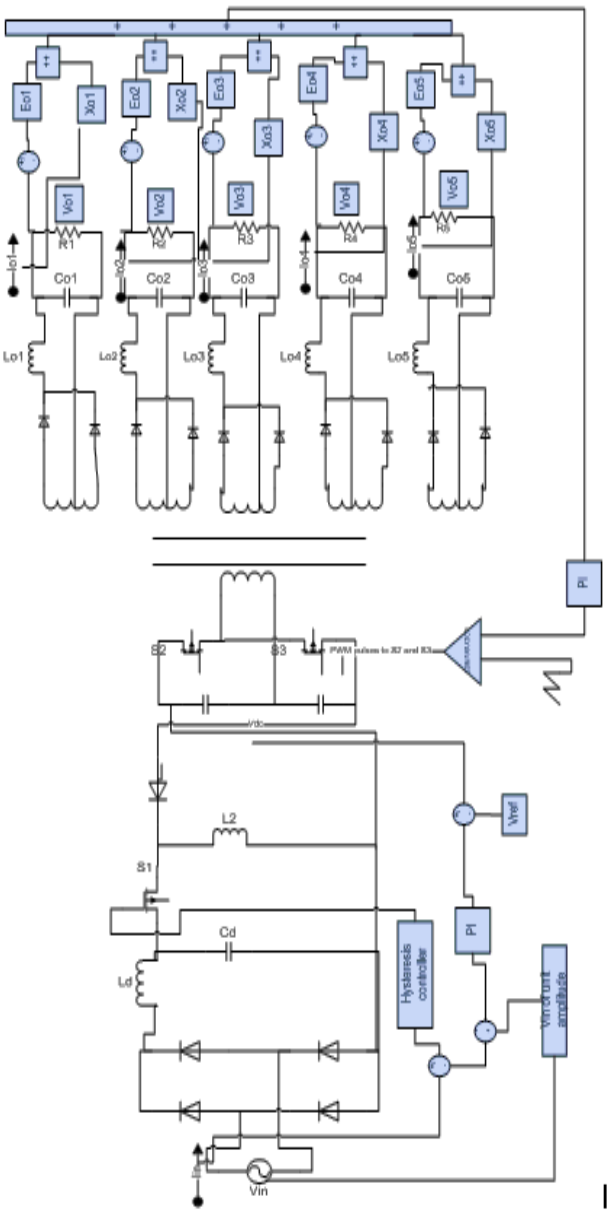

Fig. 4 Buck-Boost PFC based SMPS complete model block diagram

3.4. Control

Personal computers require well-regulated DC voltages at the output in order to drive different devices. Hence, in order to regulate the output, a feedback circuitry is necessary, which may control the pulses to be given to the converter circuits. Two feedback loops are employed in the proposed model, where one feedback loop senses the error at the output of the PFC converter, and the second feedback loop controls the half-bridge inverter circuit with respect to the load-end side voltage variations. For the first feedback circuit, that is, the PFC feedback circuit, the desired output is 50V, which will then be given to the inverter stage. Hence the actual voltage at the output of the Power Factor Correction(PFC) stage is compared with the reference voltage (50V) and then is fed to a Proportional-Integral(PI) controller. The output of this PI controller is then multiplied with a unit amplitude input supply side voltage. This acts as a reference current, which then has to be compared with the supply input side actual current and given to a hysteresis loop controller, which determines the pulses to be given to the switching element of the PFC converter circuit. Another feedback circuit comes into play at the load end side. Multiple output voltages are required for PCs having different current ratings. The voltage delivered at the output is affected by the changes in the demand for power in the other outputs. Hence, a weighted error approach is used where the weights of all the output voltages and output currents are considered, and duty cycle variation for the half-bridge inverter is done accordingly. Each output voltage is individually multiplied with an appropriate weighting factor which is then summed together.

This summation value is then given to a PI controller, and then by comparing the output of the PI controller with a saw-tooth waveform, pulses are generated, which are given to the half-bridge inverter switching elements. Weights are decided by taking the voltage error (difference in actual voltage with respect to the reference voltage) and multiplying it by a factor E, where E is the ratio of the rating of the respective voltage and the total rating of the SMPS system and, also sensing the output current and multiplying it by a value X, where X is the ratio of present load on the respective output and that output's rating. Hence V multiplied by E and I multiplied by X is then summed up for all the individual outputs and then collectively added and then processed to a PI controller. Table 3 gives the weighting factor calculated for the output levels based on the above explanation.

Table 2. Design equations

Converter	Equations		
Buck-Boost	Vo	=	-Vs(D/1-D)
	C	=	V_o*D*T_s/2*ΔV*R
	L	=	V_g*D*T_s/2*i_L
Cuk	Vo	=	-Vs(D/1-D)
	ΔI_{L1}	=	V_S*D/L_1*f
	ΔI_{L2}	=	V_S*D/L_2*f
	ΔV_o	=	V_o*(1-D)/8$L_2C_2f^2$
	L_{1min}	=	$(1-D)^2$*R/2D*f
	L_{2min}	=	(1-D)*R/2*f
SEPIC	Vo	=	-Vs(D/1-D)
	ΔI_{L1}	=	V_S*D/L_1*f
	ΔI_{L2}	=	V_S*D/L_2*f
	ΔV_o	=	V_o*D/R*C_2*f
	ΔV_{c1}	=	V_o*D/R*C_1*f

Table 3. Weighting factors for individual output voltages

Weighting factor	Output voltage	Value
W1	+12	.5610
W2	+5	.38900
W3	-5	.012966
W4	+3.3	.012966
W5	-12	.02489

Table 4. Component values selected in converters

Converter	Cuk	Buck-boost	SEPIC
Ld (mH)	0.087	0.087	0.087
Cd(µF)	18	18	18
L1(mH)	6	11.7	20
L2(mH)	2	-	15
CI(µF)	6.33	278	4
C2(µF)	222.127	-	500

Using the design equations as mentioned in Table 2, the component values selected for the Cuk, buck-boost and SEPIC converter are mentioned in Table 4.

4. Simulation and Results

MATLAB based modeling in the Simulink environment of various SMPS systems is carried out, and the results are shown on the basis of their behavior during the transient and steady state conditions. Results are also noted whenever there are load perturbations and the change in output levels after that. For all three systems, 230V(rms) and 50Hz are given to the supply and fed to a full-wave bridge rectifier. Waveforms are recorded and results are derived henceforth.

4.1. Buck-Boost Converter

As it can be observed from the above Figures 5(a) and 5(b) above, the settling time of a buck-boost converter-based SMPS system is 0.2 seconds, and hence, it takes about 10 cycles (at the power frequency) to settle down. The power factor for this system is noted to be 0.9995598, and the total harmonic distortion is 9.75%. With the change in the output load, by increasing the load from 50% to 100%, the output response is noted to check the regulating capability of this converter. As it can be seen, with slight variation in voltage, it finally settles down to +12V.

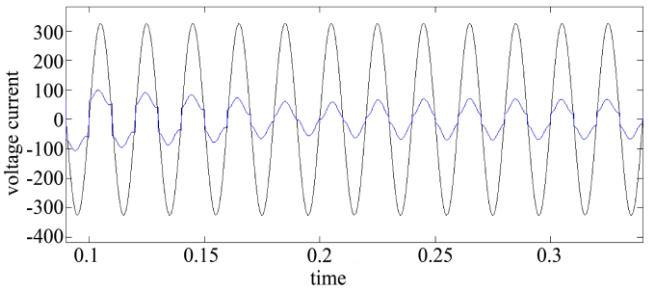

Fig. 5(a) Supply side voltage and current waveform

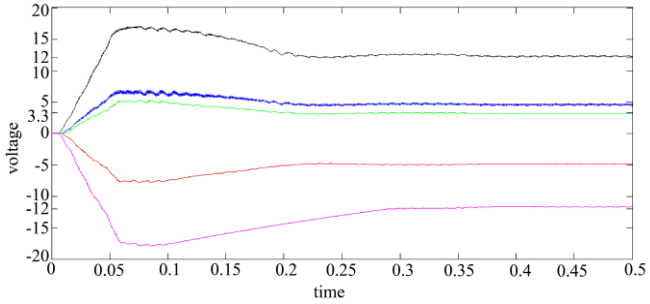

Fig. 5(b) Load voltage waveform

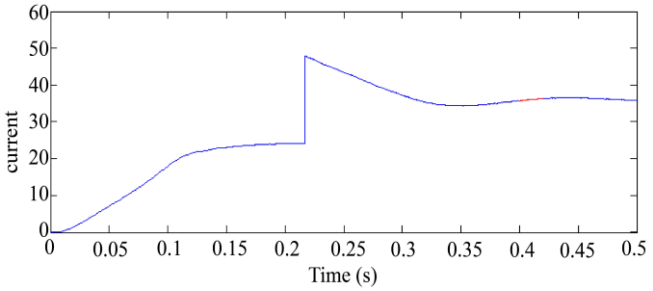

Fig. 5(c) Load current variation (for +12V output)

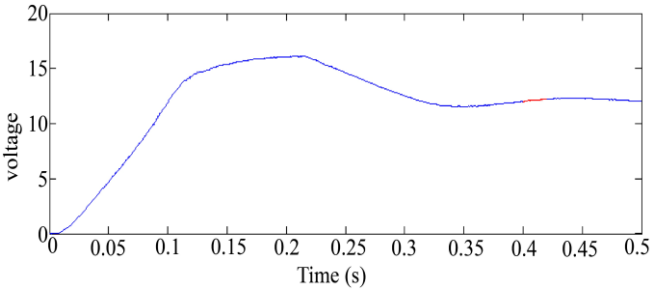

Fig. 5(d) Output voltage waveform with change in load (for +12V output)

4.2. SEPIC

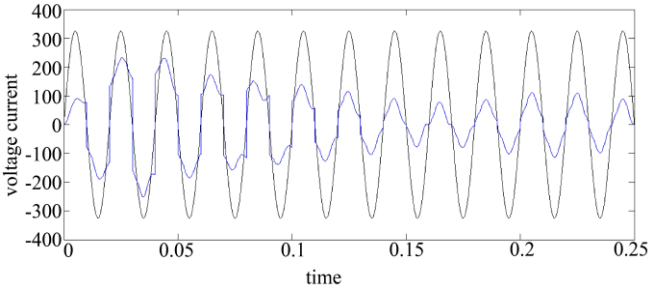

Fig. 6(a) Supply side voltage and current waveform

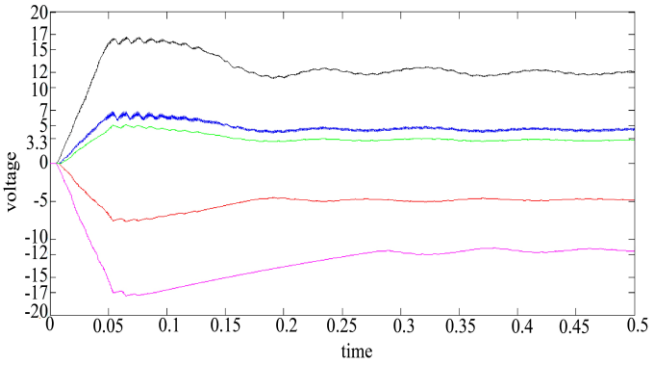

Fig 6(b) Load voltage waveform

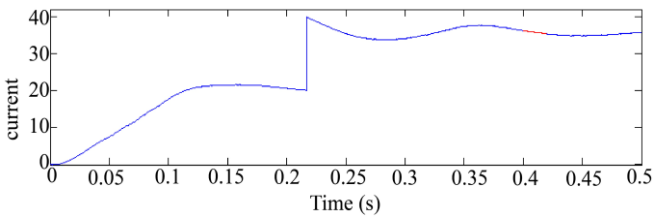

Fig. 6(c)load current variation (for +12V output)

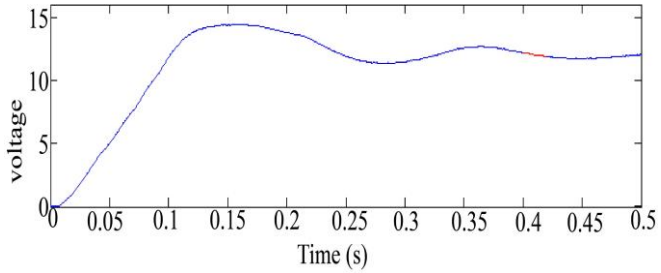

Fig. 6(d) output voltage waveform with change in load (for +12V output)

The settling time for SEPIC comes out to be 0.35 seconds, and for the PFC output stage, its peak rises to about +80V. The input power factor is 0.9990, and the total harmonic distortion for input current is 8.8%. With the change in load, the current requirement is doubled, but with slight variation initially, the voltage settles down at +12V; hence, the output voltage regulation is taken care of in SEPIC.

4.3. Cuk Converter

By analyzing the waveform shown in Figure 7(a), it is found that Cuk suffers from a high THD of 10%, but the power factor is 0.9989. With the change in the output load, by increasing the load from 50% to 100%, the output response is noted to check the regulating capability of this converter. As it can be seen, with slight variation in voltage, it finally settles down to +12V.

The results are shown in the table that power factor correction is achieved fairly well in all three converters quite effectively. However, the buck-boost converter seems to have the maximum input current THD although it will be the most cost-effective because of having the least number of components. However, the switch stress seems to be the maximum in the Cuk converter.

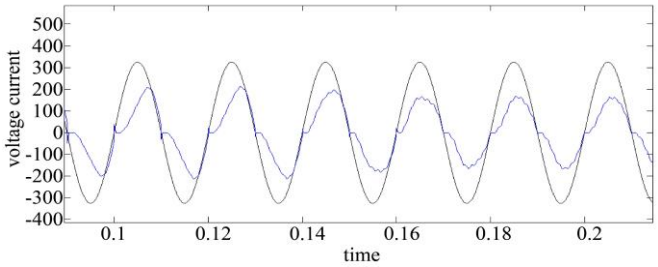

Fig. 7(a) Supply side voltage and current waveform

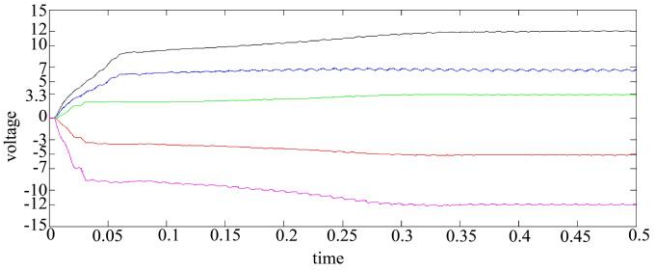

Fig. 7(b) Load voltage waveform

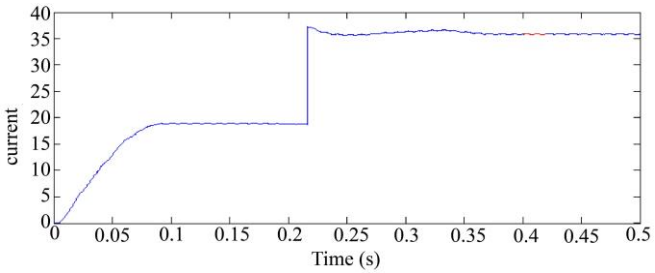

Fig. 7(c)Load current variation (for +12V output)

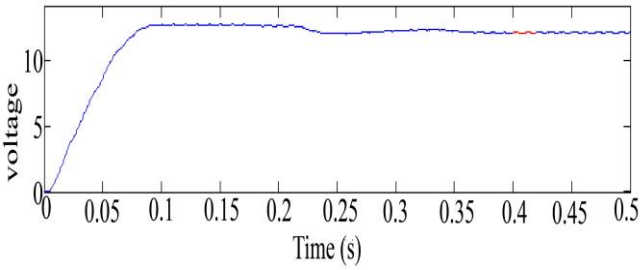

Fig. 7(d) Output voltage waveform with change in load(for +12V output)

4.4. Comparison of Various Converters

From the results obtained, it can be seen that for the performance of the three power converters varies. While the power factor has improved by all the three converters and has reached to 0.99, but the total harmonic distortion is least for SEPIC converter with the value of 8.81. The output voltage for Cuk converter and buck-boost converter is inverted, while for SEPIC we get the voltage waveform as positive due their topological differences. As buck-boost converter has only three components, the chances of component failure and the costing for the converter will be less in buck-boost converter as compared to Cuk converter and SEPIC. The comparative analysis has been depicted in the form of table in Table 4.

Table 5. Performance comparison table

Converter Type	Settling Time(s)	Peak Overshoot (at PFC Output in%)	Power Factor	THD (%)	Output Voltage Ripple (%)					No of Components
					Vo1	Vo2	Vo3	Vo4	Vo5	
Buck-boost	0.2	66	0.9995	9.75	2.1	1.9	1.5	1.5	1.6	3 elements (D=1, L=1, C=1)
Cuk	0.18	74	0.9989	10	2.2	1.7	1.4	1.5	1.4	5 elements (D=1, L=2, C=2)
SEPIC	0.25	60	0.9990	8.81	2.9	2.5	1.7	1.99	1.5	5 elements (D=1, L=2, C=2)

5. Conclusion

The three types of PFC based SMPS system has been modeled in a Simulink environment, and results have been derived from the waveforms thus obtained. It can be seen from the comparison table for the three converters that in terms of the settling time for the output to reach its steady state, Cuk takes minimum time as compared to SEPIC and buck-boost converter, but the percentage peak overshoot is also the largest for Cuk converter. The power factor for all three converters is close to unity, and hence the aim of improving the power factor and bringing it near to unity has been achieved. In terms of voltage regulation, SEPIC is a mediocre one. Buck-boost is the most cost-effective option as it requires the least number of elements as compared to the Cuk and SEPIC converter. Device stress is minimum for the SEPIC converter. Hence on the basis of the requirement of the application, a judicious choice can be made amongst the three converters from the results obtained in this paper.

References

[1] Luka Petrović, Šandor Iles, and Jadranko Matuško "Self-Learning Model Predictive Control Based on the Sequence of Controllable Sets," *19th International Conference on Electrical Drives and Power Electronics*, Dubrovnik, Croatia, pp. 359-364, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[2] Shikha Singh et al., "Power Factor Correction in Switched Mode Power Supply for Computers Using Canonical Switching Cell Converter," *IET Power Electronics*, vol. 8, no. 2, pp. 234-244, 2015. [CrossRef] [Google Scholar] [Publisher Link]

[3] William P. Robbins, Ned Mohan, and Tore M. Undeland, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley, pp. 1-802, 2003. [Google Scholar] [Publisher Link]

[4] Hugo Ribeiro, and Beatriz Borges, "Techniques to Obtain Single-Stage Power Supplies with Power Factor Correction (PFC)," *International Journal of Electronics*, vol. 98, no. 4, pp. 487-504, 2011. [CrossRef] [Google Scholar] [Publisher Link]

[5] Joel Turchi et al., "Power Factor Correction Handbook," *ON Semiconductor*, pp. 1-130, 2014. [CrossRef] [Publisher Link]

[6] D. Prasad et al., "Cuk and SEPIC Converter," *Power Electronics, IIT Kharagpur*. [Publisher Link]

[7] L. Ashok Kumar, S. Albert Alexander, and Madhuvanthani Rajendran, "Emerging DC–DC Converter Topologies," *Power Electronic Converters for Solar Photovoltaic Systems*, pp. 289-329, 2021. [CrossRef] [Publisher Link]