

Comparison of hamming, BCH, and reed Solomon codes for error correction and detecting techniques

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Abstract

In digital communication, errors are introduced during the transmission of data from the transmitter to receiver due to noise or environmental interference. Hence, we have to use some kind of error control coding for error detection and error correction. In this paper we are applying error control mechanisms, like hamming code, BCH codes and reed Solomon codes to detect and correct the errors. Thus we are used Hamming code, Reed-Solomon and BCH code control techniques to correct the errors. Lastly we are comparing the capability of error correcting those codes. The comparison is based on the strength of error correcting technique.

Keywords: hamming code, Reed-Solomon code, BCH code, error detecting, error correcting.

I. INTRODUCTION

In digital communication, errors are introduced during the transmission of data from the transmitter to receiver due to noise or environmental interference [1]. These errors can become a serious problem for achieving accuracy and performance of the system [1]. Therefore, the reliability of data transmission is required to be improved. To improve the reliability, it is essential to detect and correct the error. Hence, we have to use some kind of error control coding for error detection and error correction. In this coding, one or more than one extra bit is added to the data bits at the time of transmitting the data. These extra bits are called parity bit that helps to detect the errors. The data bits along with the parity bit form a code word [1]. There has different type of error control coding such as parity checking, check sum error detection, cyclic redundancy check, & Hamming code. Compare with other error controlling code, hamming code has high efficiency for error detection and as well as error correction and this code is also easy to implement. Because of The simplicity of hamming code, they are widely used in computing memory, data compression & other application of telecommunication [2]. In this project, we have

designed a circuit to implement the hamming code. Here they analyse the hamming code algorithm for 8 bit data word.

Hamming code can detect up to two simultaneous bit errors. In communication system, the information signal is send through transmitter and is transmitted through some random media. In the process of transmission the information gets corrupted, so we get a signal at the receiver which is different than the original information signal. The general idea for achieving error detection and correction is to add some redundancy (i.e., some extra data) to a message, which receivers can use to check consistency of the delivered message, and to recover data determined to be corrupted. The information signal is added with redundant bits “r” to form the code this code is then transmitted. The receiver receives the code and corrects it to get the original k bits information signal. The Information revolution is in full swing, having matured over the last thirty years. It is estimated that there are hundreds of millions to several billion web pages on computers connected to the Internet, depending on whom you ask and the time of day. To have a reliable communication through noisy medium that has an unacceptable bit error rate (BER) and low signal to noise ratio (SNR), we need to have Error Correcting Codes which is based on proven mathematical formulas. There are many types of error correction codes based on the type of error expected, the communication medium and weather re-transmission, etc. Some of the Error correction codes, which are widely used these days, are BCH, Turbo, Reed Solomon, and LDPC.

II. SYSTEM MODEL AND DESIGN

Modelling parameters of hamming code
Family of (n, k) block error-correcting codes with parameters:

Block length: $n = 2^m - 1$

Number of data bits: $k = 2^m - m - 1$

Number of check bits: $n - k = m$

Minimum distance: $d_{min} = 3$

Single-error-correcting (SEC) code

SEC double-error-detecting (SEC-DED) code

Modelling parameters of reed-Solomon code

RS codes are generally represented as an RS (n, k), with m-bit symbols, where

Block Length: n

No. of Original Message symbols: k

Number of Parity Digits: $n - k = 2t$

Minimum Distance: $d = 2t + 1$

Modelling Parameters of bch codes

For any positive integer's m ($m \geq 3$) and t ($t < 2^{m-1}$), there exists a binary bch code with the following parameters:

Block length: $n = 2^m - 1$

Number of parity check bits: $d - k < mt$

Minimum distance: $d_{min} \geq 2t + 1$

The code with the above parameters is capable of correcting any combination of t or fewer errors in a block of n digits with k message bits. The generator polynomial of this code is specified in terms of its roots from the Galois field $gf(2^m)$. The generator polynomial $g(x)$ of the binary t-error-correcting bch code of length $2m - 1$ is given by

$$G(x) = \text{LCM} \{ \phi_1(x), \phi_2(x), \phi_3(x) \dots \phi_{2t}(x) \}.$$

However, generally every even power of α has the same minimal polynomial as some preceding odd power of α in $gf(2^m)$, where α is the primitive polynomial. As a consequence, the generator polynomial for the t-error-correcting binary bch code can be reduced to

$$G(x) = \text{LCM} \{ \phi_1(x), \phi_3(x), \phi_5(x) \dots \phi_{2t-1}(x) \}.$$

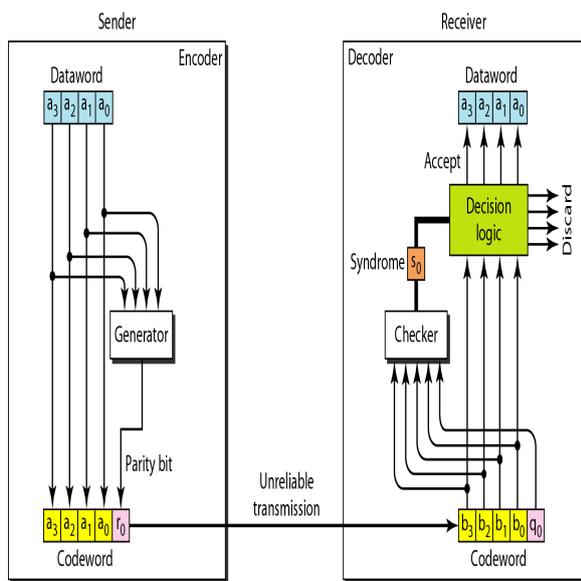


Fig.1: Encoder and decoder for parity-check code

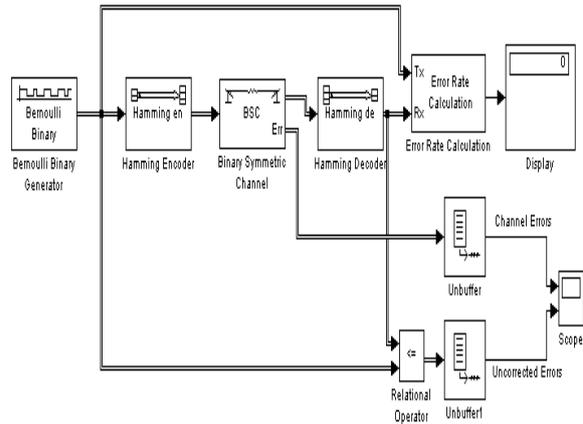


Fig.2: simulation design of hamming code

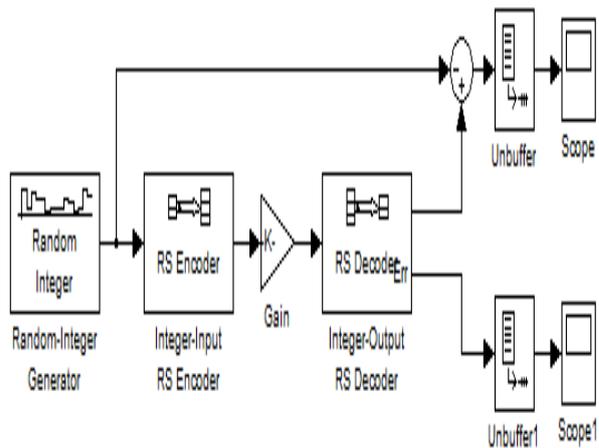


Fig.3: simulation design of reed-Solomon code

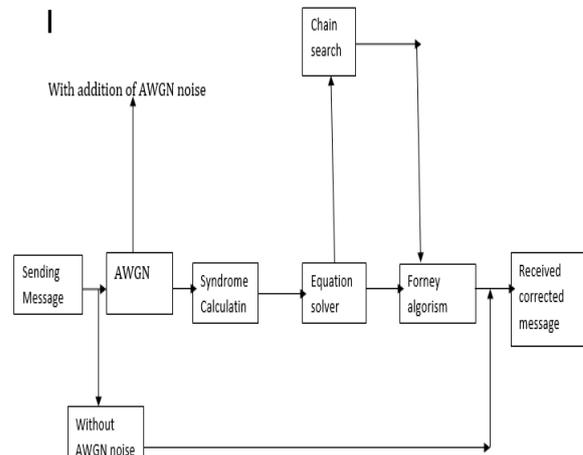


fig.4: design of bch decoder

III. RESULT AND DISCUSSION

IV.

In this section, we are comparing the three error correction and detection codes.

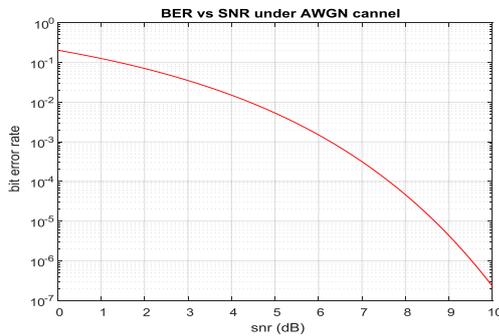


Fig.5: BER of Reed-Solomon code

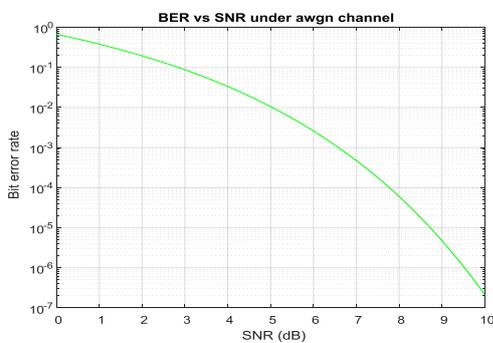


Fig.6: BER of bch code

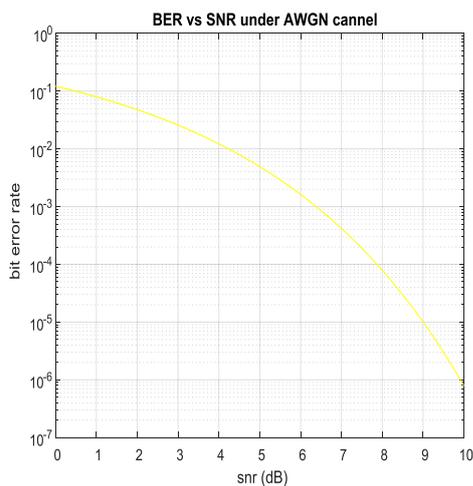


Fig.7: BER of hamming code

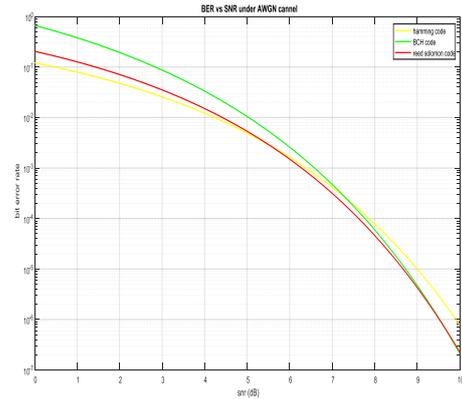


Fig.8: comparisons of bch, hamming and reed-Solomon codes

IV. CONCLUSIONS

In this paper the comparison of hamming code, BCH code and reed solomon codes has been discussed. From the result it is computed capacity of error correcting and detecting among the three error correcting and detecting codes. Thus hamming code is suitable for short communication systems. but as we can absorb from the above plots, BCH code is very good for long communication systems. because as the SNR ratio increases, the error correcting capacity of BCH code is also increase. but for high SNR, errors are difficult to correct by hamming code. but for small SNR hamming code is accurate technique rather than the others. and thirdly reed solomon code is better for correcting and detection errors at medium communication systems. reed solomon code is better than hamming but lower than BCH codes.

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