Implementation of Ultra Low Power Vlsi Design and Its Participation with Br4-Reversible Logics

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Abstract *— In this research work an advanced ultra-low power consumption circuit design approaches are defined. This method is more suitable for providing the support to modern technologies such as mobiles, PCs, tablets, laptops, super computers etc. In VLSI era size, memory, power back up, speed of operations are major necessary constraints. This foremost restrains related to present low power applications; these are mainly depending on VLSI chips. So, all discussed parameters are necessary to full fill for advanced designs. Moreover, economy is another more subject while design an ultra-low power SoC chips, therefore leakage power controlling, power maintenance schemes are overcome the limitations. Moreover, the major issue related to VLSI technology is cost and speed of operations. For ultra-low power technology leakage currents assumed to be reduced, otherwise circuits consume more power. In this research work novel leakage reduction-based chip designs are proposed through reversible logic gates. These proposed systems achieve 20% power saving, 98.7% accuracy and 20% speed of operations improved compared to existed methods.*

Keywords: *Low power, Power Organization, reversible logic gates, speed of operations.*

I. INTRODUCTION

Low power VLSI design offering many applications they are more significant. In VLSI technology important problems are solved in recent advancements. The conventional circuits and logic gates are utilised to implementing the digital circuits but, they consume more power and less in speed of operation. The generalized gates such as OR, NOR, XNOR and NAND these are having several inputs and output terminals. Therefore, they cannot be reversible during the functionality time, due to this leakage power has been dissipated. In order to perform the reversible operations and reduces the power consumption reversible logic gates are proposed. In reversible logic gates 1 to 1-bit mapping has been maintained between input and output, therefore reversible operations are possible and power consumption automatically reduces. The unwanted inputs and outputs are neglected in the circuit is not utilized. Sum of basic logic gates and reversible logic gates available but these maintenance is more. The emerging Technologies like ultra-low power VLSI designs most commonly requires low power operations. To minimize the complexity of operations and improve the speed of functionality an advanced reversible logic design is required.

The reversible computing like information enhancing and conventional logic operations or major key points in the proposed research work. The more dissipations have been occurred through absolute bit by bit transmission. The major constraint in reversible logic function is to reduce the operational logic gates in the VLSI chip design. The complexity of circuits can be minimized when Fan In and Fan Out parameter adjustment.

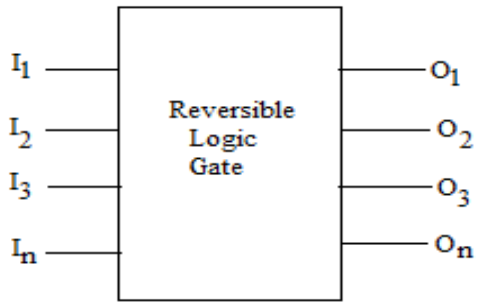

Figure.1 Power Dissipation in reversible logic

The above figure 1 clearly explains about reversible logics in the proposed work these are not supporting the repeated functions and consumes less power with irreversible property. To solve the reversible logic introduced a full adder design with reversible CMOS gates.

The performance analysis of reversible logic designs is providing more speed of operations economy and low power consumption. In this investigation BR4 reversible full adder design is estimated, it is a efficient high speed consideration to solve the present limitations of VLSI chips. In this work Xilinx 14.b software tool is used to investigate the various logics. This design is more useful for digital signal processing, computer applications and wireless applications.

II. LITERATURE SURVEY

A low power efficient carry saves adder design and modified carry save adder model with CMOS technology has been improved its performance and power consumption. The ship area and speed of operations are improved through this design with 90nm CMOS technology. In this technology generalized CMOS logic gates are designed for high speed multiplication and addition. Due to carry save the current operations are reduced and gives the more accuracy [1]. The conservative and reversible logic designs are broadly compatible with optimized VLSI technology. A generalized conservative logic gates are efficiently providing the logic functions with low level hardware, due to these complex functions performed easily. The carry skip adder and ripple carry adder are gives the results with more improvement compared to several skip adder Technologies. The practical and theoretical performances are done with carry skip adder technology [2]. In multimedia communication and many 5G communication faults tolerance technology providing the accurate results. When reversible logic techniques allow the fault effects then automatically primary outputs are easily generated from proposed logic. A fundamental logic designs cannot solve the present limitations of full adder and multiplayers. These complex limitations are overcome through reversible logic gates easily compared to past technology carry skip adder and ripple adder determine the shorter delay with flexible size. These are not sufficient and requires additional low power benefits [3].

Ref No	Technique	Key points
[4]	reversible fault tolerant	A fault tolerance adder and subtractions of reversible gates are utilized to improve the present VLSI technologies. Using these techniques performs the speed of operations with more accurate outcomes.
[5]	Stability Enhancing	Stability and scalability are a very critical term which is possible with advance logic gates design.
[6]	reversible logic gates	Delay is an important factor, it controlled only through proper usage of logic gates. In this work ALU design is implemented with reversible logic gates design.
[7]	a review on reversible logic gates	In this investigation a detailed review is conducted for reversible logic gates. This study clearly gives the major advancements of SoC design and chip design steps for high speed of operations.
[8]	Adder designs using reversible logic gates	Advanced adder designs are most useful for advance technologies this can be possible only through reversible logic gates. In this study the VLSI design is majorly concentrate on different types of modules and blocks in the design of ALU.
[9]	Cryptography with LFSR	LFSR is a technique which can offers the high-level operations for VLSI design. In this research work a low power adder and ALU designs are verified through Cryptography LFSR.
[10]	Efficient design of reversible ALU	A quantum-dot cellular VLSI design is most useful for Low power applications. In this study ALU design is verified through advanced reversible logic gates technique.

At present many irreversible logic gates can solves many low powers and less area applications. the topics like digital image processing digital signal processing, cloud computing, data mining, artificial intelligence, machine learning is run on NCB's with low level performance and high-power consumptions. Due to above limitations gigabytes of functions happens with lesser speed. The effectiveness of irreversible logic gates continually monitors the available modules with low power techniques. Due to this 34 %-time delay and 24 % overhead delay improved [11].

III. METHODOLOGY

In this research work BR4 reversible logic gates are designed for low power and less delay of operations. BR4 reversible logic gates are major logic gates available in current technology. in this the input and output reconstruct the functionality without any disturbance therefore available logic gates are do not solve the present limitations. So, BR4 reversible logic gates are proposed. In this circuits are 1 to 1 vector techniques; the reconstructed input is easily arrived from buffers then converted into output vectors. In these impulse functions plays an important key role. Moreover, there is no universal input and output reversible logic gates do not available. Hence propose reversible logic gates are minimized the power and improve the performance. The delay in operation decided by minimum number of gates with available path. The economy and design complexity are very low with proposed reversible logic gates[12-13].

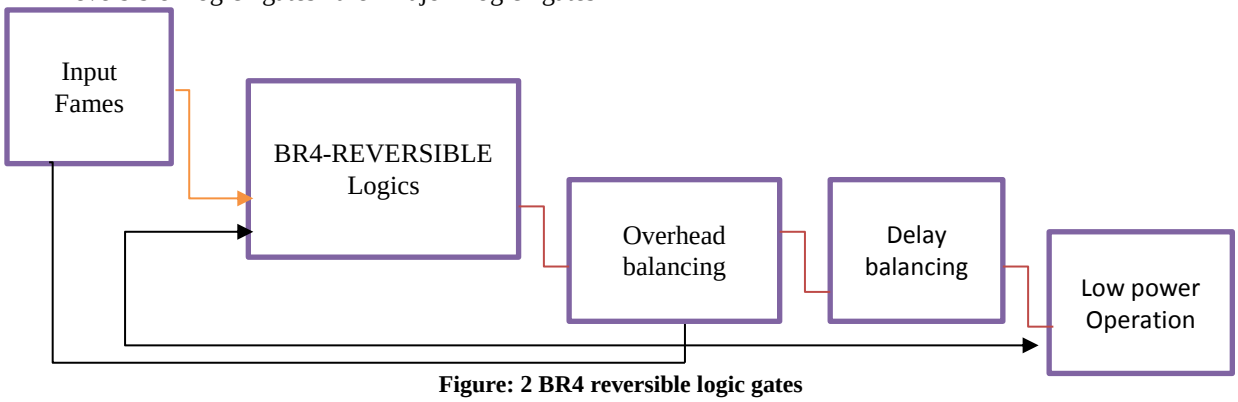

Figure: 2 BR4 reversible logic gates

Figure 1 clearly explains about logic operations of BR4 reversible logic gates, in this first step input frames are collected from buffers. In the second stage reversible operation is performed through br4 technique [14-15]. Coming to 3rd stage overhead balancing is limited the complex operations and provide the less path function. Stage coming to 4th stage balancing is adjusted through time slot analysis it simple adjustment functions. This function minimizes the samples rate and improves the speed of operations. At final stage low power functionalities generated by proposed reversible logic gates.

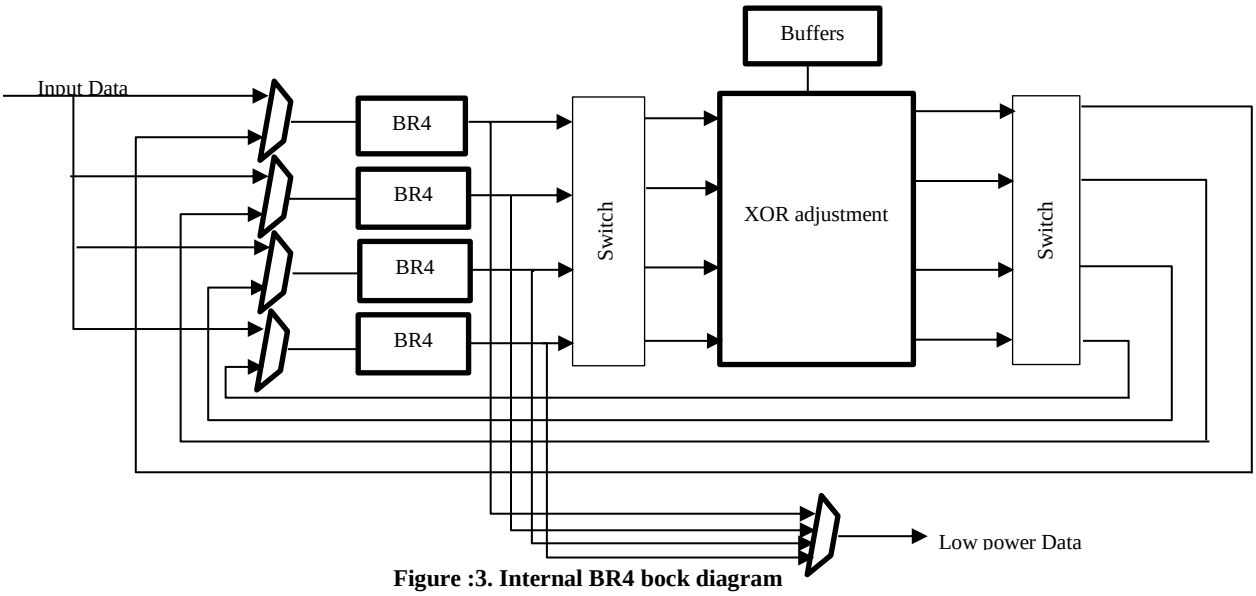

Figure :3. Internal BR4 bock diagram

The figure 3 clearly explains about internal block diagram of BR4 proposed reversible logic design. In this input data is collected from different modules in the VLSI chips. this input frames are converted into samples and process should for Bram elements, these are one type of buffers which can process the differentiated samples and send output to br4 modules[16-17].

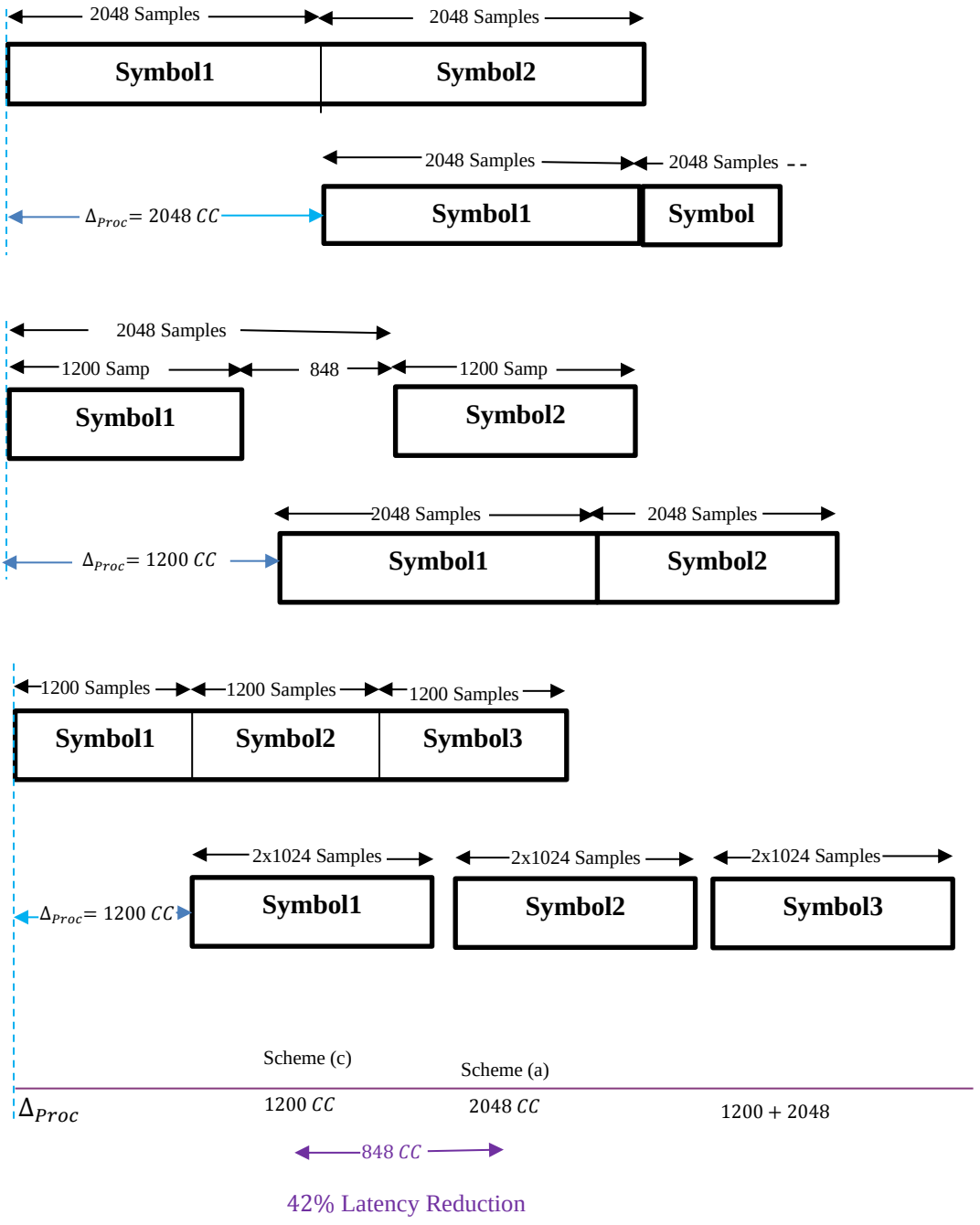

Figure. 4. An Example flow of BR4 technique.

The BR4 techniques are evaluated through switching module and send them to Xor modules. In XOR performing the OLS operations through switching buffers at final low power operation is performed by proposed reversible logic gate. This can simplifies the operations and providing the less power and high speed operations [19-20].

Mathematical computations: BR4: algorithm

Step: 1 input sample collection

$$\frac{\delta}{\delta w_k}(\mathbf{1} - \boldsymbol{y_i}\langle \boldsymbol{x_i}, \boldsymbol{w}\rangle)_+$$

$$= \begin{cases} \mathbf{0}, & \boldsymbol{if}\, \boldsymbol{y_i}\langle \boldsymbol{x_i}, \boldsymbol{w}\rangle \geq \mathbf{1} \\ -\boldsymbol{y_i x_{ik}}, & \boldsymbol{else} \end{cases}$$

Step: 2 weight balancing with BR4 technique

$$\mathcal{W} = \boldsymbol{\mathcal{W}} - \boldsymbol{\alpha}.(\mathbf{2}\boldsymbol{\lambda w})$$

Step: 3 variable adjustment

$$\mathcal{W} = \boldsymbol{\mathcal{W}} + \boldsymbol{\alpha}.(\boldsymbol{y_i}.\boldsymbol{x_i} - \mathbf{2}\boldsymbol{\lambda w})$$

Step: 4 arithmetic operations

$$MUL_a = 12N_x + 6N_a + 6L_0 + 2N_n + 12N_m + 18.N_h + 28N_f$$

Step: 5 Reduction of operations

$$CPA_a = 12N_x + 18.N_h + 28N_f$$

$$REG_a = 24N_d$$

Step: 6 stop the process

The above algorithm easily reduces the complex operations and providing the low path functionality through variable balancing technique. In the step one input samples are collected and valid through weight estimation operation. In this differentiation gives the maximum and minimum values of tracking point. Coming to step 2 weight balancing is performed with proposed br4 technique. At step 3 variables are adjusted with Alpha element and lambda is decreasing the error tolerance via logical operations. In step 4 arithmetic multiplications and additions easily operated by normalized length functions. Coming to step 5 noise reduction and path overhead reduction has been performed through CPA differentiation finally stop the process[21-24]. It relates with the accompanying components like: Capacitance per hub diminishes by ”30%”, VLSI applications increments by ”2X”, module estimate develops by ”14%” (Moore’s Law), Supply Voltage decreases by ”15%” and Frequency Increases by ”2X”. To meet these issues moderately”2.7X” dynamic-power will increment. Spillage/Leakage-Power: To take care of recurrence demand Vt will be scaled which comes about high spillage control. A low voltage/low edge innovation and circuit configuration approach, focusing on supply voltage around 1V and working with diminished edges. Dynamic power administration methods, diff ering supply voltage and execution speed as indicated by the action estimation. Low power interconnect, utilizing advance innovation, diminished swing or action approach show in fig.4

IV. RESULTS

Using BR4 technique low power, Applications are performed which is shown in clearly in the following outcomes. The designed functional diagram is clearly shown in following figure 5 in this input Bram, data flowing module, simple adjustment models, latency reduction modules are playing important key role.

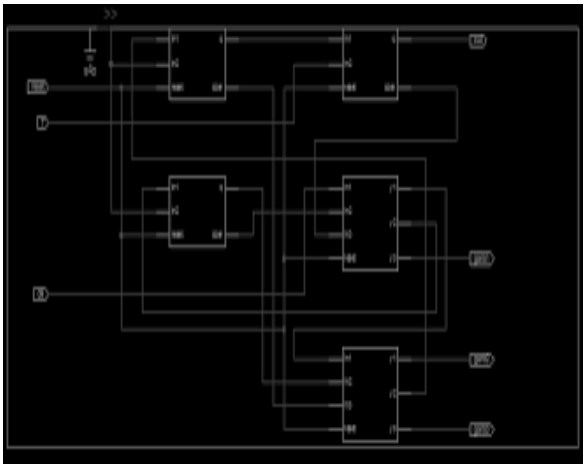

Figure: 5 designed BR4 technique

In this aimed that grant BR4 execution schemes are advancement and consumes determined power vitality near the front-end design through overall components. At this model more points are ' 100nm' advancement and control usage as a result of leakage. The above diagram operated with single clock and flip flop with sequential circuit. The sequential clock continuously monitors the delay overheads and complexity overheads through controller and minimize the reset operation. It is very near to mealy operation via FSM model using different types of factors this FSM is controlled with 6 rules. Where X is an material alphabet, Z is production alphabet, S is the state of apparatus, s0 is the set state which attend the starting $work\ (\delta: x\ S \rightarrow S), and\ \lambda\ (x;\ s)\ is\ output\ (\lambda: x\ S \rightarrow Z)$

Table: 1 power analysis

BR4 reversible gates	128 - 2048		
Die Size (um^2)	420 X 460		
Core Size(um^2)	78978	Combinational	140258
		Non-combinational	15589
		SP Memory Blocks (2136 Words)	49968
Core Power(mW)	15.102	Combinational	1.789
		Non-combinational	6.125
		SP Memory Blocks (2136 Words)	8.21

The table 1 explain about Power analysis of proposed reversible gates in this core size and core power can be evaluated through combinational and non-combinational flip flops. The memory blocks and a non-combinational memory blocks continuously divides the available samples into 22136 quotes. This model gives the accurate result compared to existed works.

Figure: 6 BR4 outcomes

The figure 6 explains about waveform representation of proposed reversible gate outcomes. In this 6a has more power consumption and consumes more area. In figure 6b proposed attains less power and less area. In terms of time delay compared to existed method proposed method less delay and suitable for high speed applications therefore this work is applicable to high speed VLSI chip and low power applications. With this model we can achieves the good performance measures such as accuracy, throughput power and delay.

Table: 2 comparison of results

Parameters	[13]	[14]	[10]	Proposed BR4
Latency (us)	7.78 $(3.89)^2$	2.56 $(5.12)^2$	0.83 $(6.64)^2$	4
Area (mm^2)	0.414	3.6	0.212	0.08
Gate Count (kGE)	445	-	-	181
Norm. En/FFT (nJ)	391.8 $(173.1)^2$	77.2	63.9^2	51
Memory Size $(word)^4$	4095 $(2047)^2$	1534 $(3070)^2$	1020 $(2044)^2$	2136
Throughput (GS/s)	0.526	0.8 $(0.4)^2$	0.128 $(0.03)^2$	0.6
Power (mW)	78.1 $(69)^2$	60.3	17.02	15.1
F_{max} (MHz)	526.32	400	320	300
Process (nm)	40	65	55	28

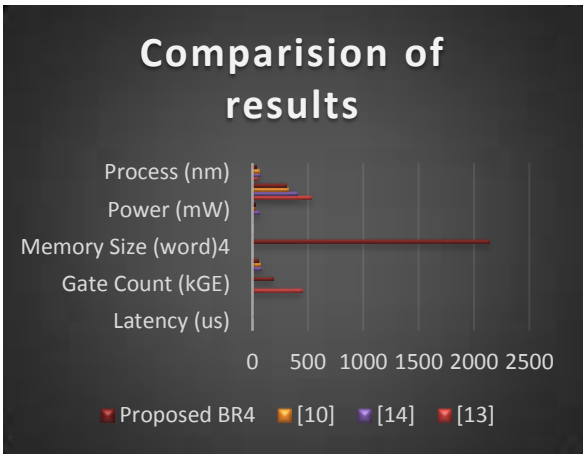

Figure: 7. Comparison of results

Table 2 and figure 7 clearly explains about comparison of results with existing models. In this latency area get count, FFT count, memory size, throughput, power, processing, and area, has been estimated. At final conditions proposed BR4 model achieves more improvement and results are outperforms the performance measures. The latency is improved by 4 percentage area is improved by 0.8 % gate count is improved by 9 % and throughput is increased by 60 %. At final power and processing area increased by 15 % and reduced by 29 % respectively which are shown in above graphical representations clearly.

V. CONCLUSION

In this research work proposed br4 reversible technique is designed using cadence tool. The area power and throughput have been improved compared through adjusted reversible technique. The symbol count and vector count can be reduced through proposed VLSI design, it can reduce the gate count and memory size. This work is more suitable for time and overhead reduction VLSI chips. The latency is improved by 4 percentage area is improved by 0.8 % gate count is improved by 9 % and throughput is increased by 60 %. At final power and processing area increased by 15 % and reduced by 29 % respectively which are shown in above graphical representations clearly.

REFERENCES

[1] Mahalakshmi, R., Sasilatha, T.: "*A power efficient carry save adder and modified carry save adder using CMOS technology*". In: 2013 IEEE International Conference on Computational Intelligence and Computing Research (ICCIC), pp. 1–5 (2013)

[2] Bruce, J., Thornton, M., Shiva kumaraiah, L., Kokate, P., Li, X.: "*Efficient adder circuits based on a conservative reversible logic gate*". In: Proceedings of the IEEE Computer Society Annual Symposium on VLSI, 2002, pp. 74–79 (2002)

[3] Parhami, B.: "*Fault-tolerant reversible circuits*". In: Fortieth Asilomar Conference on Signals, Systems and Computers, ACSSC'06, Oct 2006, pp. 1726–1729 (2006)

[4] Kaur, P., Dhaliwal, B.: "*Design of fault to learnt full adder/subtractor using reversible gates*". In: 2012 International Conference on Computer Communication and Informatics (ICCCI), Jan 2012, pp. 1–5 (2012)

[5] S.M. Swamynathan, V. Bhanumathi, "*Stability Enhancing SRAM cell for low power LUT Design*", Microelectronics Journal 96 (2020) 104704.

[6] M. Rangari, R. Saraswat, R. Jain, "*Design of reversible logic ALU using reversible logic gates with low delay profile*", International Journal of Advanced Research in Computer and Communication Engineering 4 (2015) 344–348.

[7] K. Kaur, A. Noor, "*Strategies & methodologies for low power VLSI designs: a review"*, International Journal of Advances in Engineering & Technology 1 (2) (2011) 159.

[8] P.K. Lala, J.P. Parkerson, P. Chakraborty, "*Adder designs using reversible logic gates"*, WSEAS Transactions on Circuits and Systems 9 (6) (2010) 369–378.

[9] S Karunamurthi, V.K. Natarajan, "*VLSI Implementation of Reversible Logic Gates Cryptography with LFSR key*", Microprocessors and Microsystems (2019) 68–78.

[10] T.N. Sasamal, A.K. Singh, A. Mohan, *"Efficient design of reversible alu in quantum-dot cellular automata*", Optik 127 (15) (2016) 6172–6182.

[11] K.B. Krishna, A.P. Ramesh, "*Implementation of sequential circuit using feynman and fredkin reversible logic gates*", Journal of Physics: Conference Series 1228 (1) (2019, May) 012047 IOP Publishing.

[12] A.V. Anantha Lakshmi, G.F. Sudha, "*Design of a reversible floating-point square root using modified non-restoring algorithm*", Microprocessors and Microsystems 50 (2017) 39–53.

[13] X.-Y. Shih, H.-R. Chou, and Y.-Q. Liu, *"Design and implementation of flexible and reconfigurable SDF-based FFT chip architecture with changeable-radix processing elements*," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 11, pp. 3942–3955, Nov. 2018.

[14] N. Le Ba and T. T.-H. Kim, "*An area efficient 1024-point low power radix-22 FFT processor with feed-forward multiple delay commutators*," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 10, pp. 3291–3299, Oct. 2018.

[15] Saikumar, K., & Rajesh, V. (2020). "*Coronary blockage of artery for Heart diagnosis with DT Artificial Intelligence Algorithm"*. International Journal of Research in Pharmaceutical Sciences, 11(1), 471-479.

[16] Dr. K. Raju, Kanisetty Swathi, P. Sampath Kumar, K. Saikumar, Mr. A. Sampath Dakshina Murthym. (2020). "*Implementation of Low Power Cam Interface for Fault Tolerant Data Access Technique*". International Journal of Advanced Science and Technology, 29(06), 3435 - 3443. Retrieved from http://sersc.org/journals/index.php/IJAST/article/view/14142.

[17] Saba, S.S., Sreelakshmi, D., Sampath Kumar, P., Sai Kumar, K., Saba, S.R.(2020) "*Logistic regression machine learning algorithm on MRI brain image for fast and accurate diagnosis*" International Journal of Scientific and Technology Research. VOLUME 9, ISSUE 03, MARCH 2020.

[18] Vijetha, A., Shashirekha, T., Raju, K., Rooban, S., Saikumar, K. (2020). "*A robust fake currency detection model using ESVM machine learning technique*". Journal of Advanced Research in Dynamical and Control Systems 12(06), 170-179.

[19] Raju, V & Devi, G & Sampath, A & Achanta, Sampath & Saikumar, K & Jagan, B.Omkar. (2020). "*HEART DISEASES CLASSIFICATION AND FEATURE EXTRACTION BY SEGMENTATION AND MACHINE LEARNING MODEL*". 24. 8992-9001.

[20] Aamani, Ravada & Vannala, Adinarayana & Sampath, A & Achanta, Sampath & Saikumar, K & Jagan, B.Omkar. (2020). "*HEART DISEASE DIAGNOSIS PROCESS USING MRI SEGMENTATION AND LASSO NET CLASSIFICATION ML*". 7. 717-721. 10.31838/jcr.07.06.125.

[21] Posiyya, A., Saikumar, K.(2020). *"Data management by librarian for academic and research perceptions*". International Journal of Psychosocial Rehabilitation 24(8) 545-551.

[22] Soumya, N., Kumar, K. S., Rao, K. R., Rooban, S., Kumar, P. S., & Kumar, G. N. S. "*4-Bit Multiplier Design using CMOS Gates in Electric VLSI*". International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-8 Issue-2, July 2019.

[23] Raju, K., Pilli, S.K., Kumar, G.S.S., Saikumar, K., Jagan, B.O.L.(2019). "*Implementation of natural random forest machine learning methods on multi spectral image compression*", Journal of Critical Reviews6(5), pp. 265-273