International Journal of Engineering Trends and Technology
ISSN: 2231 – 5381 /doi:10.14445/22315381/IJETT-V70I3P227

Volume 70 Issue 3, 241-248, March 2022
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Original Article

Robust Schmitt Trigger-based Performance Booster Technique for Futuristic On-Chip Graphene Interconnects

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Abstract - *For compactly high-speed and dense nanoscale integrated circuits (ICs), it is essentially on-chip interconnects rather compared to the devices that govern the performance of the chip. At nanometer-regime, the performance of existing widely used copper on-chip interconnect is adversely affected by varying limiting effects such as sidewall and grain boundaries scatterings. Subsequently, efficient and prospective graphene is investigated as one of the most promising contenders for on-chip interconnect materials. One of the most common strategies for addressing on-chip signal deterioration caused by long interconnects is repeater insertion. CMOS inverter-based buffer has been proposed as a prominent repeater circuit by many researchers. However, these conventional buffers have a high switching time that cumulatively adds up the overall signal delay. To mitigate this issue, a novel CMOS Schmitt trigger-based booster for contemporary futuristic graphene-based nanowires has been proposed in the present paper so as to attain better signal restoration, lesser delay and power reduction. The several analyses performed in this paper show that graphene interconnects with Schmitt trigger gives on average 45% of speed improvement and average power reduction of 40% with respect to conventional CMOS inverter-based buffer design. Also, the efficiency of Schmitt trigger circuits has been verified at varying different technology nodes.*

Keywords - *Copper interconnects, Graphene interconnects, Repeater Insertion, Schmitt Trigger, VLSI technology.*

I. INTRODUCTION

Perpetual advancements in VLSI circuit technology have led to the development of compact chips that is embedded with millions of transistors, devices and interconnections. Based on ITRS (international technology roadmap for semiconductors), with the technology advancement, the future devices in the nano regime will contain billions of transistors and will run at clock frequencies over several GHz ranges [1]. Hence distributing reliable and robust signals such as clock, power, ground, address, data etc., through on-chip interconnects in such high-speed, densely populated and complex environments shall be an extremely challenging task. As a result, on-chip interconnections play a critical role in determining integrated system size, power consumption, and clock frequency. Interconnects have parasitic capacitance, resistance, and inductance due to their finite geometric dimensions. Signal degradation, skin effect, crosstalk, and propagation delay are all challenges caused by interconnecting parasitics [2]. These pervasive non-ideal effects have emerged as critical determinants of great performance at advanced and miniaturised technology nodes. As a result, on-chip interconnect performance analysis and research of novel approaches to improve their utility have become critical.

Interconnects can be categorized as global, intermediate and local based on the length of interconnects. On-chip local interconnects connect sources, drains and gates of the transistors. Local wires are short in length and occupy the first few metal layers in the multi-level integrated system. The length of local interconnects typically scales down with the miniaturization of technology [3]. Intermediate wires connect different functional blocks to each other that typically span lengths up to a millimetre. Global wiring provides power, ground, clock, and control signals to whole chip modules. Top layers are referred to by global wires, which are a few millimetres long. In miniaturised ICs, global interconnect wire length rises in proportion to die size and is the primary cause of propagation delay and signal degradation [3],[8],[11].

The vital system performance that deals with parameters such as delay and power dissipation have always been a concerning factor in integrated circuits. With a longer length of interconnects, the delay becomes quadratically proportional to the length of interconnecting [4]. To mitigate this problem, several pieces of research have been performed [3], [15]-[17]. Long global interconnects create non-ideal effects, and buffer insertion has been researched as one of the effective strategies to resolve these issues. Repeaters are

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positioned in amid of lengthy wires by segmenting them into small portion in the buffer insertion technique in order to maintain signal intensity. Because propagation delay rises with interconnecting length, splitting the interconnect line into small portions is an effective way to reduce system latency caused by interconnects. In high-performance integrated systems, however, the number of repeaters might be much higher for global cables. Conventional CMOS buffer insertion technique has certain benefits but results in increased power dissipation that impacts the overall system performance. To address this issue, conventional buffers can be replaced by CMOS based Schmitt trigger buffer for signal restoration, improved power delay product (PDP), and energy-efficient global interconnect system [3].

Initially, with the evolution of integrated circuit technology, Aluminium (Al) had been the designers' choice as interconnect metal material and silicon dioxide (SiO_2) as an intro-level dielectric material. Copper (Cu) exhibits approximately half the resistivity (1.68×10^{-8} Ω.m) compared to aluminium, which has a resistivity of (2.65×10^{-8} Ω.m) and exhibits relatively lesser electromigration effects. Consequently, Cu has proven to be a better VLSI interconnect material due to its high melting point (1357 K) compared to Al (933 K) [5].

Subsequently, with the increasing packaging density of transistors and interconnects, the cross-sectional dimensions of Cu have been reduced rapidly. This resulted in its reduced dimensions, which are of the orders of the electron mean free path (i.e., nearly 40 nm in copper at room temperature). Moreover, the resistivity of copper interconnects has been increasing due to the factors such as increased surface and grain scattering, wide interconnect lengths and high speed of operation. This escalating resistivity of copper possesses several reliability concerns, such as increasing current density in compact interconnects and reduced thermal conductivity in low-k dielectrics [8]. The increased Joule heating also escalates electromigration induced voids and hillocks formation. Therefore, due to limitations imposed by copper interconnects such as power dissipation, signal degradation, skin effect and electromagnetic interference at high frequencies, researchers are looking for serious refinements in copper interconnect technology. In order to alleviate such problems, the incorporation of high-end materials such as graphene has been proposed by many researchers [5]-[9]. The next section in this paper discusses the newer applicable interconnect materials for future VLSI applications.

II. BACKGROUND

Graphene has emerged as a potential material for advanced ICs' on-chip wiring. Researchers have extensively investigated several structures of graphene as carbon nanotubes (CNTs) and graphene nano-ribbons (GNRs). These structures have attractive prospects in various applications, including interconnects and devices in the nanoelectronics regime. CNT possesses a circular structure, while GNR has a planar structure. Due to the planar configuration and ease of fabrication of GNR, it is widely used. It has been reported in [7] that GNRs will excel in performance than Cu interconnects for smaller widths. This is because a GNR sheet possesses nearly 25 times higher electron mean free path than copper. GNRs can carry considerably large current densities. These also offer comparatively high carrier mobility (105 $cm^2/V.s$) that is approximately 3000 times greater than Cu [5]-[9].

A GNR is made up of a solitary carbon atomic layer in terms of physical structure. GNRs are characterised as an armchair (ac) or zigzag (ZZ), as shown in Fig. 1. GNR can operate as either semiconducting or metallic depending on the edge design. The edge-patterned armchair GNRs' semiconducting or metallic characteristics can be exploited. This is determined by the number of carbon atoms present over the GNR's width. The zigzag edge of GNR, on the other hand, is inextricably linked to metallic properties [7]. Electrical wire models are used to analyze the parasitic effects of interconnects. The real behaviour of interconnect wire is estimated and approximated as a function of its R, L and C parasitics. The analytical model of interconnect can be classified as a lumped and distributed model, as shown in Fig. 8.

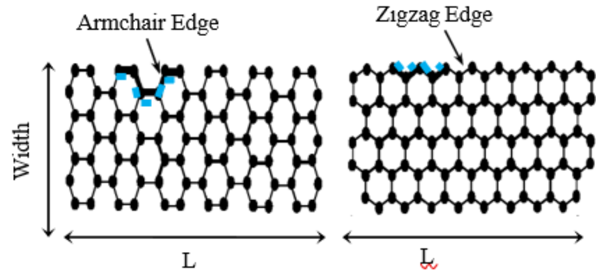

Fig. 1 Types of GNRs: armchair (left) and zigzag (right)

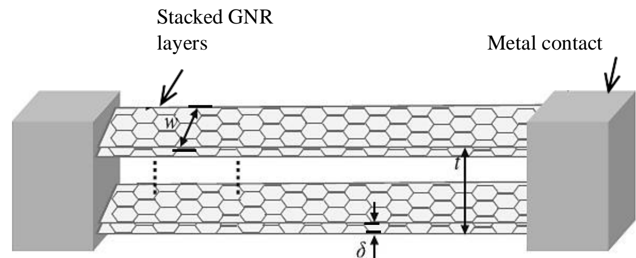

Fig. 2 The MLGNR interconnect system's geometric anatomy

Single-layer GNR is GNR with only one layer (SLGNR). When two GNRs are placed one on top of the other, it is referred to as a double layer GNR (DLGNR). Multilayer GNR is defined as multiple layers of GNR arranged in a stack structure with a least Vander Waals gap (i.e. 0.34 nm) among the intermediate layers (MLGNR). For interconnect applications, MLGNRs are the best choice. This

is because MLGNR has a lower impedance and greater current conduction than SLGNR [5]-[7]. The geometric depiction of MLGNR interconnect is shown in Fig. 2, which contains the number of layers (N), the distance between two layers Vander Waals gap ‘δ’, the width ‘w’, and the thickness ‘t’ [4], [5], [7].

GNRs can also be classified based on the number of layers present. MLGNR's total number of layers ($_{Player}$) can be calculated as follows:

$$N_{layer} = 1 + Integer(t) \quad (1)$$

Without altering lattice properties of GNR, an armchair GNR behaves as a semiconductor if a number of carbon atoms are 3k or 3k + 1, while it acts as metallic for total carbon atoms at its width as 3k + 2, where k is an integer [10]. Fig. 3 (a) shows the band structure of 24 carbon atom wide semiconducting GNR, while Fig. 3 (b) illustrates for 23 carbon atom wide metallic GNR. The energy gap in armchair GNR band structure can be evaluated [10] as,

$$E_n = \hbar . \frac{v_f}{2w}[k + \beta] \quad (2)$$

where E_n is energy gap, β is 0 for metallic GNR, and 0.33 for semiconducting GNR, $_{of}$ = 8 × 10^5 m/s is fermi velocity of graphene, ħ is Planck’s constant, k is an integer, and w is the width. It is evaluated that 0 and 0.2 eV are bandgaps in the case of metallic and semiconductive GNRs. This is demonstrated in Figs. 3 (a) and (b) respectively.

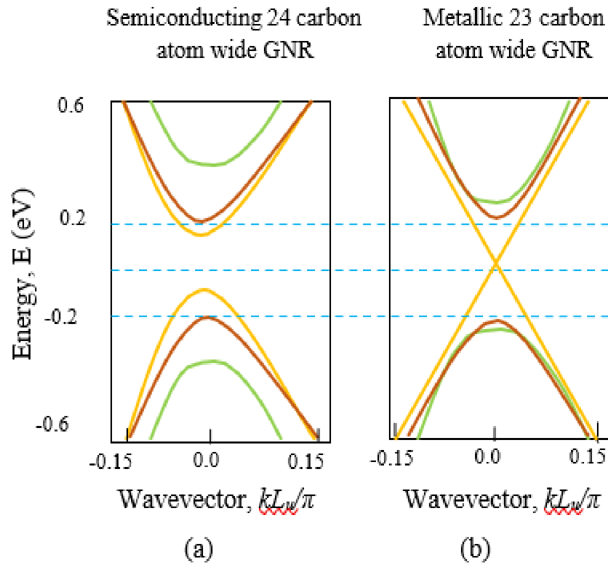

Fig. 3 Wavevector versus energy relationship represents band structure of (a) semiconductive GNR, *w* = 6.02 nm (24 atoms wide) and (b) armchair GNR as metallic, *w* = 5.78 nm (23 atoms wide) [5]

In the present paper, with the fascinating GNR on-chip interconnects, buffer insertion techniques have been explored, and an efficient buffer for the same has been proposed. This is systematically presented in the next section.

III. REPEATER INSERTION

To mitigate the graving non-ideal issues caused by the long length of interconnects, the buffer insertion technique has been adopted in the present work. In VLSI ICs, the buffer insertion technique is the most widespread and efficient technique [12]-[17]. In this technique, buffers (repeaters) are inserted at regular intervals of the distance across long interconnects in order to improve signal integrity and performance. Conventionally, CMOS buffers are used due to their ability to enhance the speed of the system [11]-[16].

The demerit of CMOS buffers is that these consume significant power from the chip power supply. To address this issue, CMOS buffers are replaced by power-efficient Schmitt trigger buffers [3]. In the Schmitt trigger buffer circuit, power can be efficiently reduced, and signal restoration can be performed. The incorporation of Schmitt trigger based buffers has been investigated with global copper on-chip interconnects. However, this has been sparsely explored for graphene interconnects. Henceforth, this has been energetically taken up in this research work. In the next subsections, conventional CMOS buffer, prospective Schmitt trigger buffer and parasitic extraction of advanced graphene interconnects are discussed.

The conventional CMOS buffers usually have a switching threshold value near around $V_{DD}/2$. They are not able to respond to very small changes in the input signal. However, a prospective Schmitt triggers based buffer can be designed in such a way to get a switching threshold value much lesser than $V_{DD}/2$. Hence, this can switch and operate at higher speeds.

A. Conventional CMOS buffer

Fig. 4 represents the circuit of buffer based on CMOS inverter design.

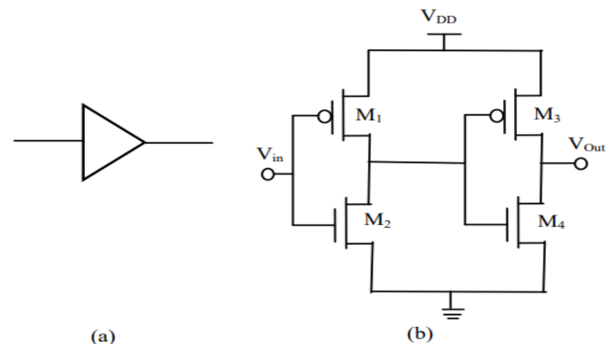

Fig. 4 Schematic represents (a) Symbol and (b) Circuit of CMOS buffer

The efficiency, noise immunity and signal integrity of the on-chip system can be well assessed using noise margin. Noise margin defines the maximum noise that a circuit can tolerate. The DC transfer characteristics to evaluate the noise margin of the CMOS inverter is shown in Fig. 5. The noise margins of CMOS inverter are evaluated from Fig. 5 as [2],

$$NM_H = V_{OH} - V_{IH} \quad (5)$$

$$NM_L = V_{IL} - V_{OL} \quad (6)$$

where NM_H and NM_L are high noise margin and low noise margin, respectively, V_{OH} and V_{IH} represent logical high and low outputs, V_{IH} and V_{IL} are logical high and low inputs, respectively. From the figure for the CMOS inverter, V_{OHmin} is closer to the power supply voltage, and V_{OLmax} is closer to zero. Therefore,

$$NM_H \approx V_{DD} - V_{IH} \text{ and } NM_L \approx V_{IL} \quad (7)$$

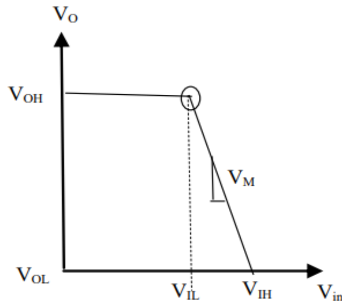

Fig. 5 Noise margin representation on DC transfer characteristics of CMOS inverter

The other limitation of the CMOS inverter is its high power consumption. Power consumption of inverter comprises of dynamic, static and short-circuit components [2]. During the switching or transition of signals, dynamic power is dissipated. Dynamic power is quadratically dependent on the supply voltage. Static power is consumed at the steady-state operation of the inverter. Another component of the power dissipation is the short circuit. In a few instances, i.e. around $V_{DD}/2$, both PMOS and NMOS transistors are momentarily in ON state. The power dissipation during this duration is referred to as a short circuit, and a significant amount of power is dissipated from the power supply. Hence, under high speed operating conditions, it is necessary to develop a circuit that can effectively operate to avoid simultaneous switching of transistors. This can be achieved with the aid of a CMOS Schmitt trigger based buffer circuit.

B. CMOS based Schmitt trigger buffer

The symbol and circuit of the Schmitt trigger are shown in Figs. 6 (a) and (b), respectively. Its DC transfer characteristics are shown in Fig. 7. The significant difference between Schmitt trigger and CMOS buffers is in the DC transfer characteristics, as shown in Figs. 5 and 7, respectively. These figures reveal that CMOS buffer has a single switching threshold while Schmitt trigger operates on two varying switching thresholds for input signal going in positive and negative directions. The Schmitt trigger buffer is more sensitive to noise and hence attributes higher noise immunity compared to its conventional CMOS buffers as it can detect and operate at lower thresholds. This distinguished quality of Schmitt triggers built immunity towards unwanted noise.

The Schmitt circuit (as shown in Fig. 6 (b)) is basically an inverter circuit (double transistor inverter) with two extra transistors, M_3 and M_6, used for providing positive feedback and in turn exhibit hysteresis. In the Schmitt trigger circuit, the output voltage maintains its magnitude until the changes in the input signal sufficiently trigger a change. The Schmitt trigger behaves as a bistable multivibrator and possesses characteristics of memory like latch or flip-flop. The operation of the CMOS Schmitt trigger is demonstrated with the help of Fig. 6 (b).

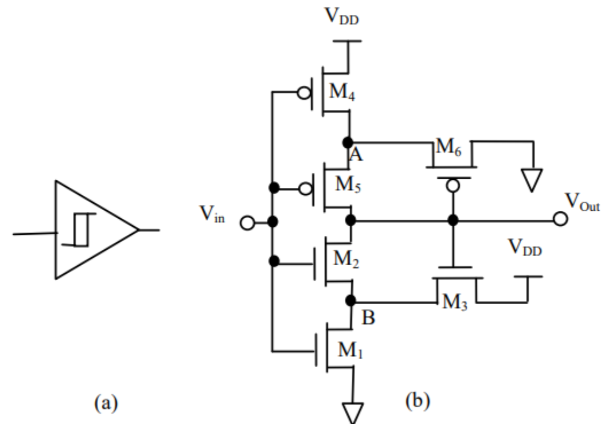

Fig. 6 Illustration of (a) symbol, (b) circuit diagram of CMOS Schmitt Trigger buffer

Initially, it is considered that V_{out} is at a HIGH state. So transistor M_3 is ON, and M_6 is OFF; hence node A is floating at V_{DD}-V_{TN3}. When the input changes from 0 to V_{DD} and crosses the threshold voltage of M_1, it gets ON. But to pull down output voltage to GND, M_2 has to be ON. For this, input has to cross the barrier voltage of V_{DD}-V_{TN3}. Thus, the switching threshold of the circuit under this condition will be higher than $V_{DD}/2$. On the contrary, for LOW output voltage M_6 will be in ON state and pull-down node A to GND. In this condition, to pull up output voltage, HIGH state M_5 needs to be active will be conducted only when the input goes below zero voltage level. Therefore, Schmitt's trigger with this kind of intelligent switching exhibits typical hysteresis behaviour and is shown in Fig. 7. This type of hysteresis operation avoids both pull up and pull-down networks switching simultaneously, hence consuming less power than that of CMOS inverter-based buffer circuit.

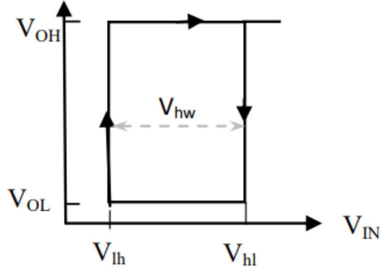

Fig. 7 DC transfer characteristics of Schmitt trigger buffer

Here V_{OH} and V_{OL} are logic high and low output voltages, respectively. V_{hl} and V_{lh} are logic high and low input voltages, respectively. V_{iew} denotes the hysteresis width. V_{hl}, V_{lh} and V_{hw} are computed as,

$$V_{hl} = V_{DD} - \frac{RV_{TN}}{R+1} \quad (9)$$

$$V_{lh} = \frac{RV_{TP}}{R+1} \quad (10)$$

$$V_{hw} = V_{hl} - V_{lh} = \frac{V_{DD} - R(V_{TN} - |V_{TP}|)}{R+1} \quad (11)$$

Where V_{TN} and V_{TP} represent threshold voltage of NMOS and PMOS transistors respectively and $R = \sqrt{(\beta_n / \beta_p)}$, β_n and β_p correspond to transconductance parameters of NMOS and PMOS transistors, respectively.

C. Prospective MLGNR on-chip interconnects

In this section, eminent graphene-based MLGNR on-chip interconnects are discussed. The MLGNR interconnect having an electrical model comprising of distributed RLC segments is as shown in Fig. 8.

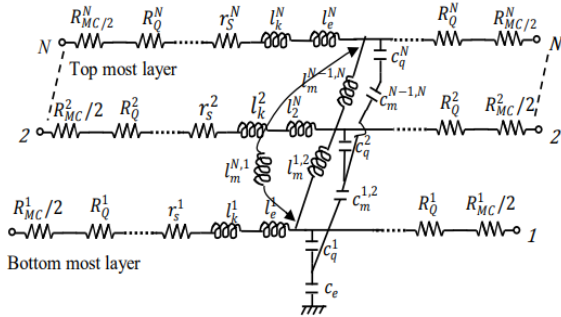

Fig. 8 MLGNR interconnect represented in multi-conductortransmission line model

The driver-interconnect-load (DIL) model is applied in this research, as illustrated in Fig. 9 (a), in which CMOS inverters are used as driver and load circuits, and the buffers are substituted by Schmitt triggers as per Fig. 9 (b). In this configuration, using MLGNR for global on-chip interconnect benefits in limiting the non-ideal behaviour for high-speed applications [18]-[27]. While using Schmitt trigger as buffer aids in boosting the overall performance for long interconnects.

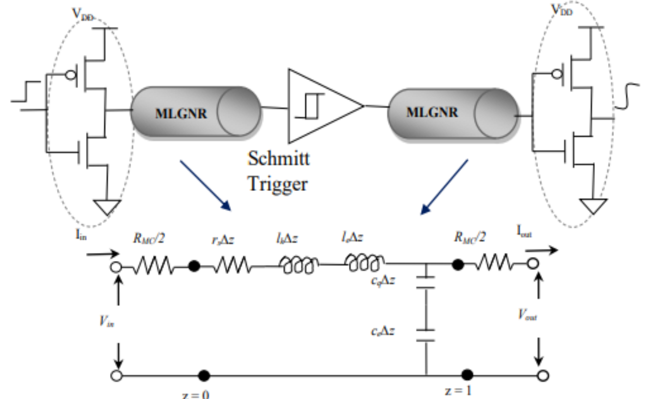

Fig. 9 DIL model using (a) MLGNR interconnect (b) model for buffer insertion with Schmitt trigger

IV. RESULTS AND DISCUSSION

In the current work, MLGNR interconnect is used. The width (w) and thickness (t) of MLGNR are 6.8 nm and 1 nm, respectively. The analyses are carried out at 22 nm technology. Performance analysis has been performed in two stages. Firstly, the performance of long interconnects is analyzed under various technology nodes. Secondly, performance and comparative analysis are implemented for Cu, and MLGNR interconnects. Various performance-based simulations are performed at different technology nodes. The effects of increasing the length of on-chip Cu and MLGNR interconnects are shown in Figs. 10 and 11. The length of the interconnect varies from 4 to 10 mm. The statistics indicate that as the length of the wire increases, the propagation delay increases. As a result, as the wire length grows longer, the system's performance suffers. It is also seen from Figs. 10 and 11 that the impact of signal distortion and delay is comparatively lesser for MLGNR interconnects for increasing lengths with respect to outputs of Cu interconnects. Therefore, to deal with the issue of degrading signal integrity at larger wire length, performance booster techniques such as CMOS based conventional buffer and Schmitt trigger are introduced and investigated.

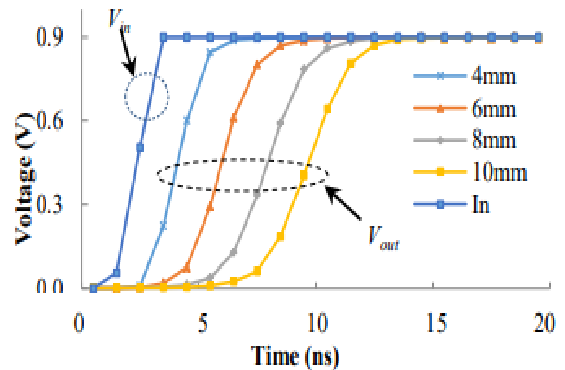

Fig. 10 Input-Output characteristics of Cu interconnect system for various interconnect lengths (viz. 4mm, 6mm, 8mm, 10mm) at 22nm technology node

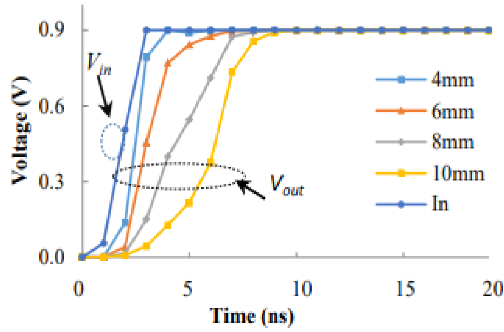

Fig. 11 Input-Output characteristics of MLGNR interconnect system for various interconnect lengths (viz. 4mm, 6mm, 8mm, 10mm) at 22 nm technology node

To validate the efficiency of the proposed work, three cases have been considered. In the first case, no buffers are used in between driver and receiver. In the second case, prominent Schmitt triggers are inserted in between long interconnects. While in the third case, instead of Schmitt trigger, conventional CMOS buffer has been tested. The different input and output waveforms for all the cases are shown in Fig. 12. A fast-rising edge input signal is applied to interconnect through the driver. So, in the ideal case, the signal received at the receiver-end of interconnecting should be the same signal as that of input. However, due to the presence of parasitic impedances, the strength of the signal gets degraded, and signal is obtained after a certain propagation delay. This latency in signal transmission can be up to a few nanoseconds. It is seen from the figure that signal integrity of the output signal with Schmitt trigger is comparatively better and higher than output signals without buffer and conventional CMOS buffers.

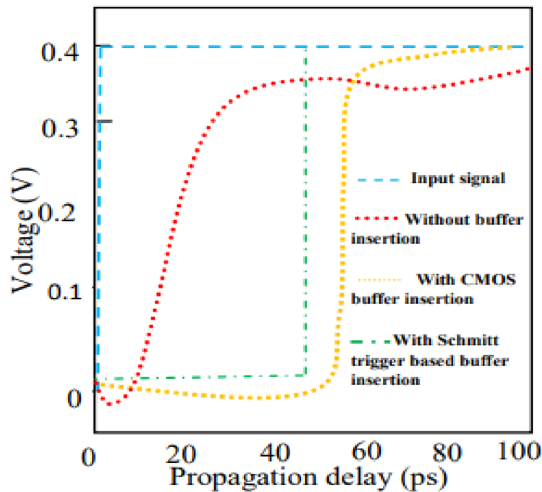

Fig. 12 Schematic representing (i) input waveform, (ii) case 1: delayed output waveform (without buffer insertion), (iii) case 2: output waveform (with buffer as Schmitt trigger) (iv) case 3: output waveform (with conventional CMOS buffer)

To assess further efficiency between different buffers (conventional CMOS buffer and prominent Schmitt trigger buffer) and to vary on-chip interconnect materials, transient response, delay, and power dissipation have been analyzed.

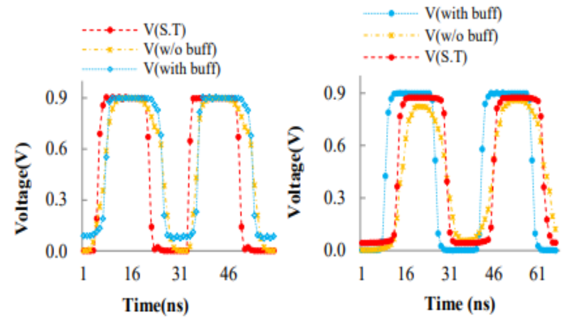

Fig. 13 Transient response of Cu (left) and MLGNR (right) interconnect without buffer, with CMOS buffer and with Schmitt trigger

Fig. 13 shows the transient response of Cu and MLGNR interconnects without buffer, with CMOS buffer (with buff) and with Schmitt trigger (ST), respectively. It is evident from Fig. 13 that Schmitt trigger-based buffer gives better output response than CMOS inverter buffer for MLGNR based system. The better performance of the Schmitt trigger is because of its faster switching action. It is identified from the output that delay in case of Schmitt trigger with MLGNR based system is 1.31 ns while delay in case of CMOS buffer and without buffer is 2.32 ns and 3.36 ns respectively at 22 nm technology node. Hence, delay in Schmitt trigger-based system has nearly 45% lesser delay than its counterparts. Also, it is seen that MLGNR based system performs better than a system working with copper interconnects. Next, power consumption in Cu and MLGNR interconnect without buffer, with CMOS buffer and with Schmitt trigger have been analyzed. As technology scales down, operating frequency tends to increase. This, in turn, increases switching actions resulting in higher power consumption. It can be clearly seen in Fig. 14 that as feature size shrinks from 180 nm to 22 nm, power consumption in interconnects increases. However, this increase in power consumption is significantly lower in the case of Schmitt trigger as buffer and MLGNR interconnects. It is evident from this analysis that approximately 45% power can be minimized using Schmitt trigger-based buffer in MLGNR interconnects as compared to copper and other buffer circuits. Hence proposed Schmitt trigger buffer insertion with MLGNR interconnects leads to power-efficient systems.

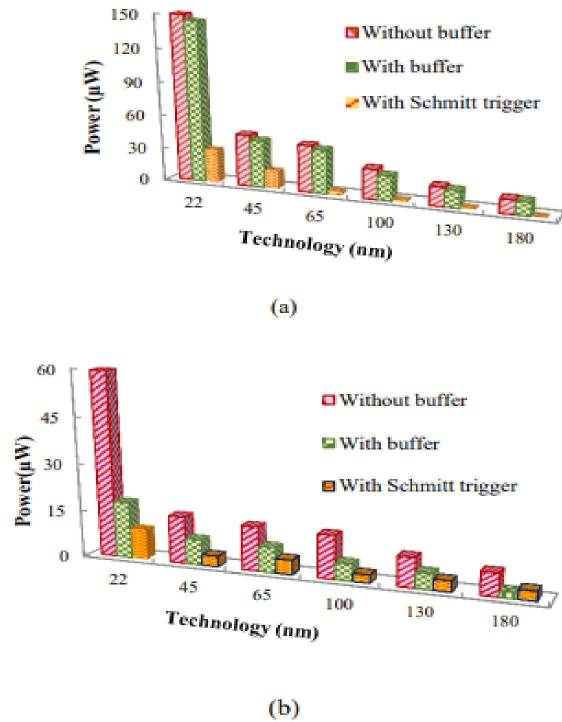

Fig. 14 Comparative power analysis of (a) Cu and (b) MLGNR interconnects without buffer insertion, with conventional CMOS buffer and with Schmitt trigger-based buffer insertion techniques

V. CONCLUSION

Prospective Schmitt trigger-based buffer insertion technique for futuristic graphene interconnects has been proposed to attain low power and high performance in integrated circuit designs. It is observed that in the driver-interconnect-load model, with the increase in length, delay increases, and signal integrity degrades considerably. To restrict these issues, different buffers such as conventional CMOS inverter-based buffer and potential Schmitt trigger-based buffer have been analyzed. It is observed that improved performance can be achieved with Schmitt trigger-based buffer than conventional CMOS inverter-based buffer insertion technique in advanced global MLGNR interconnects. Comparative delay and power analyses have been performed for copper, and MLGNR interconnects together with CMOS and Schmitt trigger-based buffer. It is computed that approximately 40% improvement can be achieved in delay and 45% power dissipation using Schmitt trigger-based buffer insertion technique. Also, it is envisaged that signal restoration is higher at global MLGNR interconnects as compared to its counterpart copper interconnects using the buffer insertion technique. Hence, MLGNR interconnect and Schmitt trigger buffer insertion techniques are effective high-end prospective design strategies to attain high performance in integrated circuits.

ACKNOWLEDGMENT

The authors express their gratitude to the SSRG journal committee 2022 for selecting the manuscript based on its suitability and henceforth enabling the updated manuscript to get the possible prospective publication in the international journal of engineering trends and technology (IJETT).

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