

# Design Approach for Decimation Filter for ADC Application

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**Abstract**— This paper presents a kind of design method about the decimation filter design for high performance ADC application. It was implemented and validated by simulation using MATLAB tool and its complete architecture was realized using DSP blockset and Simulink. A two-stage decimation filter architecture which can reduce digital switching noise was also introduced in this design. The FIR low pass filter is used for both the stages of the decimation filter as an anti-aliasing filtering process. The resulting architecture having increased computational efficiency, smaller size and high performance also it consumes less power as compared to conventional decimation filters. The design was simulated using MATLAB according to this scheme can achieve higher performances.

**Keywords**— Digital Decimation Filter, ADC, FIR low pass filter, Comparator.

## I. INTRODUCTION

Decimation is the process of reducing the sampling rate. In practice, this usually implies low pass-filtering a signal, then throwing away some of its samples. The most immediate reason to decimate is simply to reduce the sampling rate at the output of a system so the system operating at a lower sampling rate can input the signal. But a much more common motivation for decimation is to reduce the cost of signal processing such as calculation and memory required to implement a DSP system generally is proportional to the sampling rate, so the use of a lower sampling rate usually results in a cheaper implementation also computational efficiency and resolution of the output of ADC will be increased. The main task of a decimation filter is to remove the quantization noise away from the band of interest and avoid aliasing of high frequency components down to low frequency region or within the signal bandwidth. Decimation filters are used for digital-signal-processing (DSP) applications such as audio, music and video applications. There have been continuous efforts to improve the performance of digital decimation filters in terms of speed, hardware, and power dissipation. Hence, several techniques have been investigated to obtain high performance digital decimation filters. Li Hongqin states that the comb-FIR filter architecture is an efficient structure for the decimation filter [1]. The design of decimation filter using canonic signed digit (CSD) representation has been presented [2], [3]. Khalid describes the design and implementation of low power and hardware efficient decimation filter [4]. The comparison of different decimation architectures for high resolution sigma delta analogue to digital conversion was presented [5].

Generally there are many methods to design digital decimation filter, but conventional decimation filters are designed by VLSI with DSP processor or FPGA structure, but it has drawbacks with large sizes, it is also impracticable for hardware's cost due to large sizes. So it is beneficial to develop smaller size's filter than conventional decimation filter. With the development of electronic technology, some handy electronics device's bulk is more and more smaller, so the purpose of this design is to realize a kind of structure with smaller sizes and lower power. Especially this method is realized easily in hardware language in SOC ASIC design.

In this paper, we propose the design and implementation of decimation filter architecture using two stage decimation processes with FIR low pass filter in both stages used for high performance ADC application. The paper is organized as follows: In section II the proposed decimation filter architecture and its different stages is described. In section III the simulation results of the different stages of the decimation filter architecture is presented and section IV concludes the paper.

## II. DECIMATION FILTER ARCHITECTURE

In this paper the proposed decimation filter architecture was designed in order to improve computational efficiency and the performance of ADC. The combined operation of filtering and downsampling is called decimation. But the downsampling process will result in aliasing so we designed the proposed decimation filter architecture such that the overall aliasing and quantization noise will be removed. There are two major requirements for a decimation filter used in a delta-sigma ADC. The first is that the frequency response was designed to attenuate both out of band signals from the input to the delta sigma modulator and the modulator quantization noise sufficiently to meet the overall ADC performance objectives. The second is that the decimation filter's truncation noise must be sufficiently low to allow the overall ADC performance to meet the required specification. For this design, a linear-phase filter with greater than 90dB stop-band attenuation and less than 0.1dB pass-band ripple was developed. A decimation ratio of 128 supports sampling rates of 48 KHz, 44.1 KHz, 32 KHz and 8 KHz. To decrease power consumption of the filter, a multi-stage decimation process is designed to implement decimation filter in this design. FIR and IIR filters are generally used to meet the design specifications. FIR filters offer great control over filter shaping and linear phase performance with waveform retention over the pass band. Due to its linear phase response,

they are used in audio application as compared to IIR filters. So we designed the proposed filter architecture using FIR low pass filter.

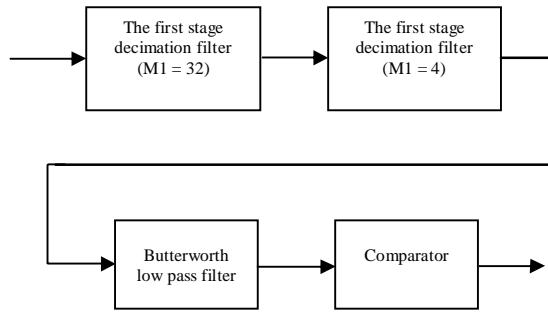


Fig. 1 Proposed decimation filter architecture

To efficiently perform the decimation, a two-stage decimation filter is used. The first stage filter decimates by 32, and the second stage filter decimates by 4. In addition, an optional low pass filter is designed to filtering DC offset. The digital decimation filter architecture used for this design is shown in Fig. 1. To reduce the hardware and the power consumption the decimation filter is used where the sampling frequency in each stage is reduced. The filter specifications of the proposed decimation filter are presented in table 1.

TABLE I  
DECIMATION FILTER SPECIFICATIONS

Decimation factor	128
Pass band frequency	20 KHz
Pass band ripple	0.01 dB
Stop band attenuation	90 dB
Cut off frequency	20.37 KHz
Output word length	16 bits

A. First-Stage Decimation Filter Design

The first stage filter accepts data at high sample rate, and performs the bulk of the decimation. Therefore, a simple structure is preferred to limit implementation size. The FIR filter is an excellent choice for the decimation filter due to their simple implementation and linear phase response characteristics and it can be designed easily. So the first stage decimation filter was designed. In this design decimation consists of two processes FIR low pass filtering process followed by the downsampling process with decimation factor of 32. The downsampling process will result in aliasing, in order to avoid the aliasing problem, a low-pass filtering process is needed in decimation. A 4<sup>th</sup>-order FIR low pass filter with cut of frequency of 20 KHz is designed to perform the decimation by 32. The decimation process for first stage was designed by writing the codes in the MATLAB. The design of the first stage decimation filter is shown in fig. 2

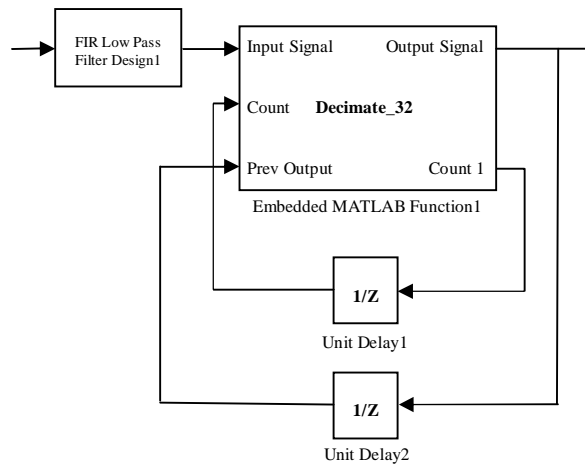


Fig. 2 First stage decimation by 32

B. Second-Stage Decimation Filter Design

The second-stage decimation filter performs the final decimation by 4 and compensates for the pass band droop of the first-stage decimation filter. A FIR low pass filter is implemented for the second stage decimation by 4. Figure 3 shows the design of second stage decimation by 4. Similar to first stage decimation process for this stage was also designed by writing the codes in the MATLAB. The design consists of two processes namely FIR low pass filter followed by downsampling block with decimation factor of 4.

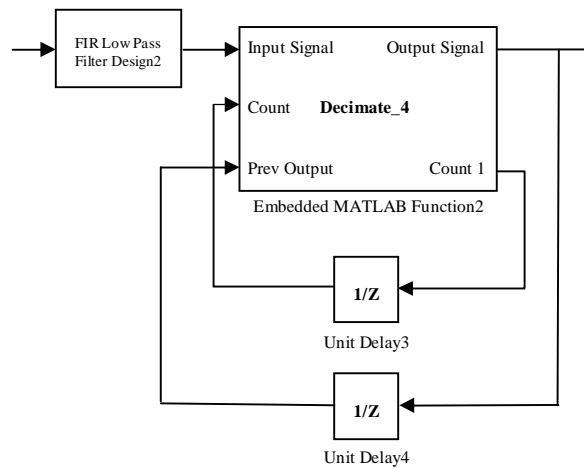


Fig. 3 Second stage decimation by 4

C. Low Pass Filter Design

The low pass filter passes low frequencies and attenuates high frequencies of the signal. For this architecture the butterworth low pass filter was designed after decimation stages. This low pass filter's design aims to filtering DC offset and smoothes the signal. The cut-off frequency of the LPF is 20.37 Hz at  $f_s=1$  kHz and also scales with sampling rates.

#### D. Comparator Design

The comparator is a device that compares two signals, one is the known signal called reference signal and other is input signal and produces the output a digital signal indicating which is larger. The comparators are commonly used in devices that measure and digitize analog signals. The comparator block was designed by writing codes in the MATLAB to get the digital output. The design of comparator block is shown in fig. 4.

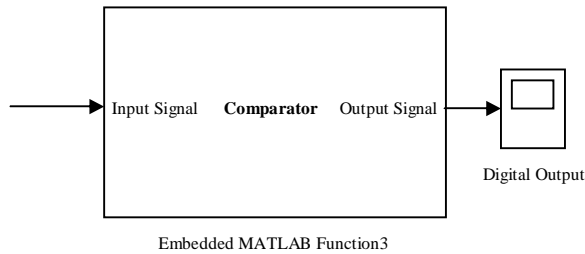


Fig. 4 Comparator Design

### III. SIMULATION RESULTS

In this project different stages of the decimation filter architecture was considered and simulated it by using MATLAB tool, and their outputs was observed for high performance A/D converter. The simulation results of different stages of the architecture are given below.

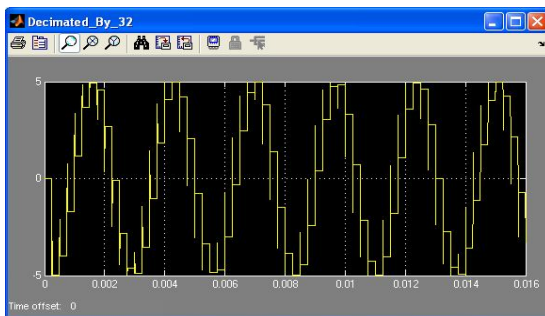


Fig. 5 First stage decimated output by 32

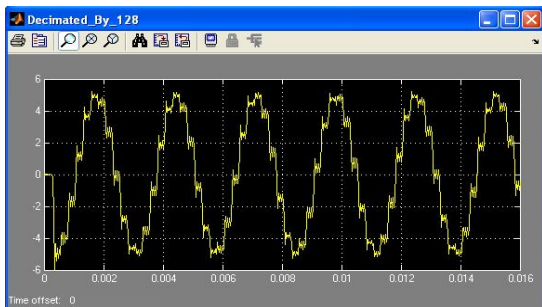


Fig. 6 Second stage total decimated output by 128

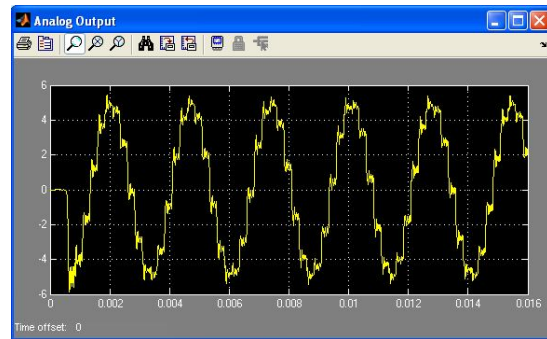


Fig. 7 Analog output signal

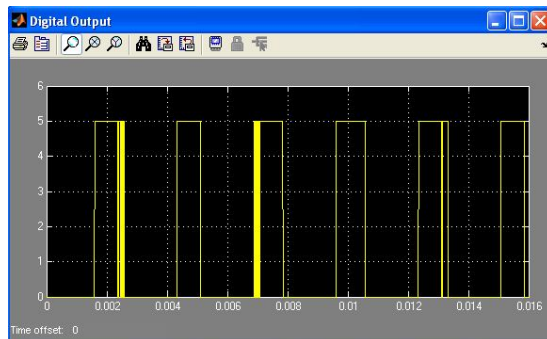


Fig. 8 Digital output signal

### IV. CONCLUSIONS

In this design, a complete digital decimation filter design procedure, from architecture optimization, to simulation implementation for ADC application was presented. This decimation filter achieved 16-bits of accuracy. The selection of the proposed decimation filter results in a smaller size, low power and high performance design compared to the conventional digital decimation filters, which were used for ADC in audio and music applications. The multi-rate multi-stage decimation filter structure reduces the power consumption and the hardware used for implementation. The advantage of the proposed decimation filter is that it has smaller size and consumes less power as compared to conventional decimation filters can be achieved.

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