Implementation of Adaptive Viterbi Decoder

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ABSTRACT
Viterbi algorithm is employed in wireless communication to decode the convolutional codes; those codes are used in every robust digital communication systems. Such decoders are complex & dissipiate large amount of power. Thus the paper presents the design of an Adaptive Viterbi Decoder (AVD) that uses survivor path with parameters for wireless communication in an attempt to reduce the power and cost and at the same time increase in speed. Most of the researches work to reduce power consumption, or work with high frequency for using the decoder in the modern applications such as 3 GPP, DVB, and wireless communications. Field Programmable Gate Array technology (FPGA) is considered a highly configurable option for implementing many sophisticated signal Processsing tasks. The proposed decoder design is implemented on Xilinx Spartan 3 , XC3S200 FPGA chip using VHDL code and Xilinx ISE 9.1 used for synthesis.

General Terms
Viterbi Algorith

Keywords
FPGA, VHDL, AVD, AWGN,DoD, VHSIC.

1. INTRODUCTION

Most digital communication systems nowadays convolutionally encoded the transmitted data to compensate for Additive White Gaussian Noise (AWGN), fading of the channel, quantization distortions and other data degradation effects. For its efficiency the Viterbi algorithm has proven to be a very practical algorithm for forward error correction of convolutionally encoded messages. The requirements for the Viterbi decoder or Viterbi detector depend on the applications used. Most of the researches work to reduce cost, the power consumption, or work with high frequency for using the decoder in the modern applications such as 3GPP, DVB, and Wireless communications. Some of them comparing between using FPGA, ASIC, and DSP to find which one is suitable for the applications, other studies the differences method for back trace unit to find the correct path, and the other trying to work with high frequency by using parallel operations of decoder units . The complexity of these decoders increased with the increasing of the constraint length. Thus, we attempts to;

1. Design an adaptive Viterbi decoder that uses survivor path storage with parameters for wireless communication.

2. Design and implement the decoder using Xilinx system generator modeling tool. Evaluate the decoder for timing accuracy and resource utilization.

VHDL stands for VHSIC Hardware description language. VHSIC is itself an abbreviation for very high speed integrated Circuit. This language was first introduced in 1981 for the Department of Defense (DoD) under the VHSIC program. In 1983 IBM , Texas instruments and intermetrics started to develop this language. In 1987 IEEE standardized the language. VHDL is a hardware description language. It describes the behavior of an electronic circuit or a system from which the physical circuit or system can then be implemented. VHDL is intended for circuit synthesis as well as circuit simulation. VHDL is programming language that allows one to model and develop complex digital system in dyanamic environment by dataflow, behavioral and structural style of modeling. The behavior of field programmable gate arrays can be illustrated by this language.

2. VITERBI ALGORITHM

Viterbi algorithm was devised by Andrew J. Viterbi (1967). The optimality and the relatively modest complexity for small constraint lengths have served to make the Viterbi algorithm the most popular in decoding of convolutional codes with constraint length less than 10. Viterbi algorithm is called as optimum algorithm because it minimizes the probability of error. The Viterbi algorithm is one of the standard sections in number of high-speed modems of the process for information infrastructure applicable in modern world. The unit of branch metric will calculate all the branch metrics and then processed to add compare for selecting the surviving branches as per the branch metrics finally the decoded data bits are generated by the trace back unit.

The algorithm can be broken down into the following three steps.

1. Weight the trellis; that is, calculate the branch metrics.

2. Recursively computes the shortest paths to time n, in terms of the shortest paths to time n-1. In this step, decisions are used to recursively update the survivor path of the signal. This is known as add-compare-select (ACS) recursion.

3. Recursively finds the shortest path leading to each trellis state using the decisions from Step 2. The shortest path is called the survivor path for that state and the process is referred to as survivor path decode. Finally, if all survivor paths are traced back in time, they merge into a unique path, which is the most likely signal path.

3. ARCHITECTURE OF VITERBI DECODER

The input to our proposed design is an identified code symbols and frames, i.e. The design decodes successive bit stream and the proposed decoder has no need to segment the received bit stream into n-bit blocks that are corresponding to a stage in the trellis in order to compute the branch metrics at any given point in time . The architecture of the viterbi decoder is illustrated in fig 3.1.

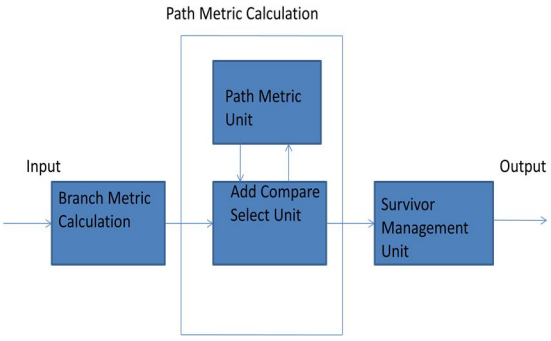

Fig 3.1 Basic building blocks of the Viterbi decoder.

The basic performance of the Viterbi decoder is analyzed with the block diagram shown below. It consists of three main blocks-

1. Branch Metric Calculation
2. Path Metric Calculation
3. Survivor Management Unit

3.1 The Branch Metric Calculation (BMC)

This is typically based on a look-up table containing the various bit metrics. The computer looks up the n-bit metrics associated with each branch and sums them to obtain the branch metric. The result is passed along to the path metric Calculation. The responsibility of this unit is to compute the Hamming code between the expected code and the receiving code as a frame. At each processing, the BMU finds the Hamming code for these symbols.

3.2 Path Metric Calculation

There are Path Metric Unit (PMU) and Add Compare Select Unit(ACSU) blocks in it.

3.2.1 Path Metric Unit (PMU)

It computes the partial path metrics at each node in the trellis.

3.2.2 Add Compare Select Unit (ACSU)

This ACSU is the main unit of the survivor path decoder . The function of this unit is to find the addition of the Hamming code received from BMU's and to compare the total Hamming code. This takes the branch metrics computed by the BMC and computes the partial path metrics at each node in the trellis. The surviving path at each node is identified, and the information-sequence updating and storage unit notified accordingly. Since the entire trellis is multiple images of the same simple element, a single circuit called Add-Compare-Select may be assigned to each trellis state.

3.3 Survivor Management Unit (SMU)

This is responsible for keeping track of the information bits associated with the surviving paths designated by the path metric Calculation. There are two basic design approaches: Register Exchange and Trace Back. In both techniques, a shift register is associated with every trellis node throughout the decoding operation . Since one of the major interests is the low power design, the proposed decoder has been implemented using the trace back approach which dissipates less power. The major disadvantage of the RE approach is that its routing cost is very high especially in the case of long-constraint lengths and it requires much more resources.

4. MODIFIED ARCHITECTURE FOR ADAPTIVE VITERBI DECODER

The aim of the adaptive Viterbi Decoder is to reduce the average computation and path storage required by the Viterbi algorithm. Instead of computing and retaining all $2K-1$ possible paths, only those paths which satisfy certain cost conditions are retained for each received symbol at each state node. Path retention is based on the following criteria.

A threshold T indicates that a path is retained if its path cost is less than dm + T, where dm is the minimum cost among all surviving paths in the previous trellis stage.

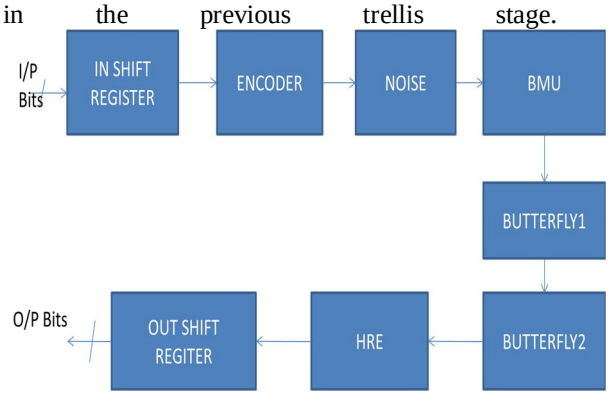

Fig 4.1 Block diagram of adaptive viterbi decoder.

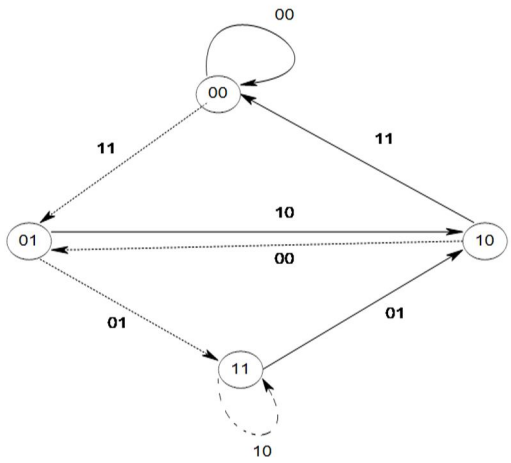

Fig 5.2 State diagram

5. CONVOLUTIONAL CODES

The convolutional encoder is basically a finite state machine. The k bit input is fed to the constraint length K shift register and the n outputs are calculated from the generator polynomials by the modulo-2 addition. The generator polynomial specifies the connections of the encoder to the modulo-2 adder.

The Fig 5.1 below illustrates a simple convolutional coder with

$$V_1 = m_0 \oplus m_1 \oplus m_2 \ldots\ldots\ldots(1)$$

$$V_2 = m_0 \oplus m_2 \ldots\ldots\ldots\ldots(2)$$

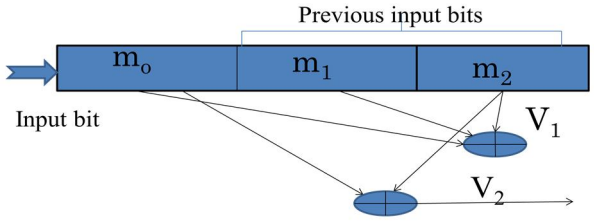

Fig 5.1 Convolutional encoder.

Convolutional encoder can be described in terms of state table, state diagram and trellis diagram. The State is defined as the contents of the shift register of the encoder. In state table output symbol can be described as a function of input symbol and the state. State diagram shows the transition between different states.

Table 5.1 State table

Input Bit (mo)	Present state (S1S0)	Next state(S1 S0)	Output bits(V1V0)
0	00	00	00
1	00	01	11
0	01	10	11
1	01	11	00
0	10	00	10
1	10	01	01
0	11	10	01
1	11	11	10

Trellis diagram is the description of state diagram of the encoder by a time line i.e. to represent each time unit with a separate state diagram

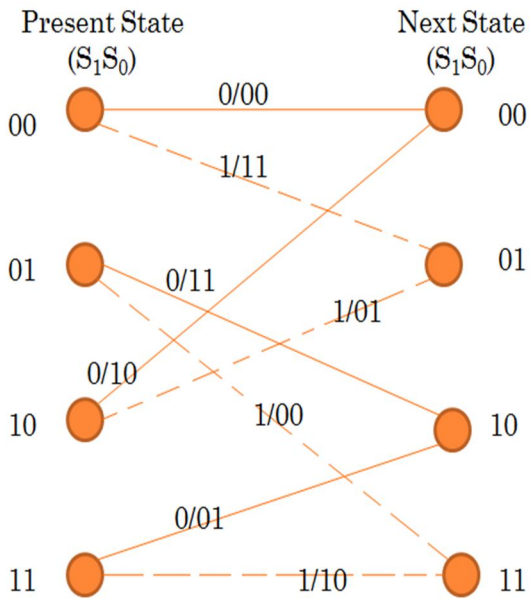

Fig 5.3 Trellis diagram

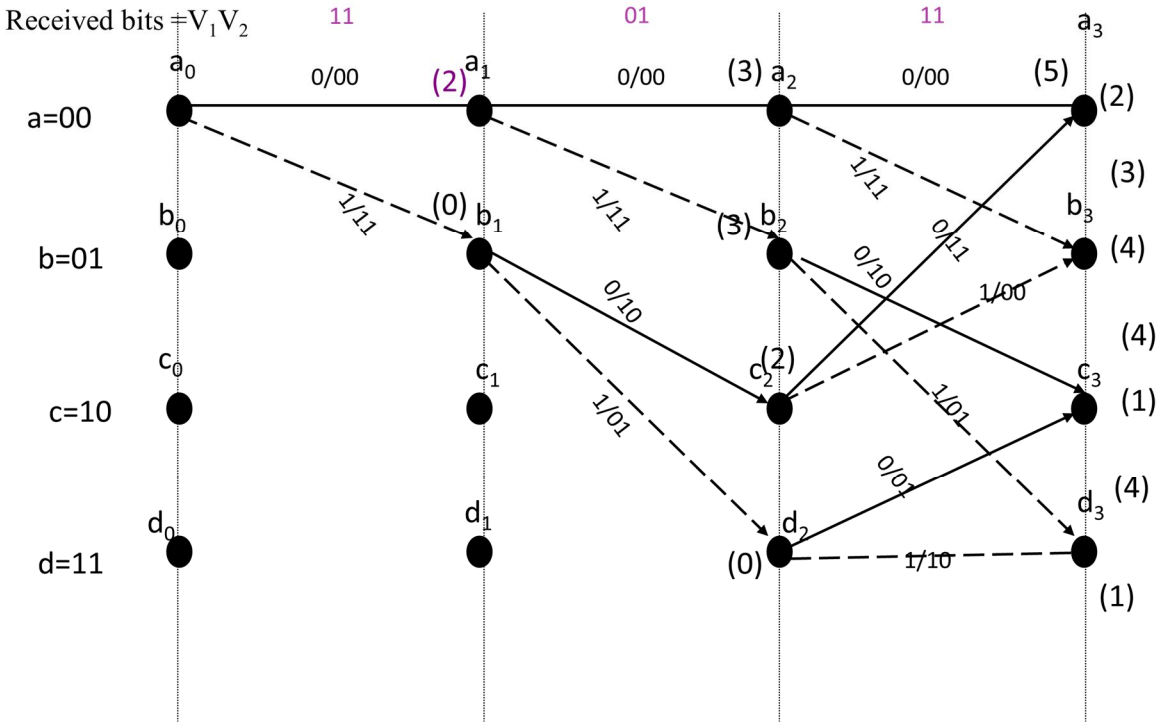

Fig 5.4 Viterbi algorithm

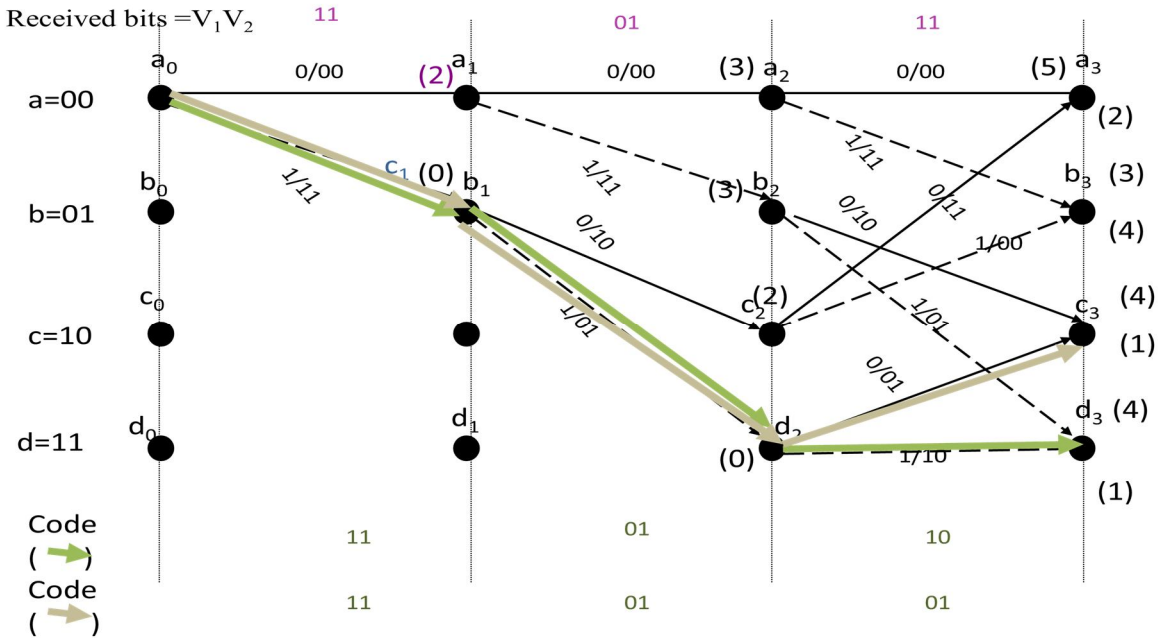

Fig 5.5 Viterbi Algorithm for Trace Back Path

6. ADVANTAGES AND APPLICATIONS

6.1 Advantages

- The use of error-correcting codes has proven to be an effective way to overcome data corruption in digital communication channels.
- It is used for increasing the speed, reducing the power and cost. .

6.2 Applications

- A Low-Power Viterbi Decoder for Wireless Communications Applications.
- Pipelined VLSI Architecture of The Viterbi Decoder for IMT-2000.
- 200Mbps Viterbi decoder for UWB.
- Viterbi Decoder for WCDMA System.
- Low complexity efficient trackback viterbi decoder for wireless applications.
- A Soft IP Generator for High-speed Viterbi Decoders.

7. CONCLUSION

• The processing execution time has been reduced by removing the trace back algorithms that is used to find the correct paths.
• The survivor path algorithm used, the address of the memory unit to select the correct path which specify the output code.
• Reconfigure the Viterbi decoder, and adaptive Viterbi decoder units will give simple elements in each unit and new algorithms.
• It was found that the survivor path decoder is capable of supporting frequency up to 790 MHz for constraint lengths 7, and 9 , rate 1/3 and long survivor path is 4. The different constraint length didn't affect of the complexity of the decoder and the processing time of computing the correct path.
•As mobile and wireless communication becomes increasingly ubiquitous, the need for dynamic reconfigure ability of hardware shall pose fundamental challenges for communication algorithm designers as well as hardware architectures.
•This paper attempts to solve this problem for the particular case of the Viterbi decoder, which is a critical component at a physical layer of most wireless communication systems.
•A new Viterbi decoder architectures have been proposed. These results were evaluated and assessed. Next the adopted design were coded in VHDL and implemented on a SPARTAN 3.

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