

Simulation of Integer N Frequency Synthesizer

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Abstract:-This document implements oscillator in the up conversion and down conversion of wireless transceivers using Integer N Frequency synthesizer with an external loop filter and VCO. The Easiest way to design and simulate Frequency synthesizer and lock the PLL. It can implement practically at high frequencies.

Keywords : ADF4106, ADSIMPLL, Pulse Swallow Function.

I.INTRODUCTION

To implement Local oscillators in the up conversion and down conversion blocks of wireless receivers and transmitters by ADF4106 frequency synthesizer. Its features includes 6.0 GHz bandwidth with 2.7V to 3.3V power supply having a separate charge pump supply having a feature of programmable dual-modulus prescaler 8/9, 16/17, 32/33, 64/65. It is with a programmable charge pump currents with analog and digital lock detect. It is also with hardware and software power down mode.

Applications include Broadband wireless access, satellite systems, Instrumentation, wireless LANS, Base Stations for wireless radios.

A. phase-locked loop or phase lock loop(PLL):

PLL is a control system that generates an output signal whose phase is related to the phase of an input "reference" signal. It is an electronic circuit consisting of a variable frequency oscillator and a phase detector. This circuit compares the phase of the input signal with the phase of the signal derived from its output oscillator and adjusts the frequency of its oscillator to keep the phases matched. The signal from the phase detector is used to control the oscillator in a feedback loop.

PLL has the following components

1. Phase Detector: A non-linear device whose output contains the phase difference between the reference signal and the VCO signal.
2. Voltage Controlled Oscillator (VCO): Another non-linear device which produces an oscillation whose frequency is controlled by a voltage.
3. Loop filter: Most PLLs depend on some sort of low pass filtering in order to function properly.
4. Feedback interconnection: A part of the VCO signal is fed back as an input to phase detector. Phase error, which is the output of phase detector, is used as control voltage for the VCO.

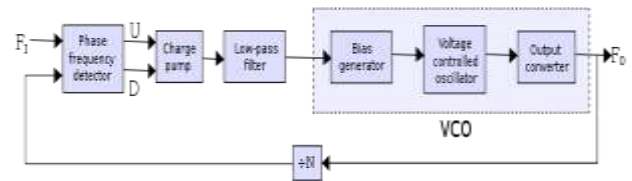


Fig.1.Digital Phase Locked Loop

II.FUNCTIONAL BLOCK DIAGRAM OF ADF4106

It is equipped with low noise, digital phase frequency detector (PFD), a précised charge pump, a programmable input reference divider, A and B counter which can be programmed, and dual modulus prescaler with $P/P + 1$. The A is a 6-bit counter and B is a 13-bit counter, by combining A And B with Prescaler P we get an N counter looking for with an equation $N=BP+A$. Additionally 14 bit counter gives the reference input for phase frequency detector circuit. By combining ADF4106 with an external loop filter and Voltage Control Register, we can implement a complete Phase locked loop. The bandwidth can be changed by changing the loop filter bandwidth. High bandwidth indicates frequency doublers can be eliminated in many high frequency systems in order to simplify system architecture and for cost reducing.

A. RF Input Stage

CML clock levels are generated by 2 stage limiting amplifier which needed prescaler.

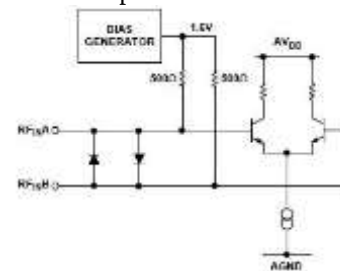


Fig.2.RF input stage of adf4106

B. Pulse Swallow Function

VCO frequency equation, output frequency generated by A, B and R counter values along with prescaler input i.e.,

$$f_{vco} = [(P \times B) \times (f_{\text{reference input}} / R)]$$

Where f_{vco} is the output voltage control oscillator frequency, P is preset counter, B is 13 bit counter, A is 6 bit counter, $f_{reference\ input}$ is external oscillator reference frequency.

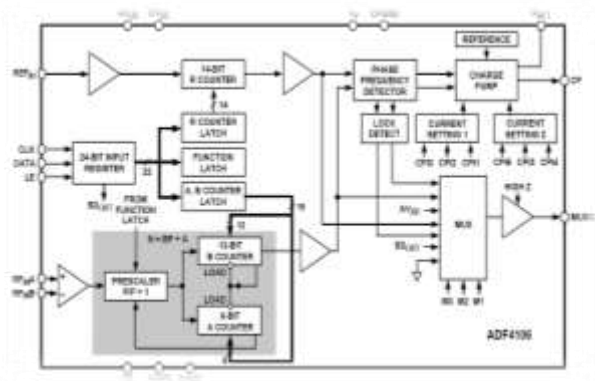


Fig.3.BLOCK DIAGRAM OF ADF4106

C. R Counter

R Counter divides from 1 to 16383 as it has 14 bit counter. It produces clock to phase frequency detector.by dividing the count with the reference frequency.



Fig.4.R Counter Latch

D. A and B Counter

A and B CMOS Counter combin with prescaler to get a wide range division ratio in PLL feedback counter. The counter works when prescaler output to be as 325 MHz.

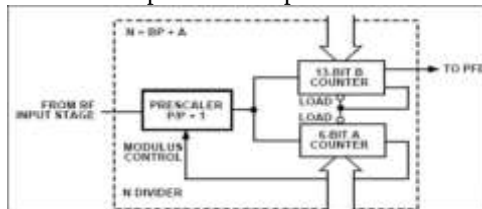


Fig.5.A and B Counters



Fig.6. N Latch

E. Phase Frequency Detector

The input from R and N are taken producing output which is proportional to the difference between phase and frequency. It includes delay element that controls the pulse width of anti backlash.

The phase noise and reference spurs get minimized with no dead end in PFD transfer function. ABP2 and ABP1 are the two bits that controls the pulse width.

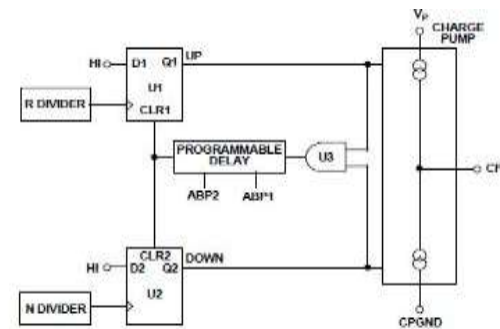


Fig.7.Simplified schematic of PFD in ADF 4106

F. Charge Pump

It is an electronic circuit which uses capacitors as energy storage elements to create either a higher or lower voltage power source. These circuits are capable of higher efficiencies as high as 90 -95%. It can double, invert the voltages and generate arbitrary voltages depending on the controller and circuit topology.

It is a charge pump action which operates on 10 KHz to minimize the amount of capacitance needed. Charge pump capacitor is known as 'Flying Capacitor'.

G. Initialization Latch



Fig.8. Initialization Latch

H. MUX Output

The output multiplexer on the ADF4106 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch.

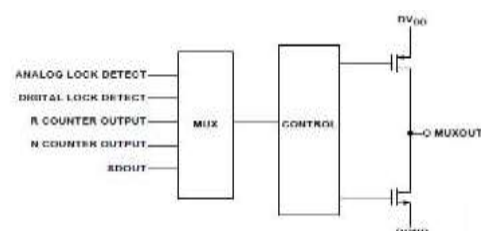


Fig.9.MUXOUT section of ADF4106

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect. Digital lock detect is active high. When LDP in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle. When lock is detected, this output is high with narrow, low-going pulses.

III.DESIGN SIMULATION

A. Required Specifications

Locking frequency	=	5000MHz
Reference frequency	=	10MHz
Step size	=	1MHz
Chip V_{pmax}	=	5.5V

B. Procedure:

1. Calculation of reference divider(N):

$$N = \frac{\text{output frequency}}{\text{channel spacing}} = (BP+A)$$

B = B counter value, A=A counter value

$$\frac{P}{P+1} = \text{Prescaler value.}$$

2. Using Above Equations find the A and B values where B should be greater than A by selecting equivalent P value.

3. Hexa decimal equivalent values of N,A,B should be calculated.

4. Obtained values should be loaded in to the registers to lock the given frequency. When c2 and c1 bits are 00 then it selects R counter, if 01 then it selects N counter, if 10 then it selects functional latch and if it is 11 then it selects initialization latch.

IV.SOFTWARE IMPLEMENTATION

A. By using ADSIMPLL Software tool ADF4106 is locked for the given specifications.

For Designing and analyzing PLL Frequency synthesizers ADSIMPLL provides an integrated environment using the analog devices ADF series of PLL chips. It is a user friendly graphical interface with complete design package.

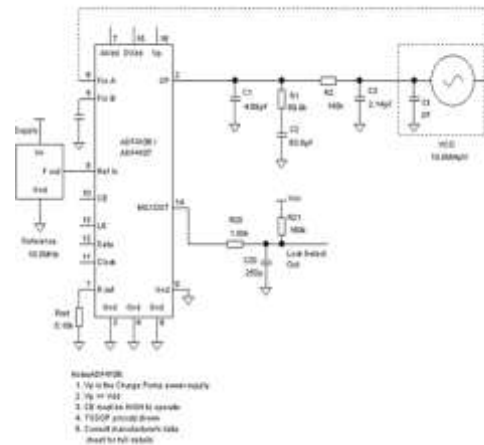


Fig.10.Schematic

Flow Chart For Configuring Registers:

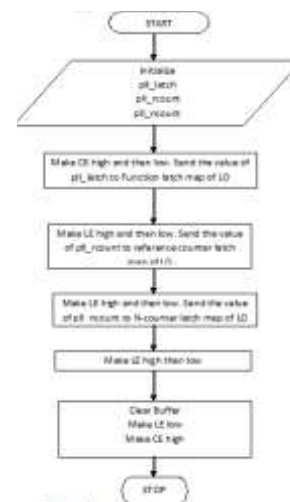


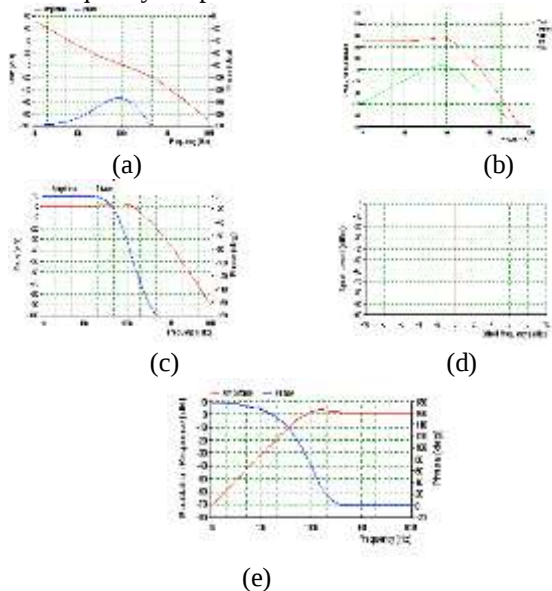
Fig.11.Flowchart for configuring Registers

B. Working with ADSIMPLL:

1. PLL synthesizer chip used in the design is specified
2. Type of PLL whether it is Integer N or Fractional N should be selected.
3. Minimum and maximum frequency range and channel spacing should be specified.
4. The prescaler value should be specify.
5. Lock detect type should be selected.
6. Desired loop filter should be selected.
7. By specifying k value choose VCO from library file.
8. Select custom reference or choose reference oscillator from the library file.
9. Run simulation and observe frequency and time domain results for the given specifications.

V.SIMULATION RESULTS

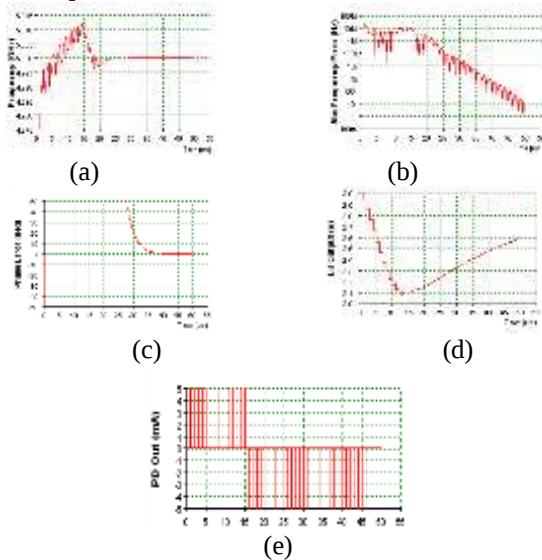
A. Frequency Response



(a)Open loop gain at 5GHz (b)Closed loop Gain at 5GHz
(c)Phase noise at 5GHz (d) Leakage Spurs at 5GHz (e) FM Response at 5GHz

Fig.12.Frequency Response

B. Time Response



(a)Frequency (b) Output Phase Error (c) Frequency error (d) Lock detect output (e) Phase detect output

Fig.13.Time Response

VI.CONCLUSIONS

Thus given ADF4106 integer-N frequency synthesizer is designed with external loop filter and VCO and locked for the required specifications with the verification of time and frequency simulation results. It is easier procedure to lock

PLL by Designing PLL with ADF4106 with an wxternal loop filter and VCO.

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