

Design and Analysis of CMOS and Adiabatic 4-Bit Binary Multiplier

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ABSTRACT

The power dissipation becoming a limiting factor in VLSI circuits and systems. Due to relatively high compatibility of VLSI systems used in various applications, the power dissipation in CMOS circuits arises from its switching activity, which is influenced by the supply voltage and effective capacitance. The power dissipation can be reduced by adopting different design style. Adiabatic logic style is said to be an attractive solution for such low power electronic applications. The proposed technique has less power dissipation when compared to the conventional CMOS design style. This paper evaluates the 4-bit binary multiplier in different adiabatic logic style and their results were compared with conventional CMOS design. The simulation results indicate that the proposed technique is advantageous in many of low power digital applications.

Keywords— Adiabatic logic, charge recovery, Low power, multiplier, Power supply

INTRODUCTION

The main objective of this thesis is to provide new low power solutions for Very Large Scale Integration (VLSI) designers. Especially, this work focuses on the reduction of the power dissipation, which is showing an ever-increasing growth with the scaling down of the technologies. Various techniques at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architectural and system level. Furthermore, the number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, so the power dissipation rises and heat removal becomes more difficult and expensive. Then, to limit the power dissipation, alternative solutions at each level of abstraction are proposed. The dynamic power requirement of CMOS circuits is rapidly becoming a major concern in the design of personal information systems and large computers. In this thesis work, a new CMOS logic family called *ADIABATIC LOGIC*, based on the adiabatic switching principle is presented.

The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure dramatically reduces the power dissipation.

The Adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy.

In this paper we present different multiplier designs based on adiabatic and conventional CMOS logic principle and their performance

based on the power dissipation compared.

The rest of the paper is organized as follows. Section 2 gives details of conventional charging and adiabatic charging principle, Section 3 explain different 4 bit multiplier implementations, Section 4 simulation results and finally Section 5 is conclusion.

ADIABATIC PRINCIPLE

The operation of adiabatic logic gate is divided into two distinct stages: one stage is used for logic evaluation; the other stage is used to reset gate output logic value. Both the stages utilize adiabatic switching principle. In the following section conventional switching and adiabatic switching analyzed in detail.

Conventional charging

There are three major sources of power dissipation in digital CMOS circuits those are dynamic, short circuit and leakage power dissipation. The dominant component is dynamic power dissipation and is due to charging, discharging of load capacitance. The equivalent circuits of CMOS logic for charging and discharging is shown in Fig.1. The expression for total power dissipation is given by.

$$P_{tot} = \alpha \cdot C_L \cdot V \cdot V_{DD} \cdot f_{clk} + I_{SC} \cdot V_{DD} + I_{le} \cdot V_{DD} \quad (1)$$

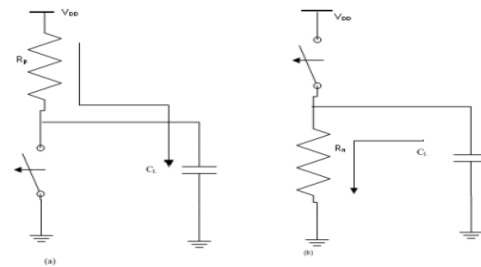


Fig.1 Conventional CMOS a) Charging b) Discharging

Eq.(1), the first term represents the dynamic power, where CL is the loading capacitance, f_{clk} is the clock frequency, and α is the switching activity. In most cases, the voltage swing V is the same as the supply voltage V_{DD} , however, in some logic circuits, the voltage swing on some internal nodes may be slightly less. The second term is due to the direct-path short circuit current I_{SC} which arises when both the NMOS and PMOS transistors are

simultaneously active, conducting current directly from supply to ground. Finally, leakage current I_{le} which can arise from substrate injection and sub threshold effects is primarily determined by fabrication technology considerations.

Adiabatic Switching

Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time varying voltage source or constant current source, as shown in Fig. 2. Here, R represents the on-resistance of the pMOS network. Also note that a constant charging current corresponds to a linear voltage ramp. Assuming that the capacitance voltage V_C is zero initially, the variation of the voltage as a function of time can be found as

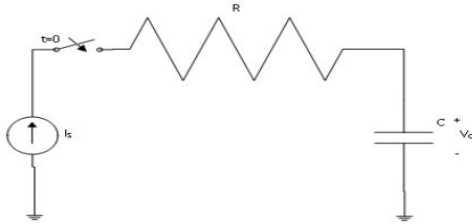


Fig. 2 Schematic for adiabatic charging process

$$V_C(t) = I_S \cdot t / C \tag{2}$$

Hence the charging current can be expressed as a function of V_C and time t

$$I_S = C \cdot V_C(t) / t \tag{3}$$

The amount of energy dissipated in the resistor R from $t = 0$ to $t = T$ can be found as

$$E_{diss} = R \int I_S^2 dt = R I_S^2 T \tag{4}$$

Combining (3) and (4), the dissipated energy during this charge-up transition can also be expressed as

$$E_{diss} = RC / T \cdot CV_C^2(T) \tag{5}$$

From (5) we can say that the use of inductors should be limited from integrated circuit point because of so many factors like chip integration, accuracy, efficiency etc. An alternative to using pure voltage ramps is to use stepwise supply voltage waveforms, where the output voltage of the power supply is increased and decreased in small increments during charging and discharging. Since the energy dissipation depends on the average voltage drop across the resistor by using smaller voltage steps the dissipation can be reduced considerably. The total dissipation using step wise charging is given by (6)

$$E_{diss} = 1/n CV_{DD}^2 / 2 \tag{6}$$

Where n is number of steps used to charge up capacitance to V_{DD} .

In literature, adiabatic logic circuits classified into two types: full adiabatic and quasi or partial adiabatic circuits. Full-adiabatic circuits have no non-adiabatic loss, but they are much more complex than quasi-adiabatic circuits. Quasi-adiabatic circuits have simple architecture and power clock system. There are two types of energy loss in quasi-adiabatic circuits, adiabatic loss and non adiabatic loss. The adiabatic loss occurs when current flows through non-ideal switch, which is proportional to the frequency of the power-clock. If any voltage difference between the two

terminals of a switch exists when it is turned on, non-adiabatic loss occurs. The non-adiabatic loss, which is independent of the frequency of the power-clock, is proportional to the node capacitance and the square of the voltage difference. Several quasi-adiabatic logic architectures have been reported, such as IECL, PFAL, STACK etc.

A) ECERL-Efficient Charge Recovery Logic:

Efficient Charge – Recovery Logic (ECRL) uses cross-coupled PMOS transistors. It has the structure similar to Cascode Voltage Switch Logic (CVSL) with differential signaling. It consists of two cross-coupled transistors $M1$ and $M2$ and two pull down network with complement structure. An non standard AC power supply is used for ECRL gates, so as to recover and reuse the supplied energy. Both out and $/out$ are generated so that the power clock generator can always drive a constant load capacitance independent of the input signal. A more detailed description of ECRL can be found in. Full output swing is obtained because of the cross-coupled PMOS transistors in both pre charge and recover phases. But due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss both in the pre charge and recover phases. That is, to say, ECRL always pumps charge on the output with a full swing. However, as the voltage on the supply clock approaches to

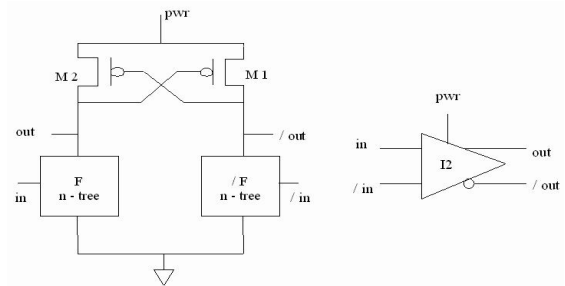


Fig.3. The Basic Structure of the Adiabatic ECRL Logic

So the recovery path to the supply clock to the supply clock is disconnected, thus, resulting in incomplete recovery. V_{tp} is the threshold voltage of PMOS transistor. The amount of loss is given as

$$E_{ECRL} = C |V_{tp}|^2 / 2 \tag{7}$$

Thus, from Equation (4.2), it can be inferred that the non-adiabatic energy loss is dependent on the load capacitance and independent of the frequency of operation.

B) Positive Feedback Adiabatic Logic:

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) [15] has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery. The general schematic of the PFAL gate is shown in Figure 4.3.

The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS $M1-M2$ and two NMOS $M3-M4$, that avoids a logic level degradation on the output nodes out and $/out$. The two n-trees realize the logic functions. This logic family also

generates both positive and negative outputs. The functional blocks are in parallel with the PMOSFETs of the adiabatic amplifier and form a transmission gate. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs.

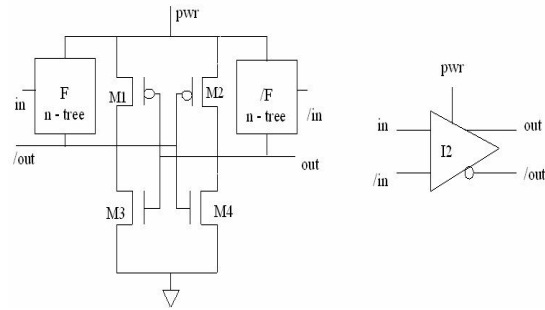


Fig. 4. The Basic Structure of the Adiabatic PFAL Logic

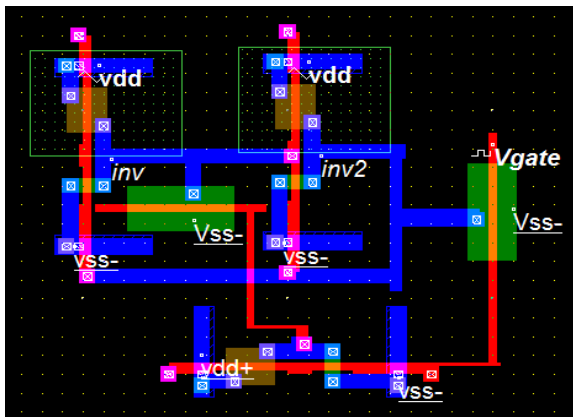


Fig.5. Inverter logic design using ECRL

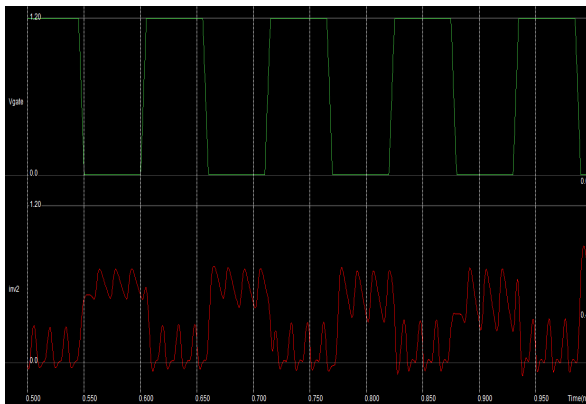


Fig.6 Inverter logic design using ECRL

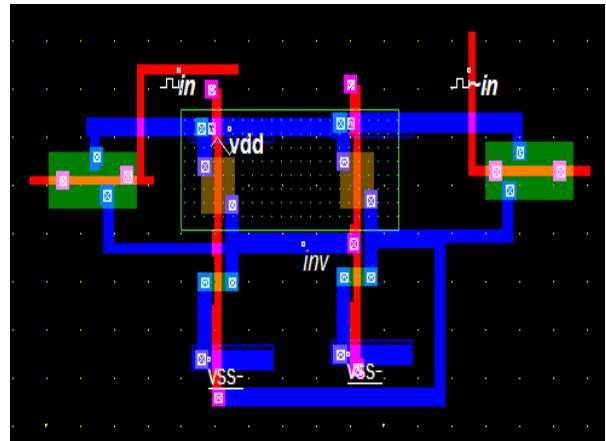


Fig.7 Inverter logic design using PFAL

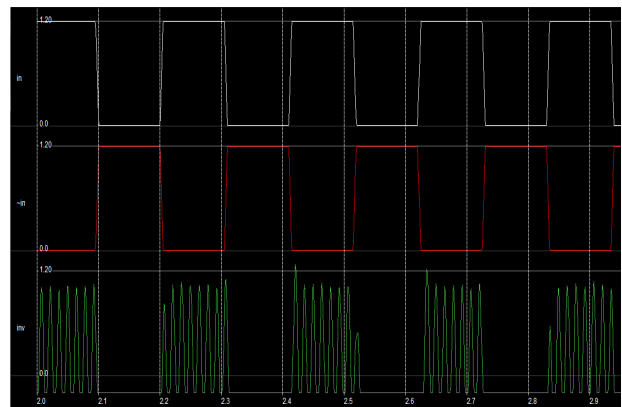


Fig.8 Simulation of inverter logic design using PFAL

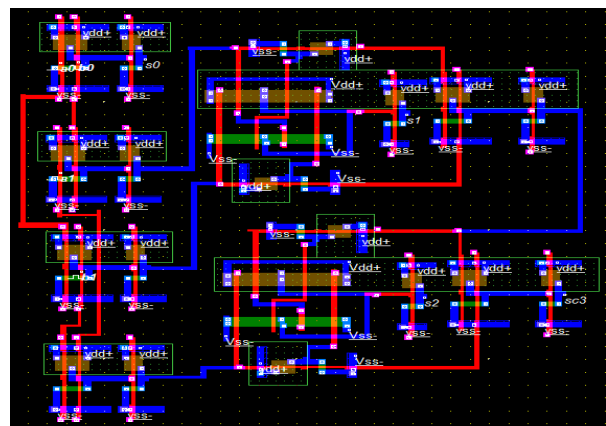


Fig.9 Layout design for multiplier logic using ECRL

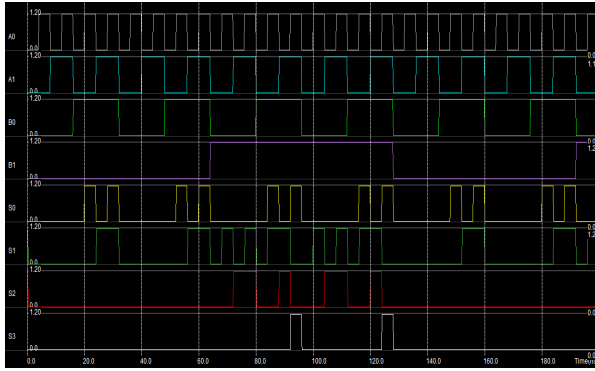


Fig.10 Simulation output for multiplier logic for ECRL

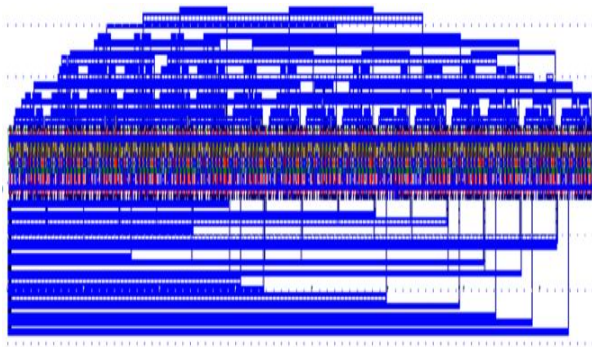


Fig.11 Layout design for multiplier logic using PFAL

Table 1: Parametric analysis of Multipliers

Parameters	Conventional multiplier	IECRL multiplier	PFAL multiplier	stack multiplier
Number of MOSFET	324 NMOS 324 PMOS	228 NMOS 228 PMOS	287 NMOS 287 PMOS	480 NMOS 480 PMOS
Switching delay	In the range of ns	In the range of ps	In the range of ns	In the range of ns
Freq at Vdd	1.125GHz	68GHz	45 GHz	--
Power dissipation	34.68uW	67uW	25.35uW	92.95uW
Max drain current	1.793mA	5.0mA	2.160mA	6.10mA

CONCLUSION

The observation table shows the reduce power dissipation in the range of uW and required more number of transistor. For 4 bit multiplication the total number of full adder (FA) block require are $4 \times 3 = 12$ and the total AND logic gate i.e partial product (PP)

requires are 16. Power reduction is achieved by recovering the energy in the recover phase of the supply in range of uW with increase in switching delays. Adiabatic logic achieves low power by maintaining small potential differences across the transistors while they are conducting, and allowing the charge stored in the output load capacitors to be recycled. The circuit becomes low power faster but hardware complexity is also high.

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