

# Reduction of Ground Bounce Noise in 14T Full Adder by Using Various Power Gating Techniques

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**Abstract:** The main objective is to compare the existing full adders circuits and their performances to design a Low Power Full Adder having improved result as compared to existing Full Adders. The Full Adder circuit is a very important part in application like Digital Signal process (DSP) design, chip, and microcontroller and processing units. This paper discusses the evolution of full adder circuits in terms of lesser power consumption higher speed. As low power circuits are most popular now a days as the scaling increase the leakage powers in the circuit also increases rapidly so for removing these kind of leakages and to provide a better power efficiency we are using many types of power gating techniques. In this paper we are going to analyse the static power dissipation on 14T Full Adder using different types of power gated circuits using low power VLSI design techniques and we are going to display the comparison results in TSMC018 Nanometre Technology. The simulations were done using Tanner Tools and the results were given below.

**Keywords:** Power Gating, Static Power, Tanner Tool

## I. INTRODUCTION

Today's there are a growing number of portable applications requiring small-area low-power high-throughput circuitry. Therefore, circuits with low power utilization grow to be the most important candidates for design of microprocessors and system mechanism ADDITION is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as application-specific DSP architectures and microprocessors. In addition to its main task, which is adding binary numbers, it is the nucleus of many other useful operations such as subtraction, Multiplication, division, addresses calculation, etc. In most of these systems the adder is part of the critical path that. The choice of logic style to design digital circuits strongly influences the circuit performance. The delay time depends on the size of transistors, the number of transistors per stack, the parasitic capacitance including intrinsic capacitance and capacitance due to intracellular and intercellular routing, and the logic depth (i.e., number of logic gates in the critical path). The dynamic power consumption depends on the switching activity and the number and size of transistors. Among other things, the die area depends on the number and size of transistors and routing complexity. Power gating affects style

design quite clock gating. It will increase time delays as power gated modes need to be safely entered and exited.

### A. Power Gating

Subject trade-offs exist between planning for the number of escape power saving in low power modes and therefore the energy dissipation to enter and exit the low power modes. Closing down the blocks will be accomplished either by computer code or hardware. Driver circuit will schedule the facility down operations. Hardware timers will be utilized [1]. An infatuated power management controller is an alternative choice.

An outwardly switched power offer could be a terribly basic type of power gating to attain long run escape power reduction. To shut off the block for tiny intervals of your time, internal power gating is additional appropriate. CMOS switches [2] that give power to the electronic equipment square measure controlled by power gating controllers. Outputs of the facility gated block discharge slowly hence output voltage levels pay longer in threshold voltage level this will cause larger short current.

Power gating uses low-leakage PMOS transistors as header switches to shut off power provides to elements of a style in standby or sleep mode [4]. NMOS footer switches may be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the facility offer and a virtual power network that drives the cells and may be turned off.

The quality of this complicated power network is vital to the success of a power-gating style. 2 of the foremost vital parameters square measure the IR-drop and therefore the penalties in semiconducting material space and routing resources. Power gating will be enforced victimization cell- or cluster-based (or fine grain) approaches or a distributed coarse-grain approach.

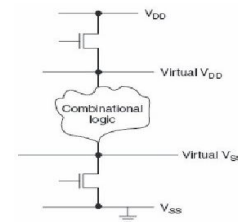


Fig1: Power Gated Circuits

## II. POWER-GATING PARAMETERS

Power gating implementation has extra issues for temporal order closure implementation. The subsequent parameters ought to be thought of and their values rigorously chosen for a booming implementation of this system.

- Power gate size: The ability gate size should be selected to handle the number of switch current at any given time. The gate should be larger such there's no measurable voltage (IR) drop attributable to the gate. As a rule of thumb, the gate size is chosen to be around three times the switch capacitance. Designers also can choose from header (P-MOS) or footer (N-MOS) gate. Sometimes footer gates tend to be smaller in space for an equivalent switch current. Dynamic power analysis tools will accurately live the switch current and additionally predict the dimensions for the ability gate.
- Gate management slew rate: In power gating, this can be a very important parameter that determines the ability gating potency once the slew rate is massive, it takes longer to modify off and switch-on the circuit and thus will have an effect on the ability gating potency. Slew rate is management led through buffering the gate control signal.
- Coinciding switch capacitance: This necessary constraint refers to the number of circuit that may be switched at the same time while not poignant the ability network integrity. If an oversized quantity of the circuit is switched at the same time, the ensuing "rush current" will compromise the ability network integrity. The circuit must be switched piecemeal so as to stop this.
- Power gate leakage: Since power gates are manufactured from active transistors, leak reduction is a very important thought to maximize power savings.

### A. Fine-grain power gating

Adding a sleep semiconductor unit to each cell that's to be turned off imposes an oversized space penalty, and severally gating the ability of each cluster of cells creates temporal order problems introduced by inter-cluster voltage variation that are troublesome to resolve. Fine-grain power gating encapsulates the switch semiconductor unit as a locality of the quality cell logic. Switch transistors are designed by either the library informatics seller or primary cell designer sometimes these cell styles adapt to the traditional primary cell rules and might simply be handled by EDA tools for implementation.

The size of the gate management is meant considering the worst case state of affairs which will need the circuit to modify throughout each clock cycle, leading to an enormous space impact. A number of the recent styles implement the fine-grain power gating by selection, however just for the low American state cells. If the technology permits multiple American state libraries, the employment of low American state devices is min within the style (20%), in order that the world impact will be reduced. Once exploitation

power gates on the low American state cells the output should be isolated if following stage may be a high American state cell. Otherwise it will cause the neighbouring high American state cell to leak once output goes to associate degree unknown state attributable to power gating.

Gate management slew rate constraint is achieved by having a buffer distribution tree for the management signals. The buffers should be chosen from a collection of invariably on buffers (buffers while not the gate management signal) designed with high American state cells. The inherent distinction between once a cells switches off with relation to another, minimizes the push current throughout switch-on and switch-off.

Usually the gating semiconductor unit is meant as a high American state device. Coarse-grain power gating offers any flexibility by optimizing the ability gating cells wherever there's low switch activity. Leak improvement must be done at the coarse grain level, swapping the low leak cell for the high leak one. Fine-grain power gating is a chic methodology leading to up to ten times leak reduction. This kind of power reduction makes it associate degree appealing technique if the ability reduction demand isn't glad by multiple American state improvements alone.

### B. Coarse-grain power gating

The coarse-grained approach implements the grid vogue sleep transistor that drives cells regionally through shared virtual power networks. This approach is a smaller amount sensitive to PVT variation, introduces less IR-drop variation, and imposes a smaller space overhead than the cell- or cluster-based implementations. There are 2 ways that of implementing a coarse-grain structure:

- Ring-based: The ability gates are placed round the perimeter of the module that's being switched-off as a hoop. Special corner cells are accustomed flip the ability signals round the corners.
- Column-based: The ability gates are inserted within the module with the cells abutted to every alternative within the sort of columns the world power is that the higher layers of metal, whereas the switched power is within the lower layers.

Gate size depends on the general switch current of the module at any given time. Since solely a fraction of circuits switch at any purpose of your time, power gate sizes are smaller as compared to the fine-grain switches. Dynamic power simulation exploitation worst case vectors will confirm the worst case switch for the module and thus the dimensions. The IR drop also can be factored into the analysis. Coinciding switch capacitance may be a major thought in coarse-grain power gating implementation so as to limit coinciding switch, gate management buffers will be flower in chains, and special counters will be accustomed by selection activate blocks of switches.

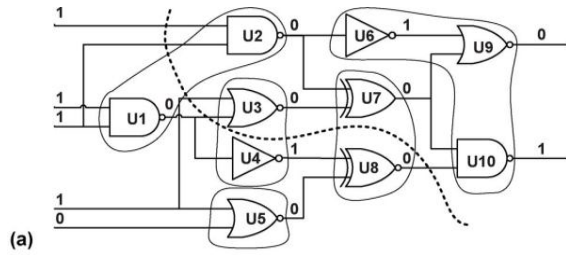


Fig2: Device without Power gating

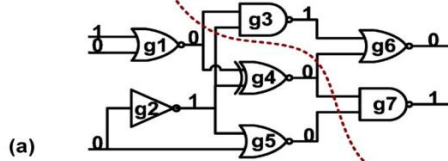


Fig3: Device with Power gating with reduced area & Power using clustering network formation.

### III. POWER GATING METHODS:

#### B. Sleep Transistor Technique

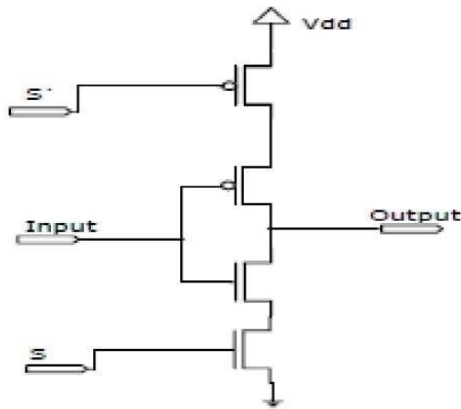


Figure 4: Sleep Transistor Technique

In sleep Transistor Technique cut off transistor (pull-up or pull-down transistors or both) networks from supply voltage or ground using sleep transistors. These types of techniques are also called gating Vdd and gating-GND (note that a gating clock is generally used for dynamic power reduction).It. propose a technique they call Multi-Threshold-Voltage CMOS (MTCMOS) [6], which adds high-Vth sleep transistors between pull-up networks and Vdd and between pull-down networks and ground as shown in Figure 3.2 while logic circuits use low- Vth transistors in order to maintain fast logic switching speeds. The sleep transistors are turned off when the logic circuits are not in use. By isolating the logic networks using sleep transistor, the sleep transistor technique continuously reduces leakage power during sleep mode. However, the additional sleep transistors increase area and delay. Furthermore, the pull-up and pull-down networks will have floating values and thus will lost state during sleep mode. These floating values significantly impact the wakeup time and energy of the sleep technique due to the requirement to recharge transistors which lost state during sleep.

#### C. Stack Approach

In stack approach every sleep electronic transistor, placed in parallel to the one amongst the stacked transistor, reduces resistance of the trail therefore delay is bated throughout active mode. However, space penalty could be an important matter for this approach since each electronic transistor is replaced by 3 transistors.

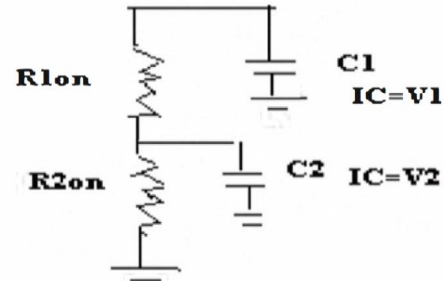


Fig5: Stacking Structure

#### D. Dual Sleep approach

Sleep transistors are crucial half in any low methodology [12] shown in figure6, 2 sleep transistors in every NMOS or PMOS block are used. One sleep electronic transistor is employed to show on in ON state and also the alternative one is employed to show in OFF state. Once more in OFF state a block containing each PMOS and NMOS transistors are utilized in order to scale back the outflow power.

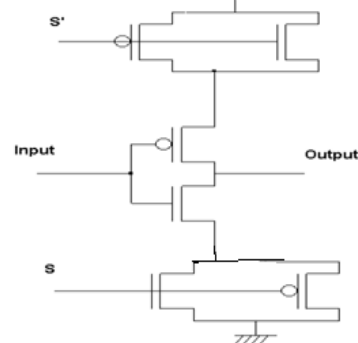


Fig 6: Dual Sleep Approach

Dual sleep approach uses the advantage [11] of using the two extra pull-up transistors and two extra pull-down transistors in sleep time either in OFF state or in ON state. It uses two pull-up sleep transistors and two pull-down sleep transistors. When S=1 the pull down n-channel transistor is ON and the pull-up p-channel transistor is ON since S'=0. So the arrangement works as a normal device in ON state. During OFF state S is forced to 0 and hence the pull down n-channel transistor is OFF and p-channel transistor is ON and the pull-up p-channel transistor is OFF while n-channel transistor is ON. So in OFF state a p-channel is in series with an n-channel both in pull-up and pull-down circuits which is liable to reduce power V.

**E. Dual Stack Approach**

In dual stack approach each sleep and stack junction transistor area unit used for reduction of leakages. during this structure stack junction transistors area unit invariably within the on state throughout stack mode they act like high threshold for reducing run also it preserve the state and within the static mode and also in active with sleep transistor can give total power offer to the circuit.

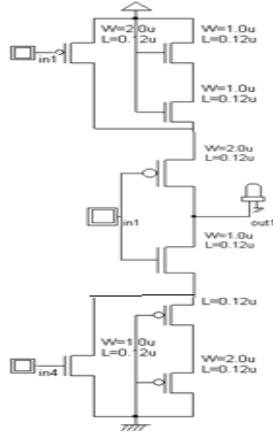


Fig7: Dual Stack Approach

**IV. Simulation**

Power Gating techniques are applied on the 14T full adder and was simulated using TSMC018 Technology

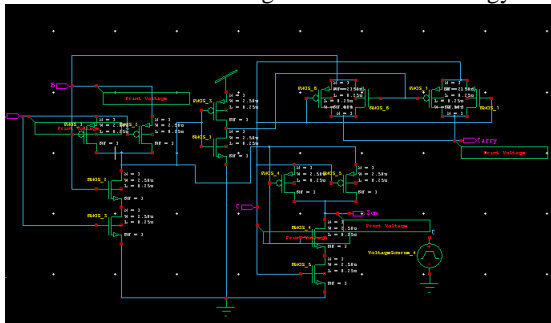


Fig8: 14T full adder Design

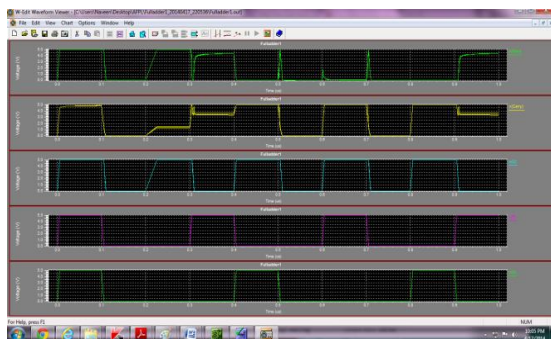


Fig9: 14T full adder Simulation

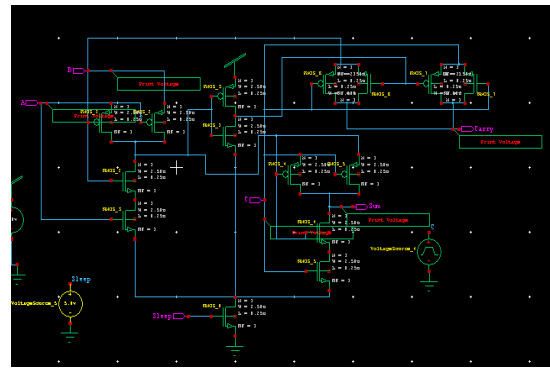


Fig10 : Full Adder with Sleep

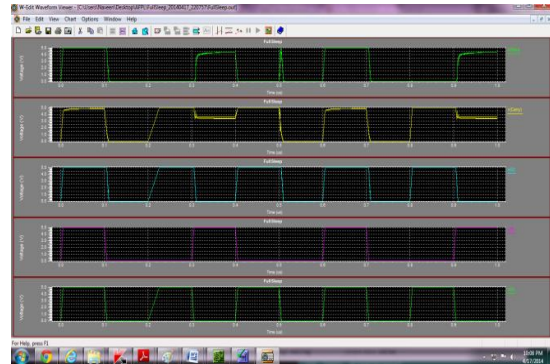


Fig11: Full Adder with Sleep Simulation

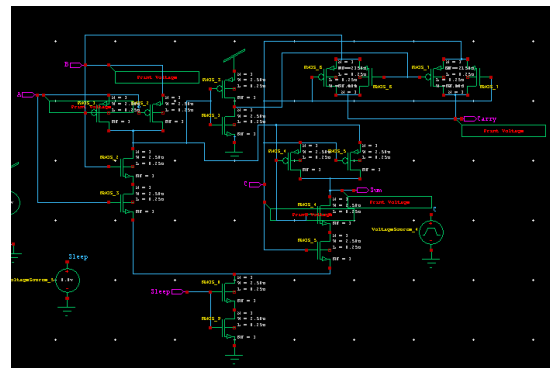


Fig12: Full adder with stacking scheme

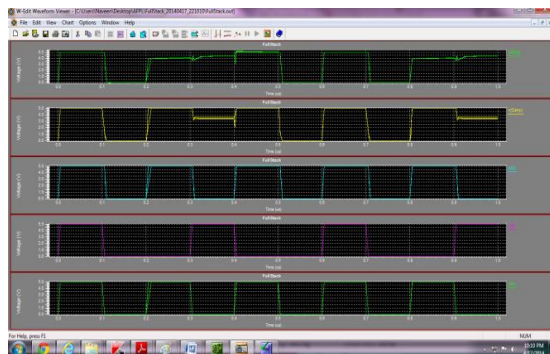


Fig13: Full adder with stacking scheme

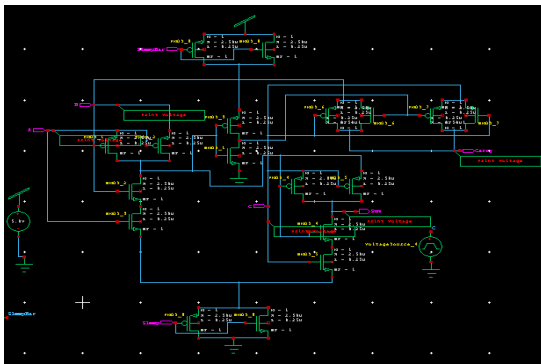


Fig14: Full adder with Dual Sleep

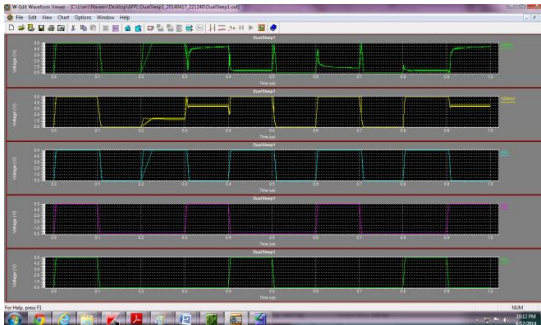


Fig15: Full adder with Dual Sleep Simulation

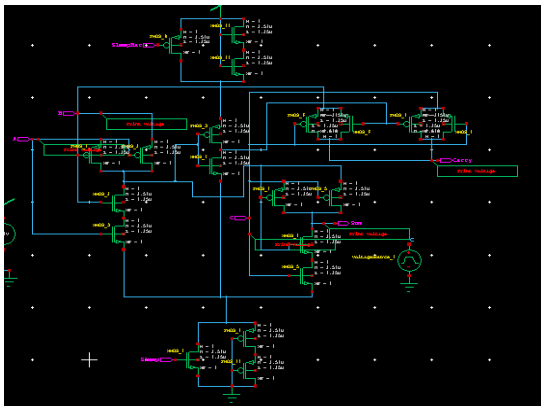


Fig16: Full adder with Dual Stack

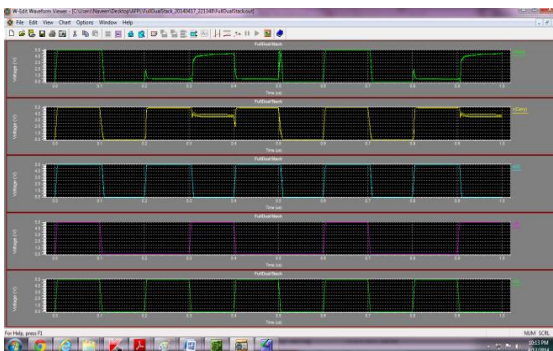


Fig17: Full adder with Dual Stack Simulation

TABULATION

Circuits	Power Dissipation
Full Adder	2.710774e-004 watts
Full Adder Sleep	1.566356e-004 watts
Full Adder Stack	1.462554e-004 watts
Full Adder Dual Sleep	1.182232e-004 watts
Full Adder Dual Stack	1.589669e-005 watts

Fig: 14T Full Adder power consumption with various power gating techniques

V. CONCLUSION

In nanometre scale CMOS technology, sub threshold powers. Unlike the sleep transistor technique, the dual stack technique retains the original state. The dual stack approach shows the least speed power product among all methods. Therefore, the dual stack technique provides new ways to designers who require ultra-low leakage power consumption. Leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques based upon technology and design criteria. In this paper, we provide novel circuit structure named “Dual stack” as a new remedy for designers in terms of static power and dynamic.

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