The Design of SET-CMOS Hybrid Logic Style of 1-Bit Comparator

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Abstract: *Single Electron Transistor is an Ultra-low power consumption as well as Ultra dense circuit formation is now possible with the help of mutual integration. These benefits have drawn the attraction of the future researchers to design the hybrid SET-CMOS style for future Nano-scale low power VLSI design. In this paper, we have designed at room temperature operable One bit Comparator circuit in hybrid SET-CMOS logic with considerably low power consumption. All the simulations are performed in SPICE MIB model for SET operation and BSIM4 for the operation of PMOS. The hybrid structure provides for better performance in respect to the conventional MOSFET structure.*

Keywords: SET, Hybrid CMOS-SET, 1 bit Comparator

Introduction: The electron devices scaling aims at increasing operational speed and reduction in power used. Researchers in single electron devices are mostly accepted to replace the present CMOS technology [1,2]. Single electron devices imply the possibility to control the movement and position of a single electron. Circuits based on the single electron transistor (SET) have the potential advantages of high integration density, ultra-low power dissipation and unique coulomb blockade oscillation characteristics [2,4]. The intrinsic drawbacks preventing the use of SETs in most applications are their low current drivability, small voltage gain, high sensitivity to background charges, and the lack of room temperature operable technology has been overcome based on the recent techniques [5,6]. The replacement of CMOS technology by SET in the near future is improbable. The CMOS has advantage of high speed driving and voltage gain which can compensate for the SET's intrinsic drawbacks. Thus the implementation of hybrid design can be considered as an alternative solution by a combination of SET and CMOS device [7]. The combination of SET-CMOS brings out the novel functionalities which are difficult to achieve in pure CMOS technology [8, 9]. For the hybrid SET CMOS circuit design, at this level a proper choice of design style for high performance logic circuits should be done. It is because all important factors affecting performance are actually influenced by chosen logic style. In this paper a review SET CMOS design style of one bit comparator is given to logic functions.

The structure of SET transistor consists of two tunnel junctions and two gate capacitors as shown in Fig (1). The tunnel junction is characterized by a capacitor Cj and a resistance Rj depending on its physical structure. The two tunnel junctions of SET create a central island that electrons can only enter by tunneling through one of these junctions. This operation is based on Coulomb blockade, which was considered in the study by Gorter [10]. The Single electron transport through a tunnel junction can be achieved by controlling the charge on the island through gate capacitors that are also used to control phase shift of the Coulomb oscillation.

In this paper, hybrid SET-CMOS of one bit comparator are designed and implemented. The MIB compact model for SET device and BSIM 4.6.1 model for CMOS are used. The circuits are verified by means of SPICE simulation software.

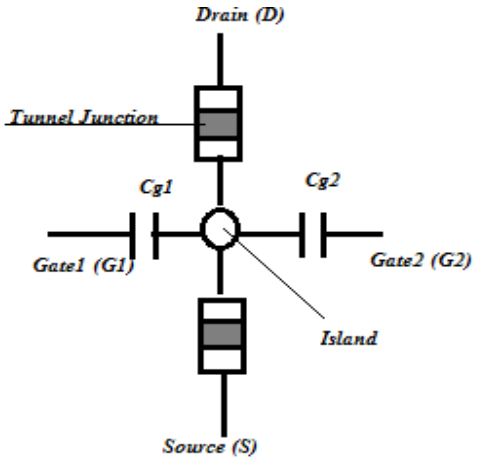

Fig 1 Schematic structure of the SET

The operation of SET, electrons are considered to tunnel through the junction one after from the source to the drain via the island. The tunneling junction can be considered as the PN junction in the MOSFET while the conducting island can be considered as the MOSFET channel. Thus the SET transistor can be used as an electronic switch where it is pushed up into the Coulomb blockade state as an OFF-state or else it can be permitted to conduct current as the ON-state. For SET logical design, the conditions to happen tunneling at room temperature are

- The charging energy E_c must be large as possible compared with the thermal energy K_BT where K_B is the Boltzman constant and T is the operation temperature and
- The tunnel junction resistance R_J must be large as possible compared with the resistance quantum h/e^2 where h is the plank constant and e is the electron charge.

Silicon based SET transistors are more suitable to realize practical proposed circuits due to availability of room temperature operation and the compatibility with modern CMOS fabrication techniques. The simple structure of SET devices offers a higher scaling potential than any existing CMOS to realize dense integrated circuits that can operated with ultra-low power dissipation. SETs have low gain, high output impedance and sensitivity to random background charges. This makes that a complete replacement of CMOS by SET is not in near future to commercially implement electronic circuits based on the existing SET technology. To overcome intrinsic drawbacks of SET technology, hybrid SET-CMOS technology is suggested by scientists as an alternative solution where SET and CMOS are rather complementary. The Single Electron Transistor is an Ultra-low power consumption as well as Ultra dense circuit formation is now possible with the help of mutual integration. The SET-CMOS architectures can also provide new functionalities based on the Coulomb blockade oscillation feature of SETs. Which are very difficult to implement in a pure CMOS technology?

One bit Comparator: Digital or binary comparators are made up from stand AND,NOR and NOT gates that compare the digital signals at their Input terminals and produce an output depending upon the condition of the inputs. For example, whether the input A is greater than, smaller than or equal to the input B at C. Also digital comparators can compare a variable or unknown number for example A(A1, A2, A3, A4, ……,An etc)against that of a constant or known value such as B(B1, B2, B3, B4,…… Bn, etc) and produce an output depending upon the result. Thus the comparator produce the following 3 output conditions A<B, A=B, A>B. This is useful if we want to compare two values and produce an output when the condition is achieved. The fig. 2(a) and fig. 2(b) shows the truth table and logic circuit which explains the operation of a one bit comparator

Input		Output		
A	B	A>B	A=B	A<B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Fig 2a Truth table of 1-bit Comparator

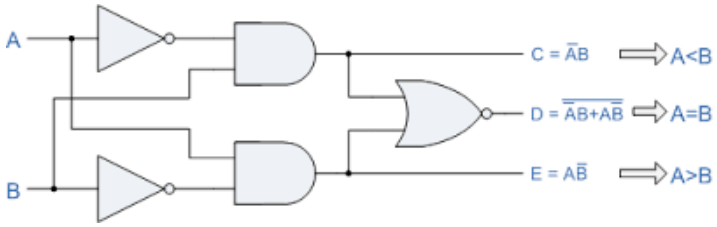

Fig 2b shows the logic diagram of 1 bit Comparator

You may notice two distinct features about the comparator from the truth table. Firstly, the circuit does not distinguish between either two '0' or two '1' as an output A =B is produced when they are both equal, either A = B = '0' or A = B = '1'. Secondly the output condition for A = B resembles that of a commonly available logic gate, the XNOR gate giving Q = A = B. Digital comparators actually use XNOR gates within their design for comparing the respective pairs of bits in each of the two words with single bit comparator cascaded together to produce multi-bit comparator so that larger words can be compared.

Hybrid SET CMOS logic gates: The circuit of a hybrid SET-CMOS Inverter proposed which is formed by a PMOS transistor as the load resistance of an SET. Although it resembles a CMOS inverter, the two differences are the pull

down transistor is a SET and the VDD is defined by the SET device parameters.

Since the MIB model is valid for |VDD| ≤3e / Cε [11] for single / multiple gate (s) and symmetric (or) asymmetric SET devices, the bias Voltage is taken as 800mv. The values of the tunnel junction capacitors are C_{TD} and C_{TS} have be designed to prevent tunneling due to thermal energy. Based on the idea that serial connection is AND and Parallel connection is OR, the circuit of 2 input NAND, 2 input NOR and 2 input XOR are realized using the hybrid CMOS-SET inverter. The circuits of 2 input NAND, 2 input NOR, and inverter are shown in Fig 3(a) , 3(b), 3(c). Using the structure of CMOS counterparts, the Circuit of one bit Comparator is designed and implemented using the hybrid logic gates is shown in fig 3(d). The simulation result is shown in fig.3(e).

Result and discussion:

Many simulators and modeling methods have been made for SET devices and circuits. SIMON, MOSES, SECS are popular SET simulation tools based on Monte Carlo method. SIMON and MOSES are not SPICE compatible. The SPICE macro model can be used to describe the behavior of SET transistors as independent elements with CMOS transistors in are of interconnection capacitance node between SET and CMOS devices is large enough. The proposed circuits are simulated using the MIB compact model. The island, gate and tunnel capacitors of SET designed for room temperature operation and the supply voltage V_{dd} is taken to 08V [11,12].

Design parameters of the SET transistor are C_{TD} = C_{TS} = 0.15aF, C_{g1} = C_{g2} = 0.2aF and R_{TD} = R_{TS} = 1MΩ.The BSIM4.6.1 predictive model is examined the behavior of CMOS transistor through SPICE simulations. Design parameters of CMOS transistor are W/L = 64/54nm, V_{th} = -0.3V for PMOS and V_{th} = 0.47V for NMOS.

Conclusion:

The simulation results show that the performances of the circuits presented in this paper are satisfactory thereby establishing the feasibility of using the proposed hybrid circuits in future low power ultra-dense VLSI/ULSI circuits.

Acknowledgements:

I would like to thank my friends and my faculty members without whom this Journal would have been a distant reality. I also extend my heartfelt thanks to my family and well-wishers.

References:

1. Lageweg. C.et al. Single electron encoded latches and flip flops, IEEE Trans. Nanotechnology 3(2, 237-248 (2004)
2. Wu, G., Cai, L., Kang: A 8 bit parity code generator based on multigate SET, IEEE, NEMS, 183-186 (2008)
3. Chen, Y.C.: Verification of reconfigurable binary decision diagram SE arrays, IEEE TCAD 32, 1473-1483 (2013)
4. Mizugaki Y. Blocking Charge Oscialltion in a series array of two tiny tunnel junctions with resistive ground path from its island. (2012), 194-192 IEEE Trans.
5. Shin, S.J., Jung, Park, Yoon, Silicon based ultra small multi switching SET operating at room temperature Appl. Physics., 97(10), (2010)
6. Karre, P.s. et al. Room temperature SET fabricated by focused ion beam deposition, Applied Physics 102(2), (2007), 0243161-0243164
7. Uchida, et. Al. Programmable SET logic for future low power intelligent LSI: proposal and room temperature operation, IEEE, Electron Devices 50(7), 1623-1630,(2003)
8. Inokawa, Takahash, A multiple valued logic and memory with combined Single electron and metal oxide semiconductor transistors, IEEE trans. Electron devices50(2), 462-470(2003)
9. Ionecu, S. Pott, Mahapatra, Hybrid SETMOS architecture with Coulomb blockade oscillations and high current drive, IEEE Electron devices Lett. 25(6), 411-413 (2004)
10. Gorter C.J., A possible explanation of the increase of the electrical resistance of thin metal flims at low temperatures and small field strengths. Physics 17(8), 777-780(1951)
11. Zhang, T. Kasai, Novel hybrid voltage controlled ring oscillators using SET and MOS transistor, IEEE, Nanotechnology 6(2), 170-175, 2007
12. Shin, Yang, S. R. Takahashi, Room temperature charge stability modulated by quantum effects in a Nano scale silicon island, Nano letter 11(4), 1591-197(2011)

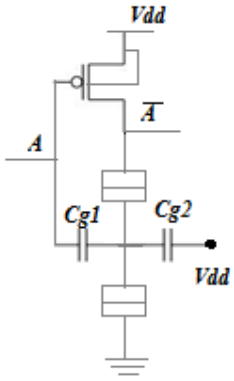

Fig 3(a) shows the SET-CMOS Inverter

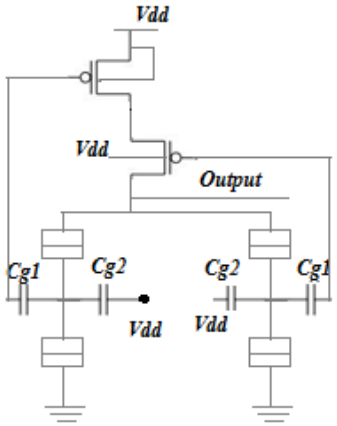

Fig 3(c) shows the 2Input of SET CMOS circuit of NOR gate

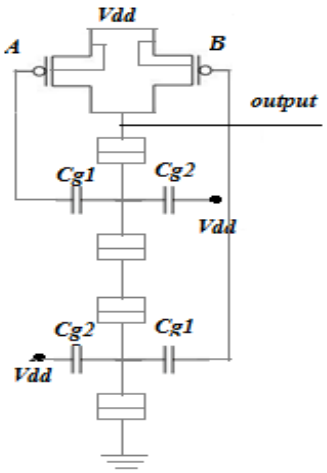

Fig 3(b) shows the 2 Input of SET-CMOS NAND gates

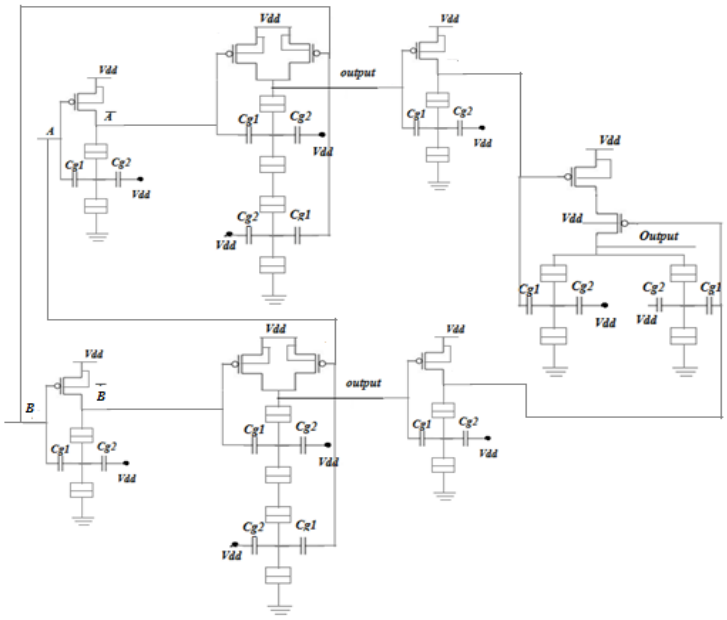

Fig 3(d) 2 input of SET-CMOS circuit of 1-bit Comparator

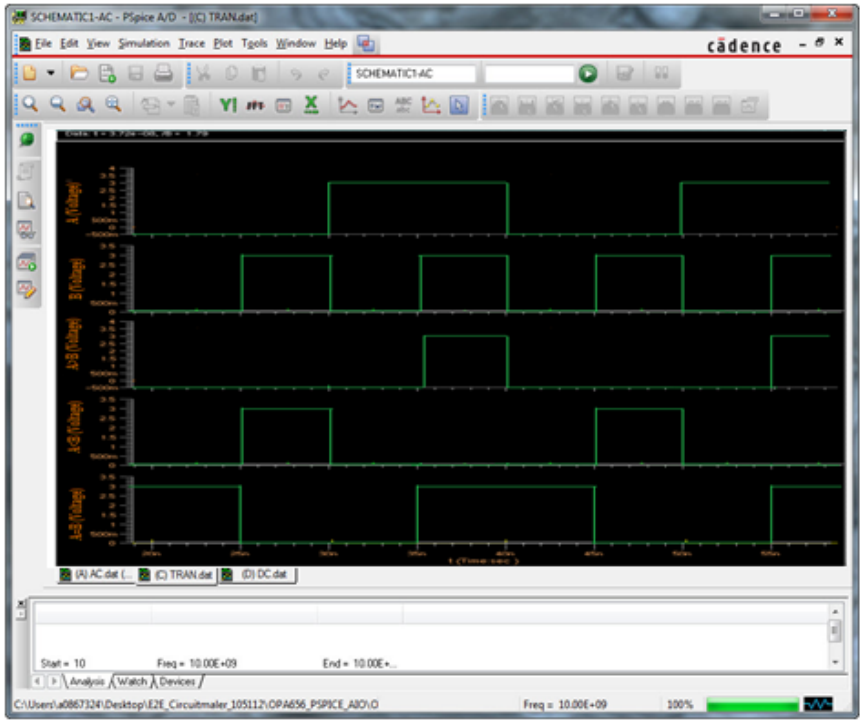

Fig 3(e) shows one bit comparator output