Efficient XOR Gate Designing using VLSI Techniques

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Abstract: *This paper concerns with the designing of different XOR gates based on 90nm technology by using some different efficient VLSI designing styles and some of the different styles are GDI, CMOS and transmission gates logic. By using these styles, the XOR gates have been implemented and comparing on basis of semicustom and auto custom design layouts. The Schematic of proposed gates has been designed and Stimulated has been developed and analyzed by using DSCH3.1 and Microwind3.1. After the layout Simulation, the parametric analysis has been done. The performance of these different designs has been analyzed and compare in terms of power and area.*

Keywords: *XOR logic gate, 90nm technology, power dissipation, CMOS, Gate Diffusion Input (GDI) & Transmission gates logic.*

I. INTRODUCTION

With the intensified research in low power, high speed embedded systems such as mobiles, laptops, etc has led the VLSI technology to scale down to nano regimes, allowing more functionality to be integrated on a single chip. The wish to improve the performance of logic circuits once based on traditional CMOS technology. The core of every microprocessor, digital signal processor (DSP), and data processing application specific integrated circuit (ASIC) is its data path. At the hearts of data paths and addressing units are arithmetic units, such as a comparators, adders, and multipliers [1]. A lot of work has been done in order to accommodate t logic circuits operating at low supply voltage (V_{dd}). V_{dd} scaling is, however,
Obstructed by the minimum operating voltage V_{dd} (min) of CMOS logic gates [2]. V_{dd} (min) is the minimum supply voltage that a logic circuit can tolerate without any damage & with increase in logic gates and CMOS technology down scaling becomes possible, this can achieved by varying channel length of transistors in such a way that for achieving ultra-low power (< 0.4 V) logic circuits V_{dd}(min)is reduced with transistor channel length ranging [3]. In VLSI (Very large scale integration) implementation, major problems are heat dissipation and power consumption. To solve these problems it is required to reduce power supply voltage, switching frequency and capacitance of transistor [4]. A PTL-based circuit that uses only one type of MOS transistor (NMOS), is Complementary pass-transistor logic (CPL). CPL consists of complementary inputs/outputs, a NMOS pass-transistor network, and CMOS output inverters [5]. Area, delay and power dissipation have emerged as the major concerns of designers. The gate delay depends on the capacitive load of the gate. The dominant term in power dissipation of CMOS circuits is the power required to charge or discharges the capacitance in the circuit. Thus, by reducing capacitance we can decrease the circuit delay and power dissipation [6]. Capacitance is in turn a function of logic cells being used in the design. One form of logic that is popular in low-power digital circuits is pass-transistor logic (PTL). Formal methods for deriving pass-transistor logic have been presented for nMOS. They are based on the model, where a set of control signals is applied to the gates of nMOS transistors. Another set of data signals are applied to the sources of the n-transistors. The PTL (Pass Transistor Logic) is most popular for low power digital circuits. As transmission gates logic technique is similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. The drawback in a transmission gate is that it needs inverted signal values to control gates of PMOS and NMOS, respectively [7]. In this paper, the comparison between the semicustom, full custom and fully automatic has been discussed based on 90nm technology. I represent the brief introduction of XOR designing by using different number of transistors by using different VLSI designing styles which helps in improving the speed of any logic circuit.

II.LOGIC TYPES

The latest technology used for constructing integrated circuits is CMOS. The technology is being used in various digital and analog logic circuits such as image sensors (CMOS sensor), data Converters, and highly integrated transceivers for many types of applications. Logical representation of CMOS is shown Figure1.

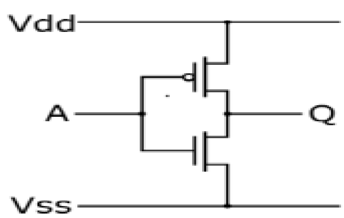


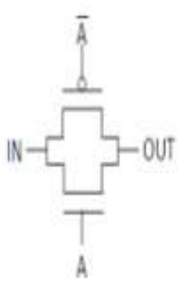
Figure I. Logic diagram of CMOS Logic

The XOR gate is a digital logic gate that implements an exclusive or; that is, a true output (1/HIGH) results if one, and only one, of the inputs to the gate is true. If both inputs are false (0/LOW) and both are true, a false output results. XOR represents the inequality function, i.e., the output is true if the inputs are not alike otherwise the output is false. A way to remember XOR is "one or the other but not both". The truth table of XOR gate is shown in table 1.

TABLE I. Truth Table of XOR Gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

A transmission gate made up of two field effect transistors, in which - in contrast to traditional discrete field effect transistors - the substrate terminal (Bulk) is not connected internally to the source terminal. The two transistors, an n-channel MOSFET and a p-channel MOSFET are connected in parallel with this, however, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other via a NOT gate (inverter), to form the control terminal. The symbol and truth table of transmission gates logic is given Figure 2(a) & 2(b).



A	IN	OUT
H	H	H
H	L	L
L	X(don't care)	Z(high imped-ance)

Figure. 2(a) Transmission Gate. 2 (b) Truth Table

The GDI cell contains three inputs: G (common gate input of nMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of nMOS). Bulks of both nMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter.

The GDI cell structure is different from the existing PTL techniques. It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies.

The basic Function Of Xor Using GDI Cell is shown in figure 3.

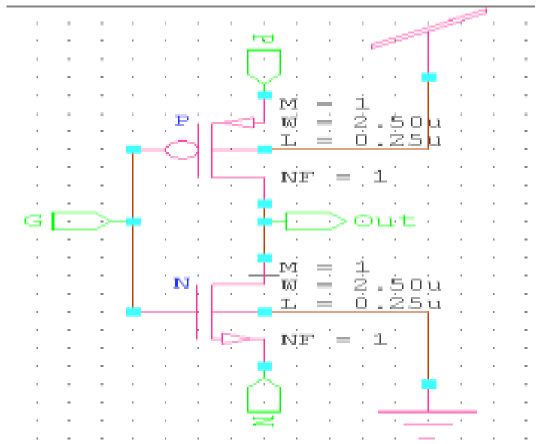


Figure 3. The Basic Function of XOR Using GDI Cell

The working of GDI logic of XOR gate is shown in table 2.

TABLE II. Basic Function of XOR Using GDI

N	P	G	OUTPUT	FUNCTION
B'	B	A	A'B+B'A	XOR

III. DIFFERENT SCHEMATIC DESIGNS OF XOR

A 2 input XOR gate is designed by using CMOS. In this design style, 6 PMOS and 6 NMOS are used. The Schematic of XOR gate using CMOS logic is shown in figure 4.

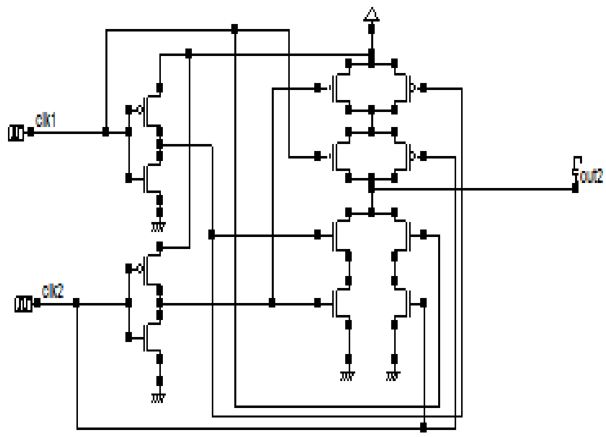


Figure 4. Schematic of XOR Using CMOS Logic

By using Transmission gates logic, the number of transistors is reduced from the conventional CMOS-XOR gate. In this design style, 3 PMOS and 3 NMOS are used. The Schematic of XOR gate 5 by using this technique is shown in figure5 of schematic design of XOR using TGL.

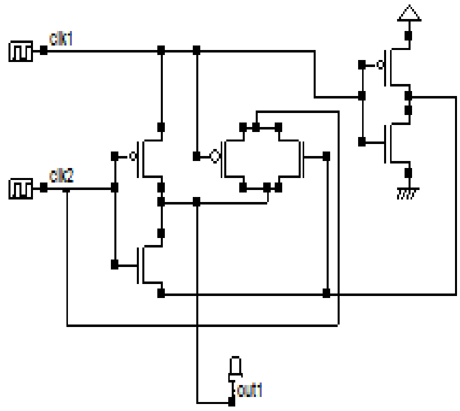


Figure 5. Schematic of XOR Using TGL

By using GDI, the number of transistors is reduced from transmission gates logic and conventional CMOS-XOR gate. In this design style, 2 PMOS and 2 NMOS are used. The Schematic of XOR gate using PTL is shown in figure 6.

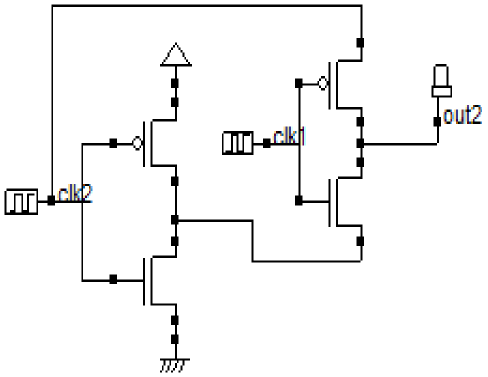


Figure 6. Schematic of XOR using GDI.

These different XOR gate designing has been alternatively checked by the truth table of XOR gate which are compared with the waveforms generated by these different styles.

IV. DIFFERENT LAYOUT SIMULATIONS

In this section, the performance of XOR logic gate based on different design technique is evaluated on semicustom layout and full custom layouts. These layouts are designed on 90nm technology. Manually, the layouts of combinational circuits sometimes become too difficult.

In fully automatic custom layout design of CMOS is developed from DSCH. The DSCH program is a logic editor and simulation then its verilog file is generated which is compiled by MICROWIND to construct its layout that is shown in Figure 7. It has been observed that average power consumption in fully automatic is 7.957 μW and area is 94.9 μm^2.

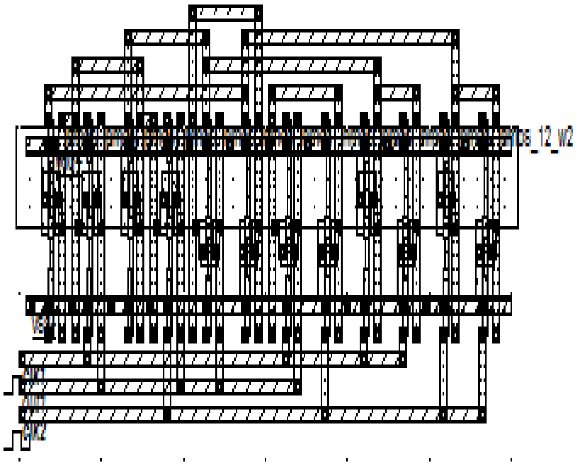


Figure 7. Fully Automatic Layout of XOR.

Simulation waveform of XOR gate in fully automatic layout design is taken by simulate the compiled file of verilog file as shown in Figure 8. Time domain representation of Layout simulations represents that the Logic '0' corresponds to a zero voltage and logic '1' corresponds to 1.2 V.

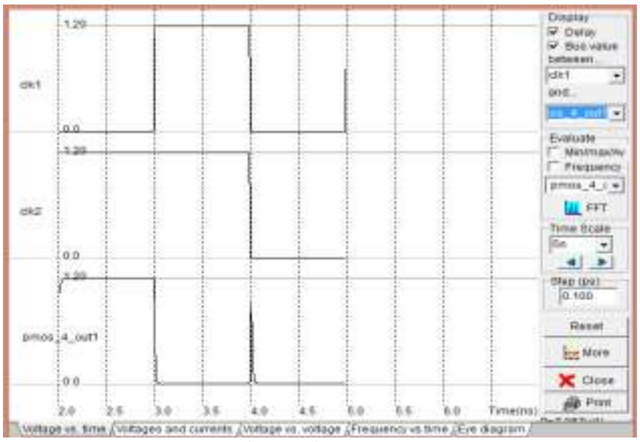


Figure 8. Simulation Waveform Of Fully Automatic

In CMOS style designing of fully automatic, there are 16 transistors to generate the design but for industry purpose we have to reduce the number of transistors used in the circuit. To reduce the number for transistors, the GDI and TGL Techniques of designing has been used which are analyzed on the basis of semicustom and full custom layout results in the form of power and area.

In semicustom layout, the design of XOR gate is created by NMOS and PMOS devices using cell generator provided by Microwind3.1 tools. The main advantage of this approach to avoid any design error. The different layout designs are shown in figure 9 & 10 by using TGL & GDI respectively.

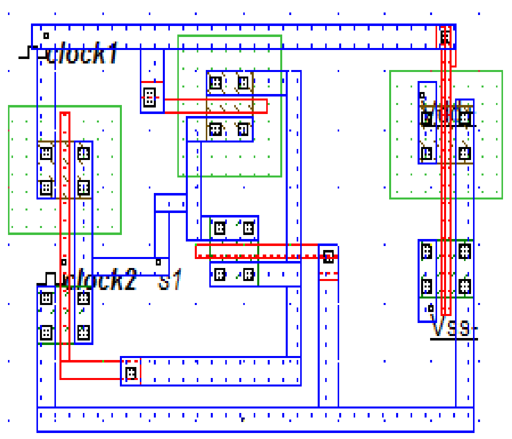


Figure 9. Semicustom Layout of XOR Gate Using TGL.

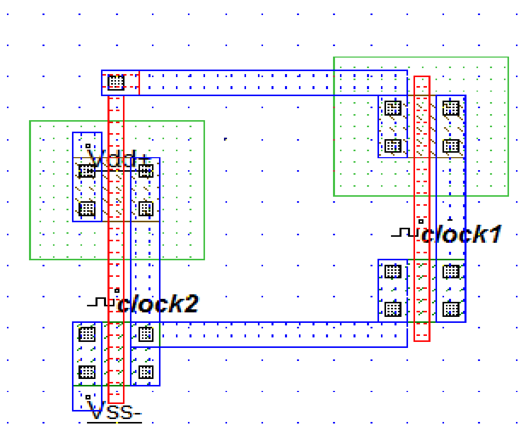


Figure 10. Semicustom Layout of XOR Gate Using GDI.

In full custom layout, the design of XOR gate is created by NMOS and PMOS. These NMOS and PMOS has been created by using lamda rule of VLSI designing and alternatively checked by DRC checker tool in Microwind3.1. The power and are has been reduced as compare to semicustom layout designs. The different layout designs are shown in figure 11 & 12 by using CMOS, TGL & GDI respectively.

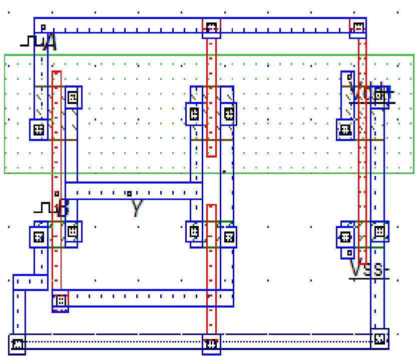


Figure 11. Full Custom Layout Of XOR Gate Using TGL.

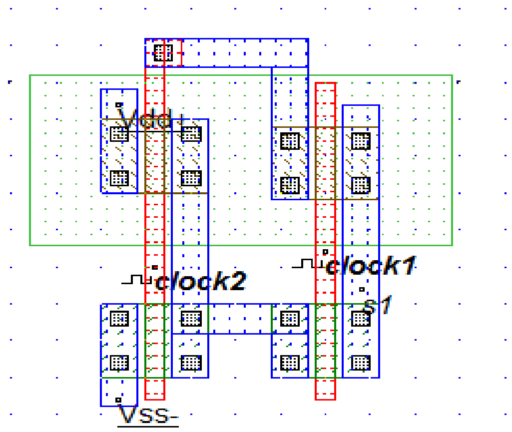


Figure 12. Full Custom Layout Of XOR Gate Using GDI

The different parameters of XOR gate are compared between semicustom and full custom based on 90nm technology. The Simulation results are shown in table 4.

TABLE III. Comparison Of Simulation Results.

Logic styles	Semicustom		Full custom	
	Power	Area	Power	Area
TGL	15.9μW	18μm^2	4.768μW	15μm^2
GDI	5.54μW	9.2μm^2	1.29μW	5.2μm^2

V. CONCLUSION

GDI technique based XOR designing is better than the conventional XOR gate and Transmission gates logic due to less number of transistors usages. Both the semicustom and full custom based layouts have their own benefits. In full custom, the power and area is reduced as compare to semicustom layout design. The area and power of GDI has been reduced as compare to TGL based on 90nm technology.

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