Pi Controlled DC-DC Converter Based on Three-State Switching Cell

Sithara Azeez[1], Sajini Susan Mathai[2]

[1]*M Tech student, EEE Department, Ilahia College of Engineering & Technology,Kerala , India*

[2]*Asst.Professor, EEE Department, Ilahia College of Engineering & Technology,Kerala , India*

Abstract— *This paper introduces a new family of PWM DC-DC non-isolated converters By substituting the converter-cell all the DC-DC converter topologies (the buck configuration) is obtained. The new converters are generated using three-state commutation cells. Comprising two active switches, two diodes and coupled inductors. This topology has 3 switching stages, thus the name given as three state switching cell. In these circuits only part of load power is transferred by the switches so switching stress is less and high power output can be attained. Advantages of this topology are less size and volume of components, wide area of continuous conduction mode, low conduction and commutation losses, and low input and output current ripple. Due to these features, the new converters are suitable for low voltage and high current application. Step down converter have overlapping and non-overlapping modes. When duty ratio is less than 0.5, we can achieve non-overlapping and continuous conduction mode. Simulations of the existing converter are done in MATALAB/SIMULINK and an experimental prototype was implemented.*

Keywords — *Buck Converter, Boost Converter, DC-DC Converters, Three State Switching Cell (3SSC).*

I. INTRODUCTION

Pulse width modulation (PWM) dc–dc converters are widely employed in numerous applications, e.g.audio amplifiers [1], uninterruptible power supplies [2], fuel cell powered systems [3], and fork lift vehicles [4]. Conventional hard switching converters typically present low power density, while attempts to further minimize the size of filter elements lead to increased switching losses, compromising the efficiency of the converters In order to overcome such limitation, several soft switching [5][6][7] approaches have been introduced .It can be achieved through either active and passive methods [8]. However, soft switching may not be achieved for the entire load range, and besides the accurate design of the resonant tank is not a trivial task, even what is also valid when active snubbers are considered [9].

Significant effort has then been made to improve the characteristics of the traditional non isolated dc-dc converter in the last few years[10]. A family of converters is also derived, which combines the advantages of reduced voltage across the switches using a three-level commutation cell, and decreased switching losses obtained from a soft switching technique. As the power rating increases, it is often required to associate converters in series or in parallel. By using interleaving techniques in high current applications, the currents through the switches become just fractions of the input current [11]. Interleaving effectively doubles the switching frequency and also partially cancels the input and output ripples, as the size of the energy storage inductors and differential-mode EMI filter in resulting implementations can be reduced [12].

In the last few years, many converters based on the three state switching cell (3SSC) have been proposed[13]-[19]. The cell can be obtained by the association of two two-state PWM cells (2SSC) interconnected to a centre tap autotransformer, from which novel converters can be derived. General advantages over conventional topologies can be achieved, e.g., the inductor is designed for twice the switching frequency, with consequent reduction of size and weight; the current through the switches is half of the input current; part of the input power is delivered to the load by the transformer instead of the main switches, consequently reducing conduction and commutation losses; lower cost switches can be used.

Within this context, this paper proposes the complete study of the dc–dc converter based on the 3SSC. Initially, some theoretical background on the 2SSC and the 3SSC is presented, leading to the conception of the improved buck converter using the so-called cell type *B*. Then, the converter operation in non overlapping mode (NOM) is described, where the main characteristics of the topology are discussed. An experimental prototype is then implemented, while the detailed discussion of experimental results is supposed to validate the theoretical assumptions and also demonstrate the merit of the proposal
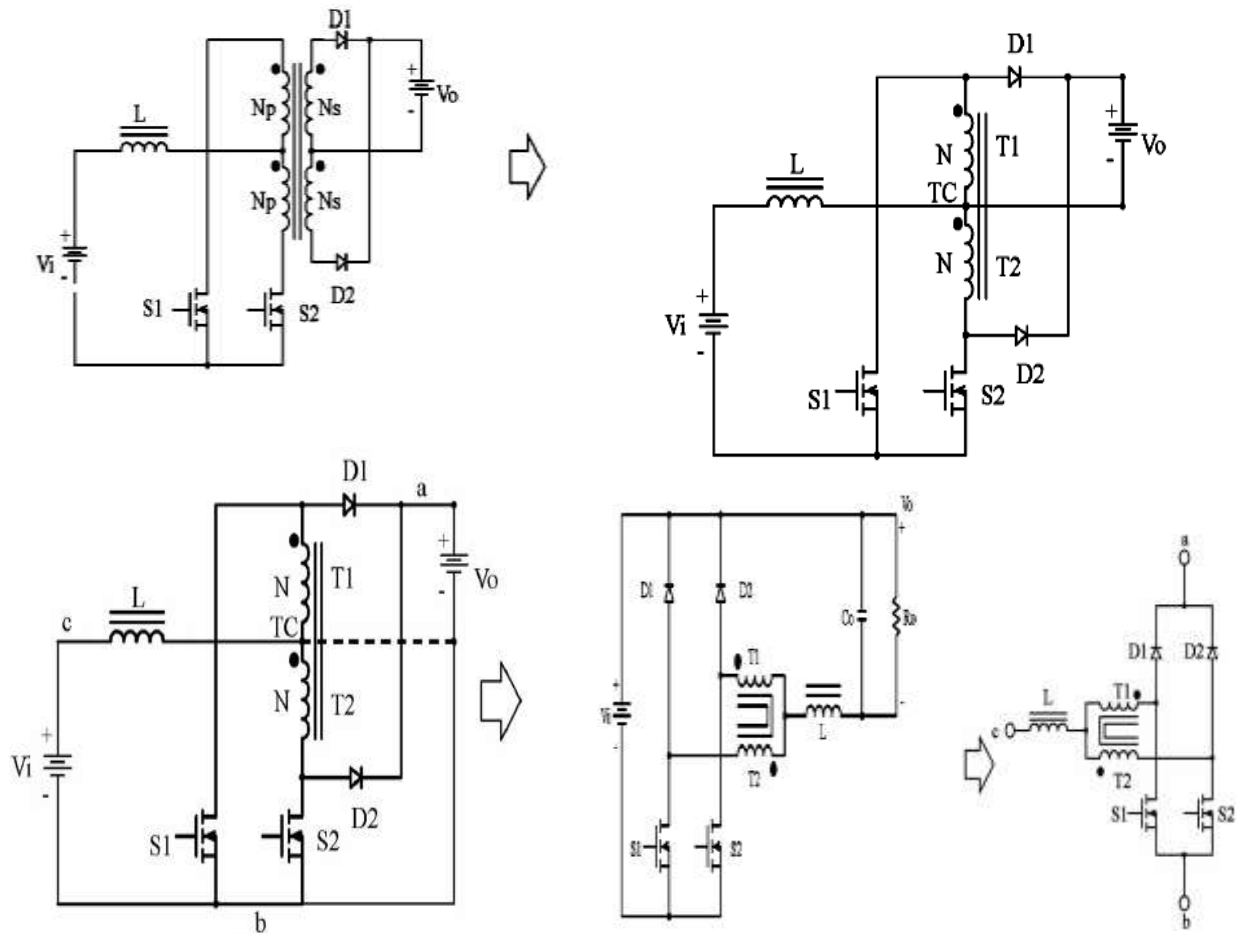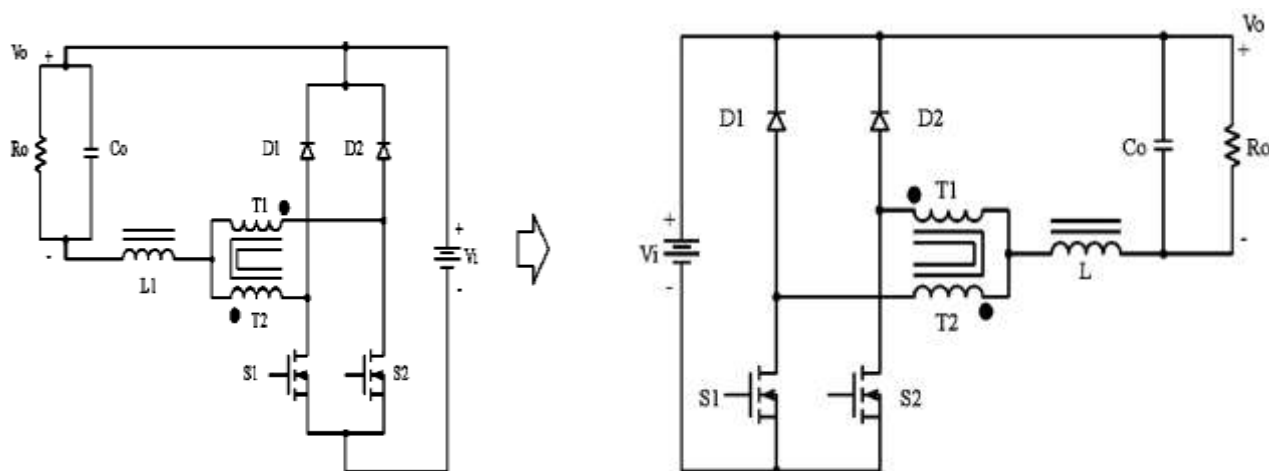
Fig.1 3SSC type B

Fig. 2 Buck converter based on the 3SSC

II. CONCEPTION OF THE THREE STATE SWITCHING CELL

The aforementioned switching cell is composed of three terminals, which are active, passive, and common. Its behaviour is based on the complementary operation of two switches connected by the common terminal. In other words, one switch is turned ON while the remaining one remains turned OFF, and vice versa. Therefore, this arrangement can be called 2SSC.

With the aim of achieving higher power density, switching frequency is usually increased, with consequent reduction of size and volume of reactive elements. In order to obtain the cell type *B*, let us consider the classical push–pull topology shown in Figure1, which is formed by switches S1 and S2 , two rectifier diodes D1 and D2 in the secondary side ,and a high-frequency transformer. The circuit corresponds to a dc–ac–dc conversion system. If the central tap transformer is considered ideal with unity turns ratio, the primary and secondary windings can be replaced by the respective magnetizing inductances, which are coupled and constitute an autotransformer. The negative terminal of the output stage represented by Vo , which was formerly connected to the central tap of the transformer, is then connected to the negative pole of the input voltage source to generate a boost topology, as seen in Figure1. Otherwise, if connected to the positive pole, a buck–boost converter is derived. The cell type *B* can then be applied to the dc–dc buck converter substituting the 2SSC, while the resulting topology is presented in Fig. 2.

It can be seen that the 3SSC is formed by two controlled switches S1 and S2 , two diodes D1 and D2 , one autotransformerT1_T2 , and one inductor L. Even though the resulting cell seems more complex with higher component count than the conventional 2SSC, the advantages over its counterpart will be clearly demonstrated in this study. For instance, the use of the 3SSC may lead to the need of switches with reduced current rating, which is desirable in step-down high-current applications.

Considering that the operation of the switch and the diode of a same leg is complementary, two modes regarding the main switches can be obtained for the proposed topology. If the duty cycle *D* is higher than 0.5, overlapping mode (OM) occurs, where two switches remain turned ON at the same time. Otherwise, if $D < 0.5$, the converter operates in NOM, while only one switch remains turned ON in a given operating stage

For the detailed description of the dc–dc buck converter using the 3SSC in NOM, the following assumptions are made:

1) the converter operates in steady state;
2) switching frequency is constant and PWM is employed to drive the switches;
3) the gating signals of the switches are 180° displaced;
4) the turns ratio of the autotransformer is unity;
5) the magnetizing current is much lower than the load current;
6) all semiconductor and passive elements are ideal

.III. OPERATION IN NOM AND CONTINUOUS . CONDUCTION MODE (CCM) (D < 0.5)

The converter operation can be defined according to four operating stages . The respective main theoretical waveforms are presented in Figure 7, where each one of the variables is defined as follows :

1) $V_g(S1)$, $V_g(S2)$—gating signals applied to switches S1and S2 , respectively;

2) I_L —current through inductor L, while the maximum and minimum values assumed by this quantity are I_M and I_m, respectively;

3) I_{S1}—current through switch S1 ;

4) I_{D1}—current through diode D1 ;

5) I_{vo}—current through the output stage, which is the sum of the currents through the output capacitor I_{co} and the load I_o;

6) V_{S1}—voltage across switch S1 ;

7) V_{D1}—voltage across diode D1 ;

8) V_L—voltage across inductor L.

FIRST STAGE [t0, t1] [see Figure 3]: Initially, switch S1 is turned ON, while switch S2 is turned OFF. The current through the inductor is divided in two parts.The first one flows through T1 and D2 with energy being delivered to the load. The second one flows through *T*2 and S1 Current sharing is maintained since the number of turns for *T*1 and *T*2 is the same. The current through *L* increases linearly. Windings *T*1 and *T*2 have the same impedance, and the voltages across them are equal to half of the input voltage Vi his stage finishes when *S*1 is turned OFF..This stage finishes when *S*1 is turned OFF.
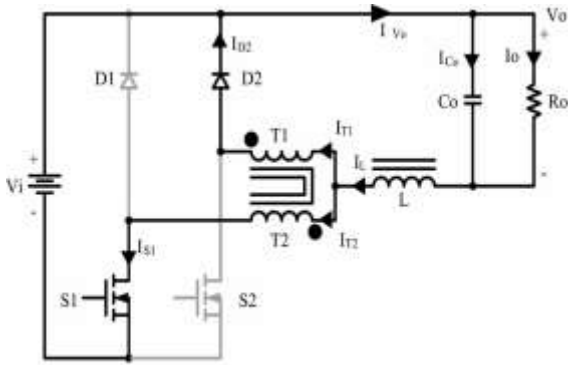
Fig. 3

SECOND STAGE [t1, t2] [see Figure:4]: Switch S1 is turned OFF, while switch S2 remains OFF. The voltage across inductor L is inverted .Diode $D1$ is forward biased while D2 remains conducting. The energy stored in L during the previous stage is then transferred to the load. The current flows through T1_T2 , according to the given polarity, what causes the magnetic flow in the core to be null. The current returns to the source analogously to the previous stage. This stage finishes when S2 is turned ON.
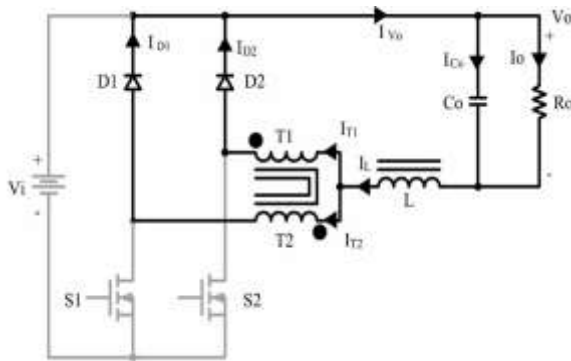
Fig. 4

THIRD STAGE [t2, t3] [see Figure 5]: Due to symmetry of the circuit, this stage is similar to the first one, although switch S2 is turned ON instead and S1 remains turned OFF. Diode $D1$ keeps conducting and D2 is reverse biased.
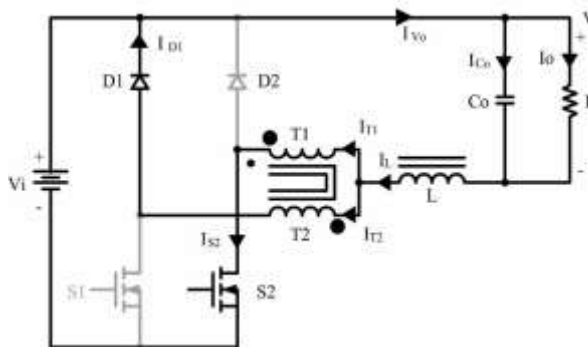
Fig. 5

FOURTH STAGE [t3, t4] [see Figure 6]: This stage is similar to the second one, as the same equivalent circuit and operating conditions are valid in this case
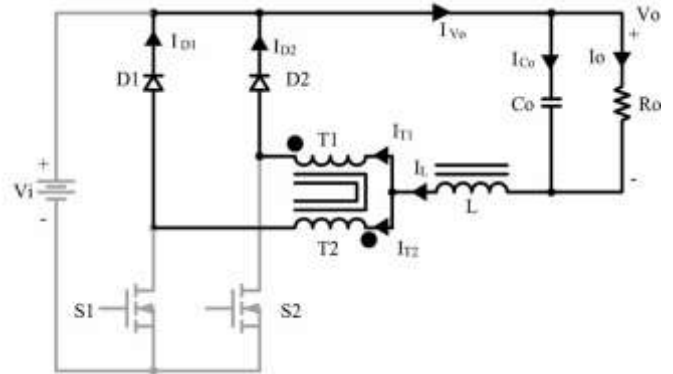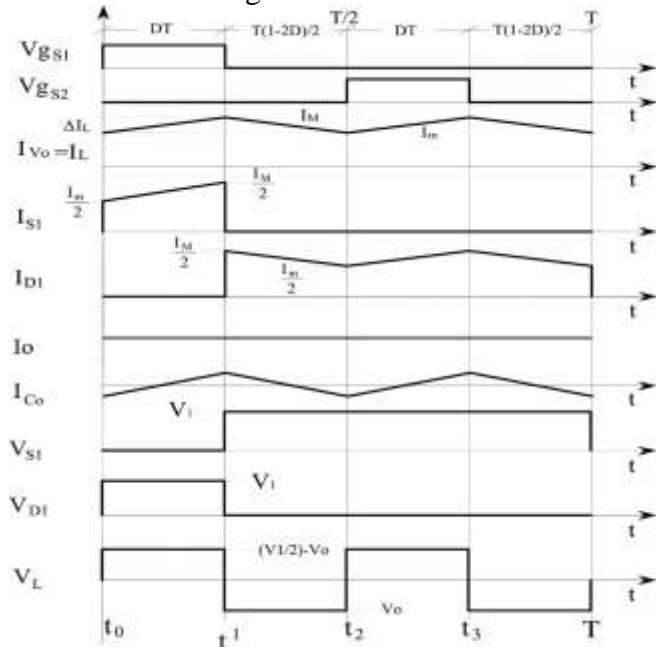
.

Fig. 6

Fig. 7 Main theoretical waveforms for NOM CCM.

IV DESIGN CONSIDERATION

A design of the proposed 3SSC buck converter, which is supposed to operate in NOM, is presented as follows:

A. Duty ratio

Considering the operation in CCM, the static gain is

$$G = D = Vo/Vi \quad (1)$$

$$Io = Po/Vo \quad (2)$$

B. Inductor

By choosing arbitrarily the ripple current, the inductance can be determined as

$$L = ((1-2D)DTsVi)/2\Delta I_L \quad (3)$$

C. *Main Switches*

The average current I_{S1}(avg) and the rms current I_{S1}(rms)

through the switch are given below

$$I_{s1(avg)} = \frac{1}{2} * I_o * D \qquad (4)$$

$$I_{s1(rms)} = \sqrt{\frac{D}{4} I_o^2 + \frac{V_i^2 T_s^2 D^2 (2D-1)^2}{48L^2}} \qquad (5)$$

Where $V_{s1} = V_i$ = threshold voltage across one main switch

D. *Capacitor*

$$Co = \Delta I_L / (4 \Pi f_s \Delta Vo) \qquad (8)$$

Where ΔVo is the output voltage ripple [V] and f_S is the switching frequency [Hz].

V. SIMULATION RESULTS AND DISCUSSIONS

The Figure. 8 shows the Simulink model for the desired converter configuration. The circuit is built using MATLAB simulation package with an input voltage of 24V, a switching frequency of 20 kHz
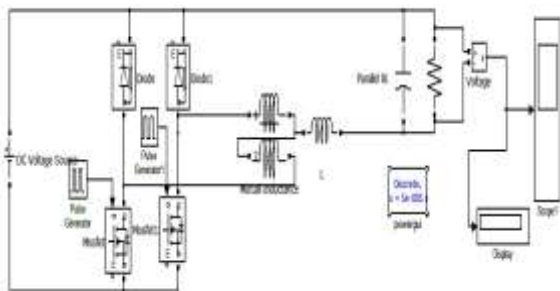

Fig. 8:.Simulink model of 3SSC buck converter

For simulating 3SSC buck converter, we uses parameter values as R=10 ohm, C=14.72µF, L=1.73m H. Input voltage is taken as 24V.
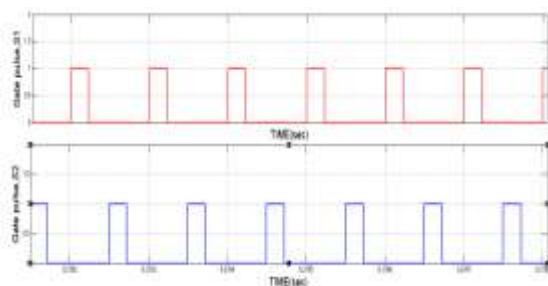

Fig. 9 Gate pulse of switches

For pulse generation we uses PWM generation and a controlled circuit is used to control output voltage.

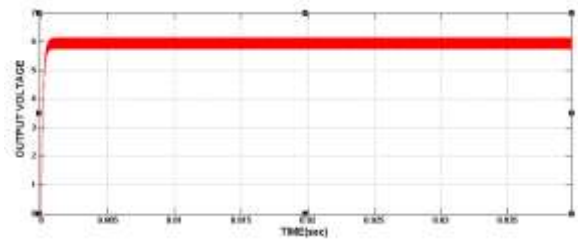Output voltage is stepped down and get 7V at duty ratio 0.3 as shown in figure 10

Fig. 10 Output voltage waveforms of 3SSC buck converter.

Figure11 and 12 shows the voltage and current sharing of the switches. From this it is evident that the proposed converter is relevant in high power converters such that we can use lower current rating switches
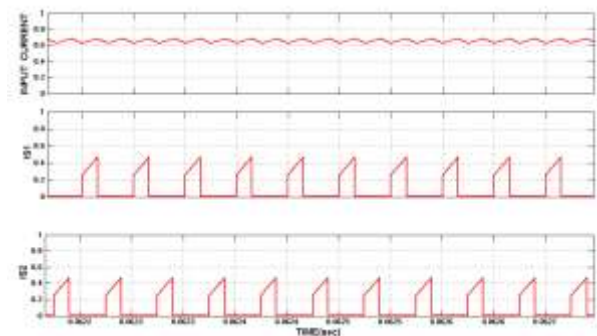

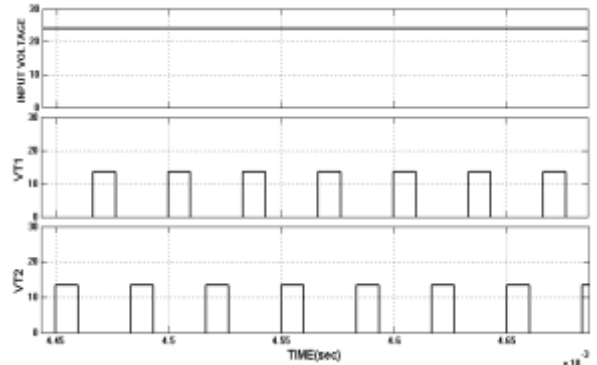Figure 11: Waveform showing current sharing

Figure 12: waveform showing voltage sharing

Figure 13 shows the voltages across switches S1 and S2, as well as the currents through inductor *L* and switch S1 . It becomes evident that the switching frequency is half of the ripple current frequency, what leads to the reduction of magnetic elements

. Figure 14 shows the voltages across D1,D2,S1,S2.It becomes evident that the operation of such semiconductor elements is complementary
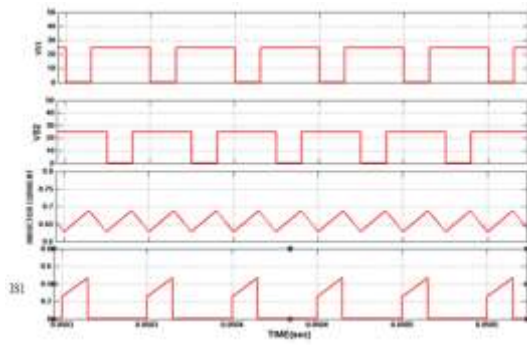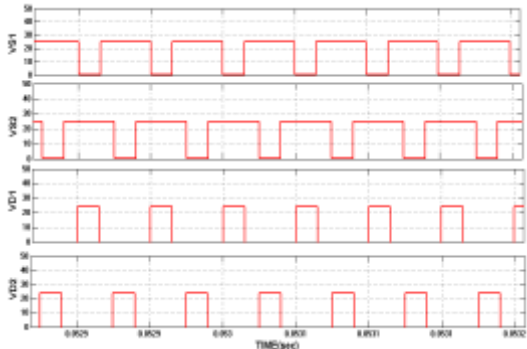
Figure 13:Inductor voltage and current

Figure:14 Voltages across D1,D2,S1,S2

In Open loop configuration, for an input voltage of 24V, the output voltage is 5.8V . which is less than the desired output (5.8<7.2).
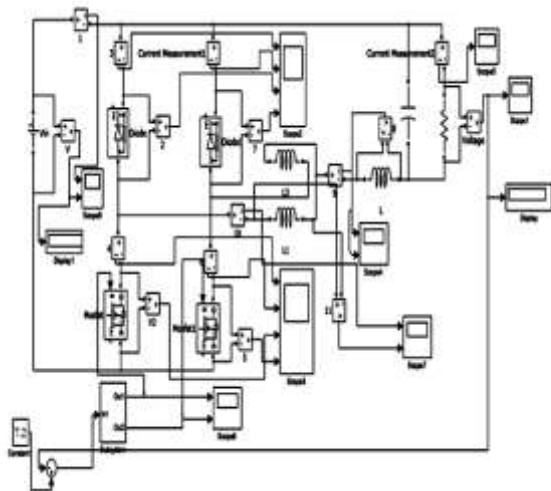

Figure 15:.Simulink model of 3SSC buck converter with PI controller

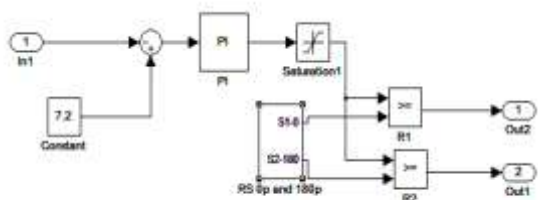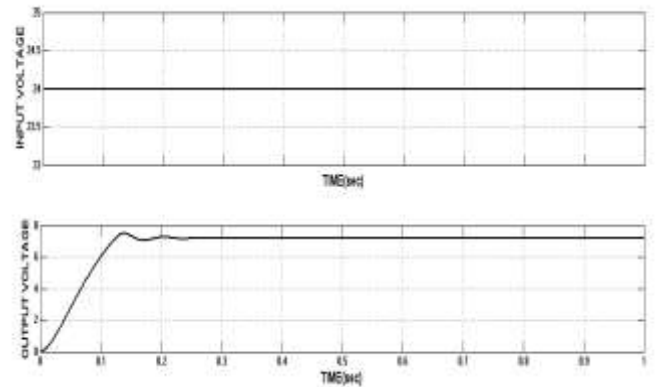Figure:16 Sub system for giving pulse

Figure:17 Input-output waveform of 3SSC buck converter with PI controller.

Compared to Open loop , Closed loop using PI controller had given more precise output, reduced steady state error and reduced overshoot and ripple. The output voltage is more regulated with PI controller .Smooth changes are observed.

VI EXPERIMENTAL RESULTS

TABLE I
DESIGN SPECIFICATIONS

PARAMETER	VALUE
Input voltage	24V
Output voltage	7.2 V
Inductor	1.73mH
Capacitor	100μF
Switching frequency	20kHz
Duty ratio	0.3
Load resistance	20 ohm ,50 W

The specifications are listed in Table I and can be used in the implementation of an experimental prototype.

The main components of hardware is three state switching cell converter ,DsPIC microcontroller for controlling the switching of the dc-dc converter and a driver circuit is used in between the MOSFET and DsPIC microcontroller. Power supply is provided for each of these components according to their requirements.

Figure 18 shows the hardware setup of the project. The output is analyzed with the help of DSO. The output waveforms are shown below. The output of buck converter is shown in Figure 20 .For a 24 V input the buck converter output is steady at 7.8 V at a switching frequency 20 kHz
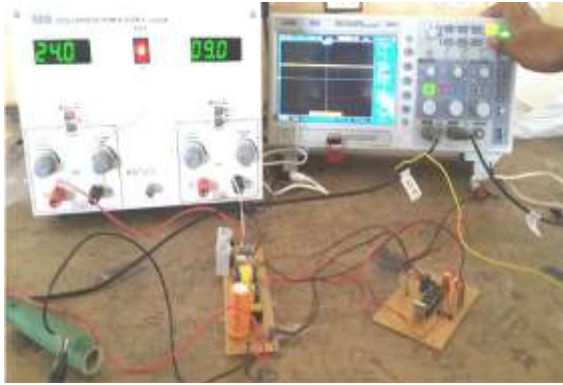
Figure:18 Hardware setup
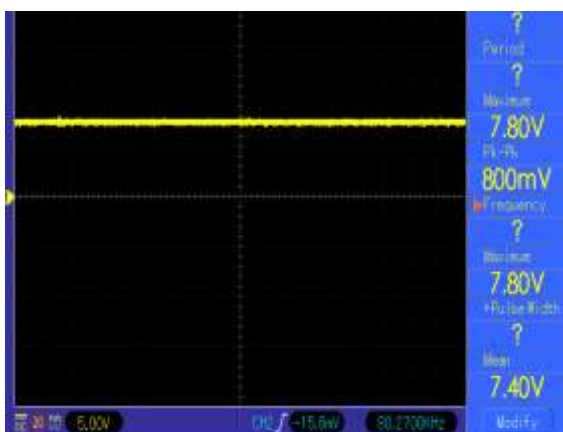

Figure 19 Gate pulses to two switches

Figure:20 Output Waveform

The 3SSC converter was evaluated over a wide load range and the efficiency curve of the converter operating at20 kHz is presented in Fig. 21. That is, the use of the 3SSC leads to high efficiency, which is higher than 94% practically over the entire output power range, demonstrating the merit of the proposed converter
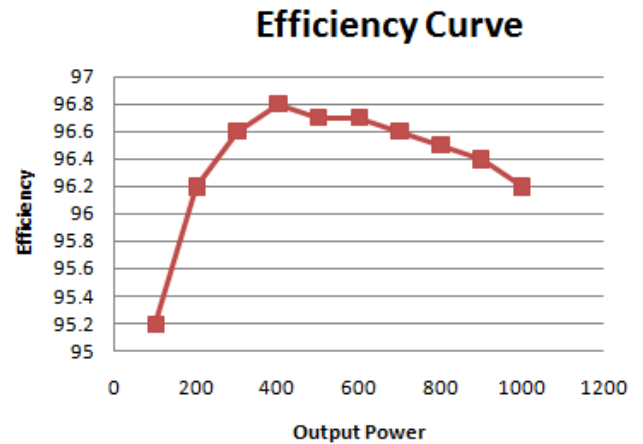

Figure:21 Efficiency curve as the function of the output power.

With the aim to further reduce voltage and/or current stress, other topologies such as multilevel converters[20][21], interleaving ensure current sharing with turn off snubber [22][23][24]and its difficulty to acquire soft switching[25] and the synchronous dc-dc buck converter witn interleaved multiphase and integrated coupled inductor[26] has been thoroughly investigated .

VII. CONCLUSION

Step down converter based on three state switching cell for high application were simulated and an experimental prototype was then implemented. In step down converter an input voltage 24 V is given and we got 7.2 V as output at duty ratio 0.3.. A controlled feedback is given to the buck converter using PI controller. .Simulations are done in SIMULINK/MATLAB R2010a. From the simulation results output is more precise, overshoot is reduced and less amount of ripples were observed.

REFERENCES

[1] M. Berkhout and L. Dooper, "Class-D audio amplifiers in mobile applications,"*IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 5,pp. 992–1002, May 2010

[2] E. K. Sato,M. Kinoshita, Y. Yamamoto, and T. Amboh, "Redundant highdensityhigh-efficiency double-conversion uninterruptible power system,"*IEEE Trans. Ind. Appl.*, vol. 46, no. 4, pp. 1525–1533, Jul./Aug. 2010

[3] S. V. Araujo, R. P. Torrico-Bascop´e, and G. V. Torrico-Bascop´e, "Highly efficient high step-up converter for fuel-cell power processingbased onthree-

state commutation cell," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6,

[4] Z. Amjadi and S. S. Williamson, "Power-electronics-based solutions for plug-in hybrid electric vehicle energy storage and management systems,"*IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 608–616, Feb. 2010.

[5] G. Yao, Y. Shen,W. Li, and X. He, "A new soft switching snubber for the interleaved boost converters," in *Proc. 35th Annu. IEEE Power Electron.Spec. Conf.*, Jun. 2004, pp. 3765–3769

[6] I.Matsuura, K. M. Smith, Jr., and K. M. Smedley, "A comparison of activeand passive switching methods for PWM converters," in *Proc. 29th Annu.IEEE Power Electron. Spec. Conf.*, May 1998, vol. 1, pp. 94–100.

[7] G. Hua and F. C. Lee, "Soft-switching techniques in PWM converters,"*IEEE Trans. Ind. Electron.*, vol. 42, no. 6, pp. 595–603, Dec. 1995.

[8] K. Fujiwara and H. Nomura, "A novel lossless passive snubber for softswitching boost-type converters," *IEEE Trans. Power Electron.*, vol. 14,no. 6, pp. 1065–1069, Nov. 1999.

[9] D. S. Oliveira, Jr., C. E. A. Silva, R. P. Torrico-Bascop´e, F. L. Tofoli,C. A. Bissochi, Jr., J. B. Vieira, Jr., V. J. Farias, and L. C. de Freitas,"Analysis, design, and experimentation of a double forward converterwith soft switching characteristics for all switches," *IEEE Trans. PowerElectron.*, vol. 26, no. 8, pp. 2137–2148, Aug. 2011

[10] J. P. Rodrigues, S. A. Mussa,M. L.Heldwein, and A. J. Perin, "Three-level ZVS active clamping PWM for the dc–dc buck converter," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2249–2258, Aug. 2009.

[11] Y. Jang and M. M. Jovanovic, "Interleaved boost converter with intrinsic voltage-doubler characteristic for universal-line PFC front end," *IEEETrans. Power Electron.*, vol. 22, no. 4, pp. 1394–1401, Jul. 2007.

[12] D. J. Perreault and J. G. Kassakian, "Distributed interleaving of paralleled power converters," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 44, no. 8, pp. 728–734, Aug. 1997.

[13] S. V. Araujo, R. P. Torrico- Bascop´e, and G. V. Torrico-Bascop´e, "Highly efficient high step-up converter for fuel-cell power processing based on three-state commutation cell," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 1987–1997, Jun. 2010.

[14] S. V. Araujo, R. P. Torrico-Bascop´e, G. V. Torrico-Bascop´e, and L. Menezes, "Step-up converter with high voltage gain employing threestate switching cell and voltagemultiplier," in *Proc. Power Electron. Spec. Conf.*, 2008, pp. 2271–2277.

[15] R. A. da Camara, C.M. T. Cruz, and R. P. Torrico-Bascop´e, "Boost based on three-state switching cell for UPS applications," in *Proc. Brazilian Power Electron. Conf.*, 2009, pp. 313–318.

[16] G. V. Torrico-Bascope, R. P. Torrico-Bascop´e, D. S. Oliveira, Jr., S.V. Ara´ujo, F. L. M. Antunes, and C. G. C. Branco, "A generalized high voltage gain boost converter based on three-state switching cell," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2006, pp. 1927–1932.

[17] G. V. Torrico- Bascop´e, R. P. Torrico-Bascop´e, D. S. Oliveira, Jr., S. V. Ara´ujo, F. L. M. Antunes, and C. G. C. Branco, "A high step-up converter based on three-state switching cell," in *Proc. IEEE Int. Symd. Electron.*, 2006, pp. 998–1003.

[18] R. P. Torrico-Bascop´e, C. G. C. Branco, G. V. Torrico-Bascop´e, C. M. T. Cruz, F. A. A. de Souza, and L. H. S. C. Barreto, "A new isolated DC–DC boost converter using three-state switching cell," in *Proc. Appl. Power Electron. Conf. Expo.*, 2008, pp. 607–613.

[19] E. E. Landsman, "A unifying derivation of switching regulator topologies," in *Proc. IEEE Power Electron. Spec. Conf.*, 1979, pp. 239–243.

[20] S. Busquets-Monge, S. Alepuz, and J. Bordonau, "A bidirectional multilevel boost–buck dc–dc converter," *ITrans. Power Electron.*, vol. 26, no. 8, pp. 2172–2183, Aug. 2011

[21] J. P. R. Balestero, F. L. Tofoli, R. C. Fernandes, G. V. Torrico-Bascop´e,and F. J. M. Seixas, "Power factor correction boost converter based onthe three-state switching cell," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3,pp. 1565–1577, Mar. 2012.

[22] M. Roslan, K. H. Ahmed, S. J. Finney, and B.W.Williams, "Improved instantaneousaverage current-sharing control scheme for parallel-connected inverter considering line impedance impact in microgrid networks," *IEEETrans. Power Electron.*, vol. 26, no. 3, pp. 702–716, Mar. 2011.

[23] N. Genc and I. Iskender, "DSP-based current sharing of average current controlled two-cell interleaved boost power factor correction converter," *IET Power Electron.*, vol. 4, no. 9, pp. 1015–1022, 2011.

[24] Y.-M. Chen, S.-Y. Tseng, C.-T. Tsai, and T.-F. Wu, "Interleaved buck converters with a single-capacitor turn-off snubber," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 40, no. 3, pp. 954–967, Jul. 2004.

[25] K. M. Smith, Jr. and K.M. Smedley, "Properties and synthesis of lossless, passive soft switching converters," in *Proc. 1st Int. Congr. Israel Energy Power Motion Control*, May 1997, pp. 112–119.

[26] L. X. Chao, Z. Bo, Y. J. Sheng, J. Gallagher, and F. J .Gen, "A nonisolatedvoltage regulator module with integrating coupled-inductor," in *Proc. Power Electron. Spec. Conf.*, 2005, pp. 438–442.