Design Low-Power Pulse-Triggered Flip-Flop using 90 nm CMOS Technology

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Abstract—*VLSI Design analysis of three important considerations is power, area and delay. Flip-flop is one of the most power consumption components. As the power budget of today's portable digital circuits is severely limited. It is important to reduce the power dissipation in both clock distribution networks and Latch design. Pulse generation Control logic design of the Flip Flop is reduce the power compare to other Flip Flop. In this paper, we present a pulsed triggered Flip-Flop design based on a novel pulse generator circuit. Our design achieves significantly improved speed when compared to recent pulsed Flip-Flop design, as well as a Existing Flip Flops. We are going to design a compare various type of flip flops & its effect of this clocking system & compare their power consumption & to create a new design using this clocking system.*

Keywords-: *Flip-flop, Low power, Pulse-triggered.*

I. INTRODUCTION

Flip-Flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. The digital designs nowadays often adopt intensive pipelining techniques and employ many FF rich modules and also estimated that the power consumption of clock system, which consists of clock distribution networks and storage elements is as high as 20% to 45% of the total system power. Pulse triggered flip flop (P-FF) is considered as a popular alternative to the conventional master slave based FF in the application of high speed operations. Besides the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system. A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master slave configuration, and is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. P-FFs are thus less sensitive to clock jitter. The pulse generation circuitry requires delicate pulse width control in the face of process variation and the configuration of pulse clock distribution network . Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit. In an implicit type P-FF, the pulse generator is a built in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Implicit-type designs, however, face a lengthened discharging path in latch design, which leads to inferior timing characteristics. The situation deteriorates further when low power techniques such as conditional capture, conditional precharge, conditional discharge, or conditional data mapping are applied.

II. Conventional Explicit Type P-FF Designs

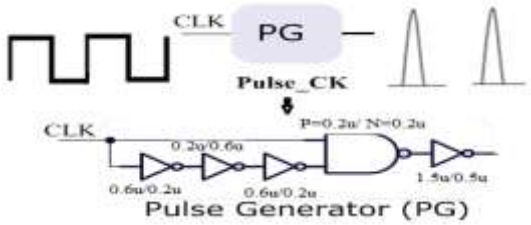

Fig.2.1.Pulse Generator Design

The Fig1 shows the Pulse is derived from clock edge in the input then output is pulse is generated after clock edge.PF-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate. Without generating pulse signals explicitly, implicit type P-FFs is in general more power-economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an *n*-bit register). In this brief, we will thus focus on the explicit type P-FF designs only.

A.EP-DCO FLIP FLOP

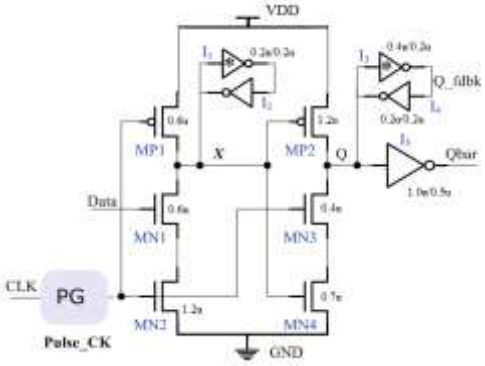

Fig. 2.2. ep-DCO

The Fig2.2 Shows the ep-DCO means Explicit P-FF design, named data-close to-output. In this circuit Pulse generation design can be used a NAND-logic-based pulse generator and a semi dynamic true-single-phase-clock structured latch design. In this P-FF design, inverters I1 and I2 are used to hold the internal node X, and inverters I3 and I4 are used to latch data. The pulse width is determined by the delay of three inverters. This design main drawback, i.e., the internal node X is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation.

B. CD FLIP FLOP

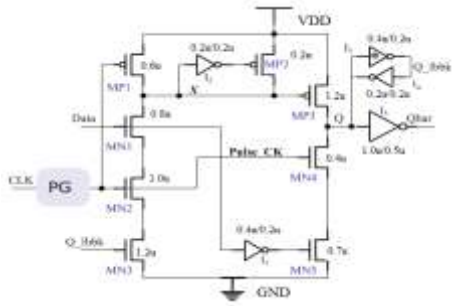

Fig.2. 3. CDFF

The Fig 2.2 to overcome this problem, many remedial measures such as conditional discharge, conditional capture and conditional precharge, conditional pulse enhancement scheme have been proposed . Fig.2.3 shows a conditional discharged (CD) technique .this circuit can be used an extra nMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1." In addition, the keeper logic for the internal node *X* is simplified and consists of an inverter plus a pull-up pMOS transistor only.

C. Static-CD FLIP FLOP

Fig.2.4 shows Static conditional discharge flip-flop, this circuit design using a static conditional discharge technique . It differs from the CDFF design in using a static latch structure. Node *X* is thus exempted from periodical precharges.

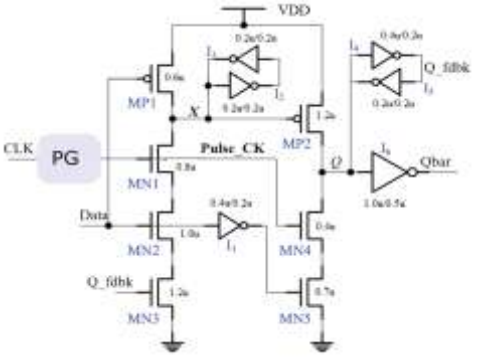

Fig.2. 4. Static-CDFF

It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption.

D. MHL FLIP FLOP

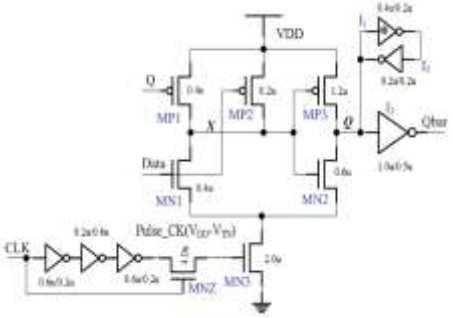

Fig. 2.5. MHLFF

The Fig2.5 shows the modified hybrid latch flip-flop (MHLFF) , This circuit also uses a static latch. The keeper logic at node *X* is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node *X* when Q equals 0. Despite its circuit simplicity, the MHLFF design encounters two drawbacks. First, since node *X* is not predischarged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one VT*)* is applied to the discharging transistor MN3. Second, node *X* becomes floating in certain cases and its value may drift causing extra dc power.

E.**TSPC FLIP FLOP**

A SFTTFF a signal feed-through technique to improve this delay. Similar to the SCDFF design, the SFTTFF design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. First, a weak pull-up PMOS transistor MP1 with

gate connected to the ground is used in the first stage of the TSPC latch.

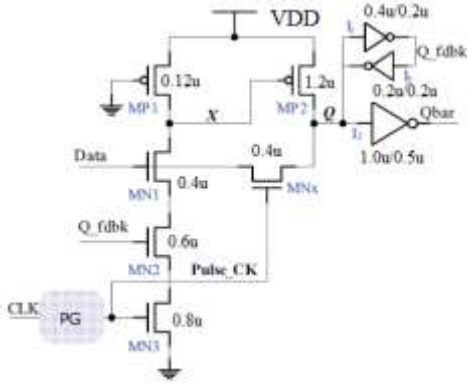

Fig.2.6. **SFTTCFF**

This gives rise to a pseudo-NMOS logic style design, and the charge keeper circuit for the internal node X can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node X. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme)as shown in fig 2.6

III. PROPOSED P-FF DESIGN

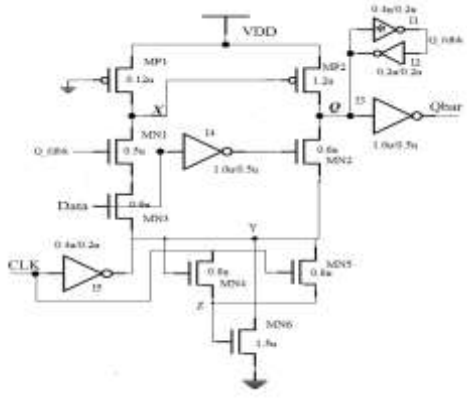

Fig 3.1 Schematic of the proposed P-FF design.

Proposed P-FF Design is also explicit pulse signals are generated. This circuit can be reduced number of transistors in Latch design and Clock Pulse generation circuit. The Clock pulse generation design by using the Pass Transistor Logic family MN3 & MN4, These two transistor discharging MN5.The clock pulse applied input of I5, the MN4 & MN5 transistor are gate and drain are connected clock pulse and inverted clock pulse, the MN5 transistor gate is connected Z node as shown in fig3.1. At the rising edges of the clock, both transistorsMN3 and MN4 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor MN5 by a time span defined by the delay inverter I5.The switching power at node Z can be reduced due to a diminished voltage swing. Where the discharge control signal is driven by a single transistor, parallel conduction of two NMOS transistors (N3 and N4) speeds up the operations of pulse generation.

In Latch design reduced the X node discharging N1&N2 transistor only. So we will be having much reduced power and area when compared to the other P-FF designs and avoids unnecessary internal node transitions to reduce power consumption and delay. So proposed design reduced power and area when compared to the other P-FF designs. At the same time due to the reduced no of transistor count. we can reduce the delay oriented things also. Thus we are reducing the overall switching delay and power, area consumption. So this circuit will be acting as good sequential elements when compared to other flip-flop design. At the same time due to the reduced no of transistor count we can reduce the delay oriented things also. Thus we are reducing the overall switching delay and power, area consumption. So this circuit will be acting as good sequential elements when compared to other flip-flop design.

IV. SIMULATION RESULTS

To evaluate the performance, Pulse-Triggered Flip-Flop discussed in this paper are designed using 90-nm CMOS technology. All simulations are carried out using MICROWIND simulation tool at nominal using MICROWIND simulation tool at nominal conditions with 1GHz frequency range. Pulse-Triggered Flip-Flop design in Soft Ware Microwind tool is shown in Fig. 4(a) & 4(f).The layout simulation window appears with inputs and output as shown in Fig.4(g)&4(l),the power consumption is also shown on the right bottom portion of the window.

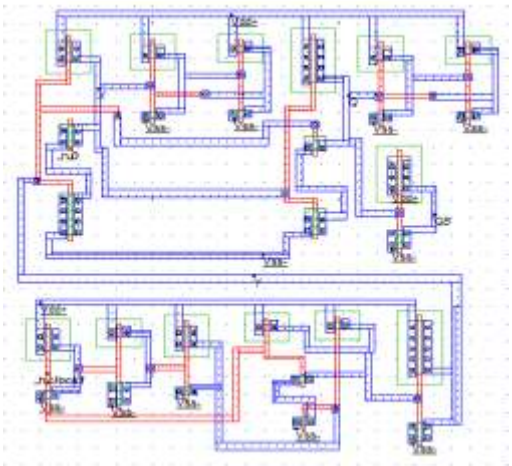

Fig 4.(a).ep-DCO Flip flop layout.

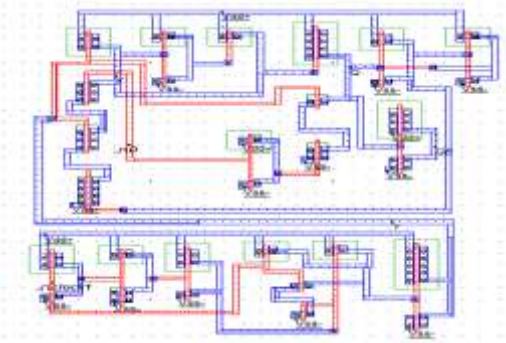

Fig 4(b).CD Flip flop layout.

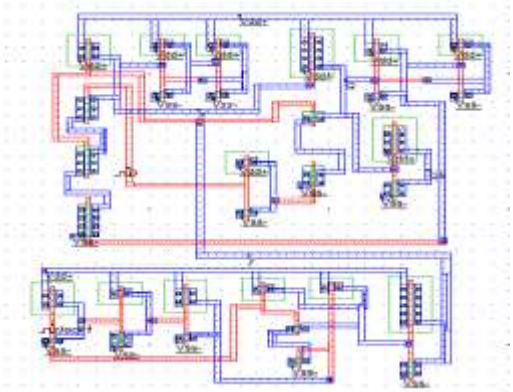

Fig 4(c).Static-CD Flip flop layout.

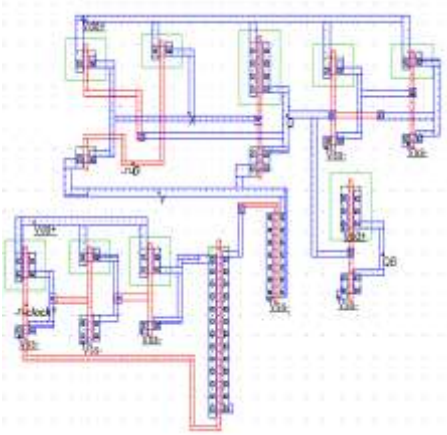

Fig 4(d).MHL Flip flop layout.

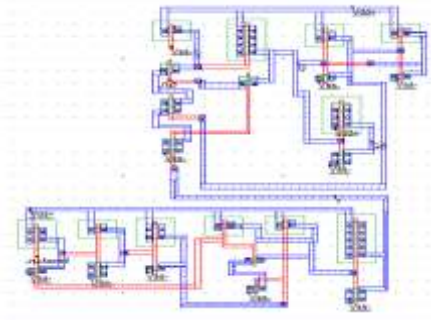

Fig 4(e) .SFTT Flip flop layout.

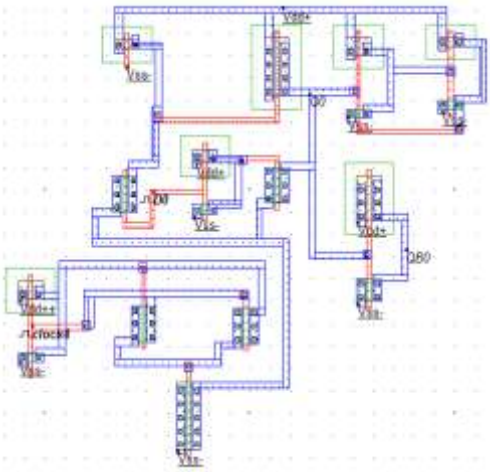

Fig 4(f).Proposed P- Flip flop layout.

Fig. 4(g) Simulation Waveform of ep-DCO Flip flop.

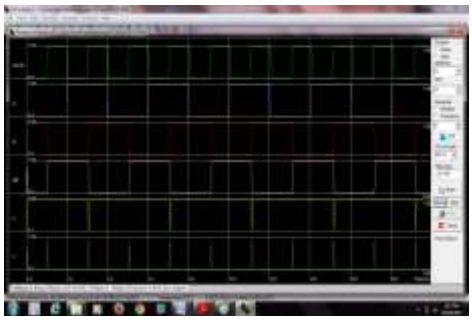

Fig. 4(h) Simulation Waveform of CD Flip Flop.

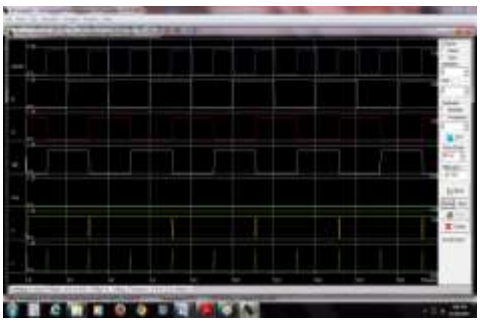

Fig.4(i) Simulation Waveform of Static CD Flip Flop.

Fig. 4(j) Simulation Waveform of MHL Flip flop

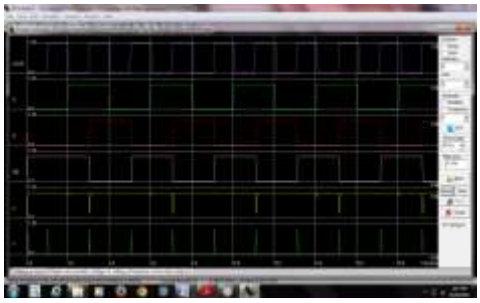

Fig. 4(k) Simulation Waveform of SFTT Flip flop.

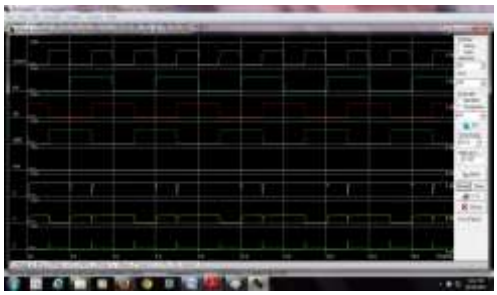

Fig.4(l) Simulation Waveform of Proposed P- FF.

V. RESULT COMPARISON

The comparison of result summarizes some important performance indexes of these P-FF designs as shown in Table1. These include transistor count, Area, D to Q Delay & Power in UMC 90-nm technology.

P-FF	NO. of Tran-sistor	Area (μm^2)	Power (µw)	D to Q Delay (ps)
ep-DCO FF	P=13 N=15	159.3	9.43	1147
CDFF	P=14 N=16	173.4	9.37	1146
Static CDFF	P=14 N=17	174	9.61	1143
MHLFF	P=9 N=10	128.4	9.01	1141
SFTTFF	P=11 N=13	147	7.38	1137
Proposed P-FF	P=7 N=11	117	3.58	974

VI. CONCLUSION

This paper concludes that Proposed P-FF designed with 17 Transistors. Proposed a pulsed triggered Flip-Flop design based on a novel pulse generator circuit. Our design achieves significantly improved speed when compared to re-cent pulsed Flip-Flop design, as well as a Existing Flip Flops. We are going to design a compare various type of flip flops & its effect of this clocking system & compare their power consumption & to create a new design using this clocking system**.** Proposed P-FF design reduced the is having less power consumption. The Flip-Flops are simulated for 90nm technology using the MICROWIND Tool. The comparisons of Different P-FFs **are** shown in Table 1. With all these results Proposed PP-FF speed performance and power are better than Ep-DCO, MHLLF, CDFF, SCDFF, SFTTFF designs.

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