Comparative Analysis of Domino Logic Circuits for Better Noise and Delay Performance

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Abstract *— High speed and lower power consumption are the most important aspects in microprocessors as the technology curtails. Dynamic logic technique is preferred over static logic technique for the higher performance circuit due to its faster speed and lesser area overhead. In this paper we compare the power and delay for the various domino circuits provided with 8-bit, comparison of power, delay, and unit noise gain (UNG) of different topologies. The simulation is performed in Cadence Virtuoso at 90nm and 65nm process technology with supply voltage 1V and 0.9V, operating temperature of 27 ^{0}C for fair comparison of results.*

Keywords — *Domino Logic, High speed, Low power, UNG.*

I. INTRODUCTION

In comparison to static CMOS circuits, dynamic CMOS circuits have a large number of advantages such as lower number of transistors, low-power, higher speed, short-circuit power free and glitch-free operation. Because of these properties, high performance systems are realized using dynamic CMOS circuits. With the requirement of low power and higher speed microprocessors, the enhanced use of portable devices results in expeditious growth in VLSI circuits [1]. In modern VLSI circuits dynamic domino logic is widely used due to its high performance superiority over static logic. But the major drawbacks of dynamic logic are high power dissipation and less immunity to noise [2, 3].

As with the scaling down of the technology, it results in the increment of leakage current which depends on gate oxide thickness, doping profile, channel dimension etc due to sub- threshold conduction, gate oxide tunneling, and reverse bias junction conduction. And as a result of this, the low noise margin and high static power dissipation becomes the most dominant factors in the design of VLSI circuits and for the wide fan-in dynamic OR gates [4]. Wide fan-in OR gates plays a very important role in critical path of microprocessor so as to achieve high performance operation [5].

Power dissipation of a logic gate is comprises of dynamic power and static power. Dynamic power results from the switching power which is due to the charging and discharging of load capacitance and short circuit power which is due to the short circuit current during output transitions whereas static power results due to the leakage current. And the increment of this leakage current in proportionally with the scaling down of technology will degrades the performance of the circuit. Thus, it is essential to diminish the leakage power of logic gates [6].

Typical Features

- Domino has smaller area than conventional CMOS logic (as does all Dynamic Logic).
- Parasitic capacitances are smaller so that higher operating speeds are possible.
- Operation is free of glitches as each gate can make only one transition.
- Only non-inverting structures are possible because of the presence of inverting buffer.
- Charge distribution may be a problem

The rest of the paper is arranged as follows. Section II, studies five types of circuits that have been proposed in related literatures, standard footless domino logic, standard footed domino logic, conditional keeper domino logic, high speed domino logic, split domino logic and high speed clock delay domino logic. Simulation results of different methods explained in section II is compare in section III. This comparison includes delay, power, Unit Noise Gain (UNG) for each method.

II. LITERATURE REVIEW

In the literature survey, the various type of domino logic configurations are shown:

(a) Footless Standard Domino Logic & Footed Standard Domino Logic

Firstly considering the footless standard domino logic and footed standard domino logic as shown in Fig.1 and 2. In conventional domino logic, a keeper transistor is utilized as a feedback for retaining the state of the dynamic node. But the resulting contention between the keeper transistor and pull down networks reduces the power and speed characteristics of the circuit [7]. Now in comparison with the footless standard domino logic, footed standard domino logic achieves better immunity to noise due to the stacking effect. To achieve the improvement in robustness of

the standard domino circuits, keeper upsizing can be done. But this upsizing of keeper transistor results in contention which degrades the power and evaluation delay characteristics of the conventional domino circuits [8].

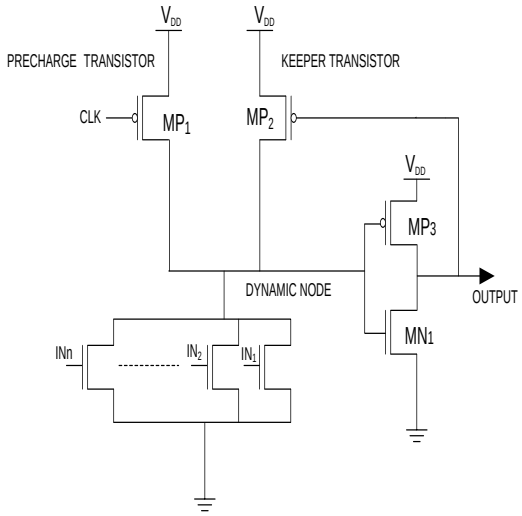

Fig.1 Standard Footer less Domino Logic Circuit

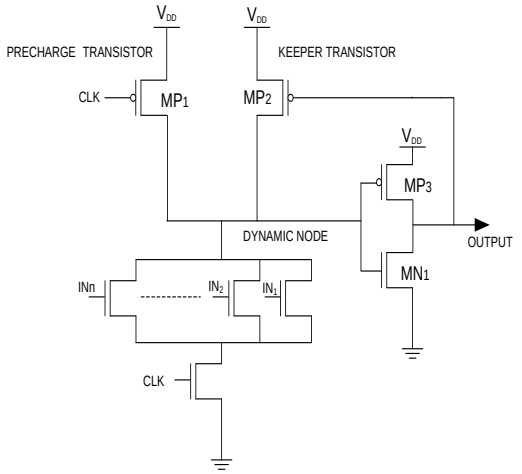

Fig.2 Standard Footed Domino logic circuit

(b) Conditional Keeper Domino Logic

Now considering the another efficient technique that is Conditional Keeper Domino Logic (CKDL) which is shown in figure 2 that make use of two keeper transistors [9]. One of the two keeper transistors is weaker one (K1) and other one is stronger (K2) as shown in Fig.2. In the working, initially K1 is on during the starting of evaluation phase for maintaining the state of dynamic node. If the state of dynamic node being retained high after the delay for inverters, then that will make the stronger keeper K2 to be turned on. This method results in the reduction of contention and also improves noise immunity. Noise characteristics can further be reduced by the sizing of delay elements but this will give rise to the higher power dissipation. And area overhead is also one disadvantage due to NAND gate for CKDL [7].

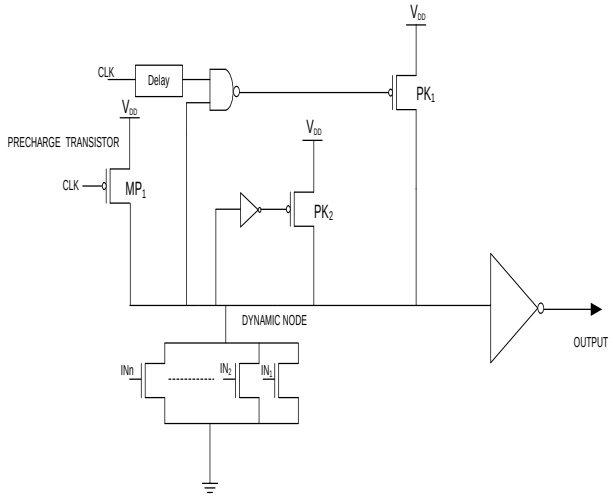

Fig. 3 Conditional Keeper Domino Logic

(c) High Speed Domino Logic

High speed domino logic is another configuration shown in figure 3. The working of this domino logic results in the reduction of the contention between the keeper transistor and the evaluation network with a use of clock delay as shown in Fig.4. As comparison to the CKDL technique it makes use of only strong keeper and eliminates the weaker one so as to enhancing speed. This keeper transistor remains off at the starting of the evaluation phase which results in the current reduction, but at the cost of power consumption, area overhead and lower noise immunity due to the float dynamic node [10].

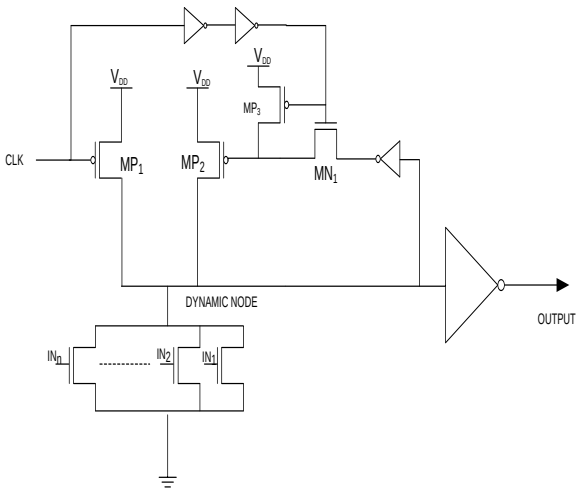

Fig.4 High-Speed Domino Logic

(d) Diode Footed Domino Logic

Diode footed domino logic is another technique presented in [11]. Customization to the standard domino circuit has been done by adding NMOS transistor in a diode configuration in series with the evaluation network as shown in Fig.5. This diode footer (M1) results in the sub threshold leakage reduction due to the stacking effect [12]. But there is performance degradation due to the diode footer that's why mirror transistor [M2] is employed to increase the performance characteristic.

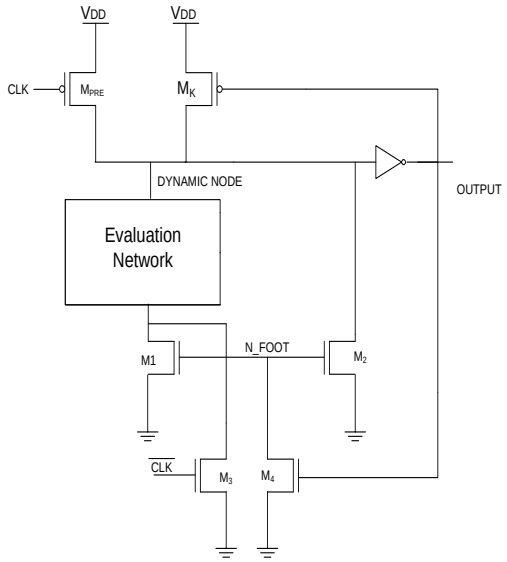

Fig.5 Diode Footed Domino Logic

III. PERFORMANCE COMPARISON OF PRESENTED METHODS

Simulations are performed in 90nm and 65 nm technology at 100MHz frequency and V_{DD} of 1V and 0.9V. The fall/rise times of the waveforms were set to 1pS. Considering the application of wide OR gates delay, power dissipation and UNG (Unit Noise Gain) has been calculated for 8 input and 16 input OR gate to compare different topologies. Fig.6 provides proper logic of footed domino logic circuit. For calculation of UNG [11], a pulse noise is applied to all inputs with amplitude which is a fraction of supply voltage and a pulse width equal to 30% of duty cycle. Then, the amplitude of the input noise pulse is increased until the amplitude of the resulting output noise voltage is equal to that of the input noise signal. This noise amplitude is defined as

UNG = {Vin : Vnoise = Voutput}

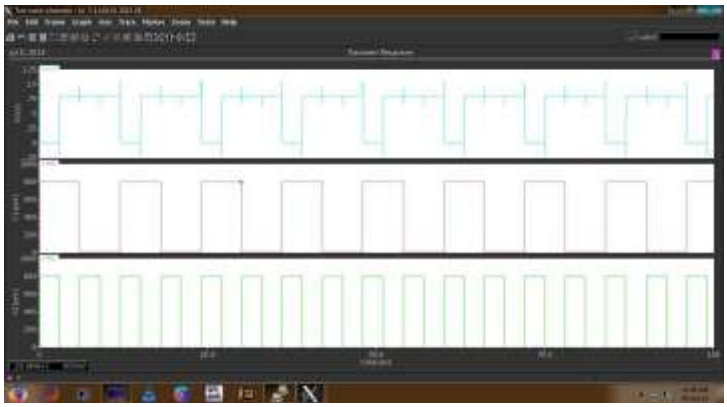

Fig 6. Output waveform of Footed Domino Logic

Table. I. Simulation is done with V_{dd}=1v, Frequency is 100MHz, For 8 Input OR Gate at 90nm Process Technology

Parameters	FLD	FD	HSD	CKD	DFD	LCR	CCD
Power (µW)	2.203	2.964	375.49	205.52	3.320	2.259	1.98
Normalized power	1	1.34	170.4	93.29	1.50	1.025	0.9
Propagation delay (ps)	16.55	29.615	16.152	19.05	27.88	16.91	18.13
Normalized propagation delay	1	1.78	0.97	1.15	1.68	1.02	1.09
Power delay product (aJ)	36.45	87.64	6064.1	3915.1	92.56	38.19	35.89
UNG	0.398	0.427	0.3962	0.4079	0.429	0.4441	0.493
Normalized UNG	1	1.072	0.995	1.024	1.077	1.115	1.23
No. of Transistors	12	13	18	23	16	14	23

Table. II. Simulation is done with V_{dd}=0.9v, Frequency is 100MHz, For 8 Input OR Gate at 65nm Process Technology

Parameters	FLD	FD	HSD	CKD	DFD	LCR	CCD
Power (µW)	1.809	2.201	276.53	137.32	2.647	1.882	1.648
Normalized power	1	1.21	152.86	75.90	1.46	1.04	0.911
Propagation delay (ps)	14.96	25.46	14.655	16.81	24.83	15.05	16.65
Normalized propagation delay	1	1.70	0.979	1.12	1.65	1.06	1.11
Power delay product (aJ)	27.06	56.03	4044.7	2303.9	65.72	28.32	27.43
UNG	0.298	0.327	0.3062	0.3179	0.331	0.310	0.361
Normalized UNG	1	1.097	1.027	1.066	1.110	1.040	1.211
No. of transistors	12	13	18	23	16	14	23

IV. CONCLUSION

In this paper, several domino logic circuit topologies were proposed for high-speed and leakage-tolerant design. High speed clock delayed (HSCD) domino method has the best performance among others. From the simulation result we can conclude that power dissipation of the Diode Footed Domino is minimum due to the stacking effect and body biasing of the NMOS exponentially while the speed is degraded because of the increase in switching threshold voltage. On the other hand this increased threshold voltage improves the noise immunity. Thus UNG of DFD logic is higher than the other domino logic. Leakage Current Replica shows best result in term of speed as compared to other logic. In modern VLSI, a bit of improvement in any parameter plays an important role. So this paper can proves to be useful because it gives a remarkable improvement in the field of delay, power, noise immunity and area when the proposed circuit is compared with other domino logic circuits. The whole simulation and comparison is based upon 65nm CMOS technology using Cadence Virtuoso.

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