# Fuzzy Controlled Capacitor Voltage Balancing Control for a Three Level Boost Converter

Neethu Rajan<sup>1</sup>, Dhivya Haridas<sup>2</sup>, Thanuja Mary Abraham<sup>3</sup>

<sup>1</sup>M.Tech student, Electrical and Electronics Engineering, Mahatma Gandhi University, India <sup>2</sup>Assistant Professor, Electrical and Electronics Engineering, Mahatma Gandhi University, India <sup>3</sup>Assistant Professor, Electrical and Electronics Engineering, Mahatma Gandhi University, India

Abstract— A three-level boost converter uses a smaller inductor and lower voltage devices than the conventional boost converter. It has two capacitors connected in series across the output which leads to voltage imbalance problem due to mismatched capacitances. If not balanced, one of the capacitor voltages may be larger than the breakdown voltage of the switch, which would contribute to make damage to the switch. In this work the capacitor voltage imbalance problem has been studied for a three level boost converter. This capacitor voltage is balanced by the adopted control strategy by sensing the voltage across the two capacitors. The simulation of the voltage imbalance mitigation strategy is done by MATLAB/ Simulink.

**Keywords-** *Power factor correction, Voltage imbalance* 

## I. INTRODUCTION

Recently, a single-phase unidirectional acto-dc rectifier with boost topology has been widely used as a front-end due to its good performance characteristics, as compared with thyristor rectifiers and diode rectifiers. It posses high power factor, low current harmonic distortion[2],[3], and small filter requirement. The boost topology has properties of step-up voltage ratio, simple control, and continuous input current. For high-voltage applications [4], the power devices with high voltage stress are generally required. A three phase three-level rectifier could reduce the voltage stress and power losses on the power devices.

In the traditional two-level boost topology, the output voltage is usually controlled dc when the input voltage is ac. If the input voltage increases or a higher output voltage is expected, the output voltage will increase accordingly, which means the power switches should withstand a higher voltage stress than the actual. It will result in the increase of the switching loss and conducting loss. The selection of power switches become difficult since the MOSFET with a high rated voltage is of shortage and expensive. A conventional single-phase three-level rectifier requires eight power switches and 12 power switches for a three-phase rectifier to perform bidirectional power flow. The drawback of this topology is a large number of power devices. If only unidirectional power flow is required, the number of power devices can be reduced significantly.

For the conventional boost converter, the single switch needs to withstand the dc output voltage when the single switch blocks. The two cascaded switches and two cascaded capacitors are connected together in the three-level boosting dc/dc converter. When one of the switches conducts and the other blocks, the blocking switch needs to withstand only half dc output voltage if both capacitor voltages are balanced. If not balanced, one of the capacitor voltages may be larger than the breakdown voltage of the switch, which would contribute to make damage to the switch. So various control strategies which could compensate the voltage imbalance by using a voltage balancing control loop could be found in [7],[11],[12],.

It is noted that the inductor voltage in the three-level boost dc/dc converter has three levels, which makes the three-level boosting dc/dc converter to have smaller inductor current ripple than the boost converter under the same switching frequency. Therefore, the three-level boost converters are often used in the high-voltage-ratio applications [4], such as the fuel cell applications [5], [6] and the grid-connected applications [7]–[9].

A three level boosting converter could be used for PFC if ac voltage is applied as the input and if a rectifier is provided in the input section [9]-[13]. This single phase three-level circuit based on the three-level boost topology provides a good solution for a single phase PFC[16] operating under high voltage and high frequency conditions. The various control strategies adopted should find a solution for both PFC as well as capacitor voltage balancing [1].

In [11] a control scheme for a single-phase ac-to-dc converter with three-level pulse width modulation was done. A single-phase power-factorcorrection circuit was adopted which could improve the power quality. The hysteresis current control technique for a diode bridge with two power switches is adopted to achieve a high power factor and low harmonic distortion. A control scheme was introduced where the line current is driven to follow the reference sinusoidal current which is derived from the dc-link voltage regulator, the capacitor voltage balance compensator, and the output power estimator.

Voltage balance issue of dc-link capacitors is important for applications of a cascade multilevel converter [14] or a modular multilevel converter. In [15], a novel diode-clamped modular multilevel converter topology was adopted and a power feedback control method was developed. With the developed control strategy, the diode-clamped circuit becomes a controllable closed loop which enables the capacitor voltages to be clamped by low power rating clamping diodes.

The circuit operation modes and the two capacitor voltage balancing strategies are described in section II. The section III includes the simulation analysis and section IV presents the experimental results to verify the theory. Sections V include the conclusion.

## II. THREE LEVEL BOOST CONVERTER



Fig. 1. Three level boost converter

A three level boosting converter is shown in fig. 1. It consists of two switches SW1 and SW2 and two switches can be operating at the same time without concern of short circuit. With these two switches there are two four operating states for this converter. As shown in fig. 2(a), both switches turn ON in the switching state1. Thus, the inductor voltage  $V_L$  in the three-level boosting PFC converter equals the rectified input voltage  $V_L = |V_S|$  and both capacitors supply energy to the load.

In the switching state2 in fig. 2(b), the top switch turns ON and the bottom switch turns OFF. The resulting inductor voltage  $V_L$  equals the rectified input voltage  $|V_S|$  minus the bottom capacitor voltage,  $V_L = |V_S| - V_{C2}$ . Additionally, the capacitor C1 supplies energy to the load but the capacitor C2 stores the energy from the input voltage.

The switching state3 is shown in fig. 2(c). Here the resulting inductor voltage in equals the rectified input voltage minus the top capacitor voltage  $V_L = |V_S| - V_{C1}$ . In this state the top capacitor C1 is charged but the bottom capacitor C2 is discharged.

The switching state4 is shown in fig. 2(d). When both switches turned OFF the resulting inductor voltage equals the rectified input voltage minus the output voltage  $V_L = |V_S| - V_d = |V_S| - V_{C1}$ -  $V_{C2}$ . The rectified input voltage  $|V_S|$  supplies the load current and charges both capacitors simultaneously.



Fig. 2. Switching states of a three level boost converter (a) state1circuit (b) state2 circuit (c) State3 circuit (d) state4 circuit



Fig. 3. Behavior of the three-level boosting converter. (a) 2>Vcont1+Vcont2>1 and (b) 1>Vcont1+Vcont2>0

The behaviour of the three-level boosting converter can be divided into two cases as shown in fig. 3. In the case of  $2 > V_{cont1} + V_{cont2} > 1$ , two switches may conduct at the same time within the switching period Ts and there are switching state 1, state 2, and state 3. In the other case of  $1 > V_{cont1} + V_{cont1}$  $V_{cont2} > 0$ , only switching state 2, state 3, and state 4 exist. In the case of  $2 > V_{cont1} + V_{cont2} > 1$  in fig. 3(a), the conducting times of the switching state 2 and the switching state 3 are  $(1 - V_{cont2})$ Ts and  $(1 - V_{cont2})$ Ts and (1 - VV<sub>cont1</sub>)Ts, respectively. The remaining time for the switching state 1 is  $(V_{cont1} + V_{cont2} - 1)Ts$ . Similarly, for the other case of  $1 > V_{\text{cont}1} + V_{\text{cont}2} > 0$  in fig. 3(b), the conducting times of the switching state 2 and state 3 are  $V_{cont1}Ts$  and  $V_{cont2}Ts$  , respectively. The remaining time for the switching state 4 is (1 - $V_{cont1} - V_{cont2}$ )Ts.

The mismatched capacitance and equivalent series resistance would result in voltage imbalance across the two capacitors. This voltage imbalance should be detected and is mitigated by using a control strategy which senses the voltage across two capacitors as is shown in fig. 4.



Fig. 4 .Three level boost converter control strategy by sensing the voltage across the two capacitor.

The ac input voltage is applied to the diode rectifier and thus the input voltage of the three-level boosting converter can be expressed with the rectified voltage |Vs |. By assuming that the switching frequency fs is much larger than the line frequency f, the control signals  $V_{\text{cont1}}$  and  $V_{\text{cont2}}$  can be regarded as two constants within the switching period Ts = 1/fs. Also inductor and capacitors are assumed to be ideal which means that the the inductor resistance and the capacitor resistances are assumed to be zero. In fig. 3, two triangular signals V<sub>tri1</sub> and V<sub>tri2</sub> are interleaved by 180°. The multiloop control generates the control signal V<sub>cont1</sub>, and then, the gate signal GT1 is generated from the comparison of the control signal  $V_{\mbox{\scriptsize contl}}$  and the triangular signal V<sub>tri1</sub>. The voltage imbalance is detected by sensing the voltage across two capacitors the compensation signal  $\Delta V_{cont}$  is generated. Then, the other control signal  $V_{\text{cont2}}\xspace$  is obtained by adding the compensation signal  $\Delta V_{cont}$ to the control signal  $V_{cont1}$ . The gate signal GT2 is obtained from the comparison of the control signal  $V_{cont2}$  and the triangular signals  $V_{tri2}$ .

## III. SIMULATION AND RESULTS

The simulation of the proposed method is done in MATLAB2010. The focus was on the output voltage and the voltage across the two capacitors. The switching frequency is taken as 20kHz. The ac input voltage applied to the circuit is 110V. The values of two capacitors C1 and C2 are 2240 $\mu$ F and 1510 $\mu$ F and that of inductor is 0.5mH. The value of load resistance is taken as 150 $\Omega$ .



Fig. 5. Simulation model by sensing the capacitor voltages

The controlling is done by using fuzzy. The simulink model of the circuit using fuzzy controller is shown in fig. 5. The dc output voltage is obtained as 300V. Also the voltage across the both the capacitors are 150V which proves that the voltages are balanced.. The power factor measured is 0.99. The simulated waveforms of output voltage and capacitor voltages are shown in fig. 6(a),fig. 6(b) and fig. 6(c) respectively.



Fig. 6.(a) Output voltage (b) Voltage across capacitor C1(c) Voltage across capacitor C2.

### IV. EXPERIMENTAL RESULTS

The system is implemented by using dsPIC30f2010 controller. The nominal parameters are shown in table I. Four ADC channels are used to sense the input voltage, output voltage, capacitor voltage and another one to provide the desired

reference voltage. In the input section the applied 230V input voltage is stepped down to 12V by using a 230/12V step down transformer. The output voltage is regulated at 28V. The experimental setup and output voltage waveform are shown in fig. 7(a) and fig. 7(b) respectively. The capacitor voltages are measured to be 14V which proves that the voltages are balanced. The waveform of capacitor voltages are shown in fig. 8(a) and fig. 8(b) respectively. The capacitors have different value of ripple voltage due to mismatched capacitances but their average value is almost same. The proposed system is developed based on the assumptions of ideal inductor and ideal capacitors.

Table I: Hardware parameters of a three level boost converter

Input voltage	12V, 50Hz
Output voltage	28V
Carrier frequency	20kHz
Inductor	.8mH
Capacitor	1000µF and 2000µF





(b)

Fig. 7.(a) Experimental setup of the proposed system (b) Output voltage





(b)

Fig. 8.(a) Voltage across capacitor C1 (b) Voltage across capacitor C2S  $\ensuremath{\mathsf{C2S}}$ 

#### V. CONCLUSION

A three level boost converter often used in high voltage ratio applications is studied here. It has two series connected capacitors in the output section which may have voltage imbalance problem due to mismatched capacitance and equivalent series resistance. A control strategy is adopted to compensate this imbalance by sensing the capacitor voltages. This particular voltage balancing control method is discussed. The simulation was done by using MATLAB/Simulink. The simulation was done by using a fuzzy logic controller. The hardware is implemented for the same and all provided results demonstrate the method. In addition, the proposed voltage balancing control loop can be extended to other circuits which needs to avoid voltage imbalance.

#### REFERENCES

- Hung-Chi Chen and Jhen-Yu Liao, "Design and implementation of sensorles capacitor voltage balancing control for three level boosting PFC," IEEE Trans. Power Electron., vol. 29, no. 7, pp. 3808–38177, Jul. 2014.
- [2] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003..
- [3] J. C. Crebier, B. Revol, and J. P. Ferrieux, "Boost-chopperderived PFC rectifiers: Interest and reality," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 36–45, Feb. 2005.
- [4] L. S. Yang, T. J. Liang, H. C. Lee, and J. F. Chen, "Novel high step-up DC–DC converter with coupled-inductor and voltage-doubler circuits," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4196–4206, Sep. 2011.
- [5] A. Shahin, M. Hinaje, J. P. Martin, S. Pierfederici, S. Rael, and B. Davat, "High voltage ratio DC–DC converter for fuel-cell applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 3944–3955, Dec. 2010.
- [6] M. H. Todorovic, L. Palma, and P. N. Enjeti, "Design of a wide input range DC–DC converter with a robust power control scheme suitable for fuel cell power conversion," IEEE Trans. Ind. Electron., vol. 55, no. 3, pp. 1247–1255, Mar. 2008.
- [7] Y.-S. Lee and Y.-P. Ko, "Switched-capacitor bi-directional converter performance comparison with and without quasiresonant zero-current switching," *IET Power Electron.*, vol. 3, no. 2, pp. 269–278, Mar. 2010..
- [9] M. T. Zhang, Y. Jiang, F. C. Lee, and M. M. Jovanovic, "Single-phase three-level boost power factor correction converter," in *IEEE App. Power Electron. Conf.*, 1995, pp. 434–439.
- [10] J. R. Pinheiro, D. L. R. Vidor, and H. A. Grundling, "Dual output threelevel boost power factor correction converter with unbalanced loads," in *Proc. IEEE Power Electron. Spec. Conf.*, 1996, pp. 733–739. [11] B. R. Lin and H. H. Lu, "A novel PWM scheme for single-phase threelevel power-factor-correction circuit," *IEEE Trans. Ind. Electron.*, vol. 47, no. 2, pp. 245–252, Apr. 2000.
- [12] H.Wu and X. He, "Single phase three-level power factor correction circuit with passive lossless snubber," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 946–953, Nov. 2002.
- [13] J. Y. Liao and H. C. Chen, "Multiloop interleaved control for two-switch two-capacitor three-level SMR without capacitor voltage balancing loop," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 3766–3772.
- [14] R. Greul, S. D. Round, and J. W. Kolar, "The Delta-Rectifier: Analysis, Control and Operation," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1637–1648, Nov. 2006.
- [15] E. Ribeiro, A. J. M. Cardoso, and C.Boccaletti, "Faulttolerant strategy for a photovoltaic DC–DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 3008– 3018, Jun. 2013.
- [16] K. Deepak Singh and Manish G Rathi," Implementation of Three Level Integrated AC-DC Converter with Pulse Width Modulation," *IJETT.*, vol. 12, no. 6, pp. 268–273, Jun. 2014.