Performance Evaluation for GSM Receiver Using Software Defined Radio

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***Abstract*—** *Software Defined Radio (SDR) is a flexible radio architecture which can be configured to adapt various waveforms, frequency bands, bandwidths, modes of operations and wireless standards such as Global System of Mobile communications (GSM) by altering the physical layer behavior through changes in its software. In this paper, The baseband section of GSM wireless receiver which includes Source Decoding, Channel Decoding, De-interleaver, Demodulation and Frequency De-hopping (FH) has been tested, simulated and designed for implementation using SDR. And the Bit Error Rates (BER) has been calculated for different modulation schemes namely, Binary Frequency Shift Keying (BFSK), Binary Phase Shift Keying (BPSK), and Quadrature Phase Shift Keying (QPSK), and Eight Phase Shift Keying (8PSK). These four models have been evaluated considering an additive white Gaussian noise channel (AWGN). Then the performance of the receiver has been analyzed by comparing the input and output waveforms with /without FH. Finally a comparison of the simulation results is presented and discussed.*

Keywords — *SDR, GSM, FH, BER, AWGN.*

I. Introduction

Wireless communication networks have become more popular in the past two decades since the advent of cellular communications. The rapid growth in cellular communications has proved that wireless communication is viable for voice and data services as well. Traditional wireless devices are designed to deliver a single communication service using a particular standard [1]. With the huge demand of new wireless services and applications, the traditional single purpose devices with dedicated hardware resources can no longer meet the user's needs. It is also expensive to upgrade and maintain a wireless system each time a new standard has been formulated. The SDR concept has become a feasible solution to make communication systems more flexible and user friendly . SDR refers to the class of reconfigurable or reprogrammable radio devices in which the same platform of hardware can perform different functions at different times [2]. SDR technology can be used to take advantage of reconfigurable hardware modules to build open system platform based on software. In this case, a variety of transceiver functions such as automatic gain control, frequency translation, filtering, modulation and demodulation can be integrated on a single hardware platform. This could result in maximizing the number of radio functions for a particular application. SDR offers the flexibility and upgradeability necessary to meet these requirements [3].

Here GSM has been chosen as wireless communication networks to design a SDR platform. GSM is a world-wide standard for digital wireless mobile telephones, currently used by 4.4 billion [4] people. It is developed to make use of same subscriber units or mobile phone terminals throughout the world. There are various GSM standards such as GSM900, EGSM900, GSM1800 and GSM 1900; they mainly differ based on RF carrier frequency band and bandwidth. The GSM-900 system is considered in this paper.

In this work GSM receiver using SDR has been analyzed, and simulated using MATLAB. First, the model is simulated as shown in Fig. 1 which includes the baseband section of a GSM communication system with several demodulation techniques, such as BFSK, BPSK, and (MPSK) to achieve a data rate of 2Mbps.

The rest of this paper is organized as follow; Section II presents an overview for the system description. The GSM receiver Simulation is presented in Section III. Then simulation results according to bit error calculations are discussed in Section IV. Finally, the conclusions are summarized in Section V.

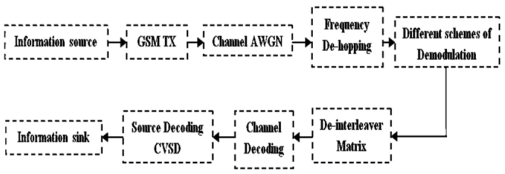

Fig. 1 Design Model.

II. System Description

GSM Physical Layer is shown in Fig. 2 after converting the analog speech signals into digital bits, the raw source bits are coded according to the model of human speech to reduce the bits needed

to be transmitted. Depending on the relative importance of the bits this called Speech Coding which using the Rectangular Pulse Excited Linear Predictable coding with Long Term Prediction (RPE-LTP) technique as in GSM 06-10 specification. Hence the channel coding function arranges that bits into blocks and adds some error correction codes. The encoded bits are then applied to interleaver. This interleaver shuffles the bit positions in the blocks to provide some time-diversity in fading channels. The interleaved bit blocks are assembled with some training bits, and control bits to form normal speech GSM bursts, which are modulated by GMSK modulation technique before sending to RF amplifier and antenna. The process in the receiver side is the reverse of the transmitter. Moreover, according to the channel which is not perfect, there always exists degradation of signal by noise, fading, Doppler shifting, etc., so some sort of channel equalization and noise filtering is needed to recover the original signals. Now we will going to explain our model design .

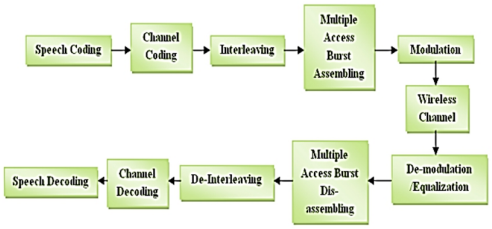

Fig. 2 GSM Physical Layer.

A. Source Decoding

Speech coder maps speech into digital blocks. Coder used in GSM compresses the speech signal to 13 kbps rate using the Rectangular Pulse Excited Linear Predictable coding with Long Term Prediction (RPE-LTP) technique. This algorithm produces a speech block of 260 bits every 20 ms.

Adaptive Delta Modulation (ADM) which called 1-bit Continuously Variable Slope Delta-Modulation (CVSD) [5], [6] has been considered as a simple technique to overcome delta modulation (DM) [7] drawbacks. CVSD has an adaptive step-size. By adjusting the step-size to the changes in slope of the input signal, the encoder is able to represent low-frequency signals with greater accuracy without sacrificing much performance due to slope-overload at higher frequencies. This data stream, usually the computer error signal, is a lower-bit-rate signal that can be decoded by a matched decoder on the receiver side and thus achieves data compression resulting in low data transmission rates as in GSM speech coding technique we need output data rate 13Kbps, so a 1-bit CVSD has been designed with data rate 13 kbps for speech coding and decoding [8].

As shown in Fig. 3 CVSD decoder in which a slope-overload detector and syllabic filter are used in conjunction with a Pulse Amplitude Modulator (PAM) to accomplish the step-size adaption. The decoder performs the inverse function of the encoder and regenerates speech by passing the analog output signal of the reconstruction integrator through the low-pass filter.

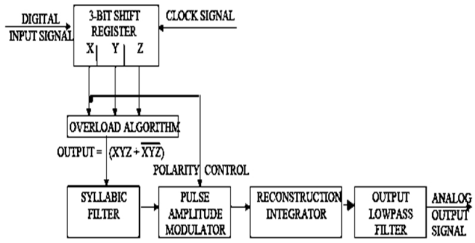

Fig.3 CVSD Decoder.

Other characteristics optimize the CVSD modulation technique for voice signals. First, Changes in the slope of the analog input signal determine the step-size changes of the digital output signal. Also the feedback loop is adaptive to continuous or smoothly incremental changes in step size. And companding is performed at a syllabic rate to extend the dynamic range of the analog input signal. Finally, the reconstruction integrator is of the exponential type to reduce the effects of digital errors.

B. Channel Decoding

Channel coding introduces redundancy into the data flow in order to allow the detection or even the correction of bit errors introduced during the transmission [9]. The speech coding algorithm produces a speech block of 260 bits every 20 ms (i.e. bit rate 13 Kbps). In the decoder, these speech blocks are decoded and converted to 13 bit uniformly coded speech samples. The 260 bits of the speech block are classified into two groups. The 78 Class II bits are considered of less importance and are unprotected. The 182 Class I bits are split into 50 Class Ia bits and 132 Class Ib bits as shown Fig. 4. Class Ia bits are first protected by 3 parity bits for error detection. Class Ib bits are then added together with 4 tail bits before applying the convolutional code with rate r = ½ and constraint length K=5.The resulting 378 bits are then added to the 78 unprotected Class II bits resulting in a complete coded speech frame of 456 bits .

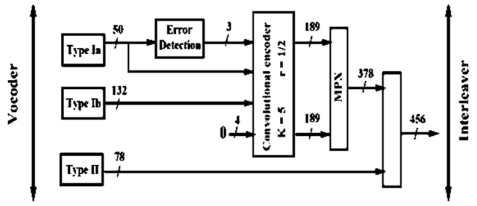

Fig. 4 Channel Coding in GSM.

1) ***Error Detecting Codes*:** The overall idea of the block code is to generate some certain redundant code from a data stream and transmit both redundant code and the data stream for error correction. If the redundant code is carefully designed and the channel noise power is acceptable, the receiver of the data can probably detect a corrupted data stream or even correct the error. Block code has many subclasses like rectangular code, Reed Solomon code and cyclic code. Here a cyclic code is involved in the design. A typical decoder is shown in the Fig. 5. The decoder at the receiving side is also a modulo division circuit.

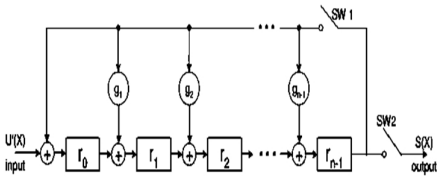

Fig. 5 Systematic n-stage Cyclic Decoder.

2) ***Convolutional Decoding:*** The convolutional coding gives the protection to every bit of transmitted data. So the decoding circuit is very expensive. Furthermore, the bandwidth requirements of the channel and the decoding circuit are sometimes increased several times. There are three well known decoding techniques for convolutional coding: the Viterbi algorithm, the sequential decoding and the feedback decoding. Sequential decoder's complexity is independent of constraint length K (K could be 41), thus can achieve very good error protection. But the main drawback of the sequential decoding is the requirement of a large buffer memory. Also the time needed for the decoding process is random. Feedback algorithm could only be used for hard-decision bit, which is not suitable for the targeting application.

As a maximum likelihood decoding as shown in Fig. 6, Viterbi algorithm is the most used algorithm for low constraint length codes. Since the decoding complexity grows exponentially as K increases, the Viterbi algorithm is scarcely used if K is larger than 13 [10], [11]. The GSM standard mostly uses low constraint length code like 5 and 7, thus makes the Viterbi algorithm a good choice. In this paper constraint length K=5 has been used. The data is decoded with convolutional decoder then it is decoded with a block decoder.

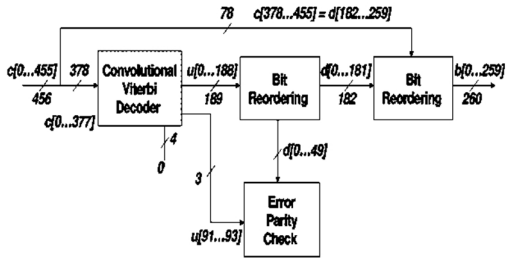

Fig. 6 GSM Channel Decoding.

C. *De-interleaving*

Interleaving is a technique which prevents burst of errors during the transmission. The convolutional coding offers correction probability for a few bits' error, but if the channel is interfered for a short moment so that several consecutive transmitted bits are contaminated, the convolutional coding will be of little help. A simple way to make better use of the convolutional coding is to reorder the encoder output so that the data are transmitted out of order. At the receiver side, the received bit sequence is rearranged into the correct order before convolutional decode starts. If there are burst errors in the channel, the erroneous bits will be distributed into many places among other correct bits so that the convolutional decoder will have better chances to correct the error. Such a reordering technique is called interleaving. The interleaving is often used in the GSM standard, GSM blocks of full rate speech are interleaved on 8 bursts: the 456 bits of one block are split into 8 bursts in sub-blocks of 57 bits each.

A sub-block is defined as either the odd- or the even-numbered bits of the coded data within one burst. Each sub-blocks of 57 bit is carried by a different burst and in a different TDMA frame. So, a burst contains the contribution of two successive speech blocks A and B. In order to destroy the proximity relations between successive bits, bits of block A use the even positions inside the burst and bits of block B, the odd positions as shown in Fig. 7. De-interleaving consists in performing the reverse operation.

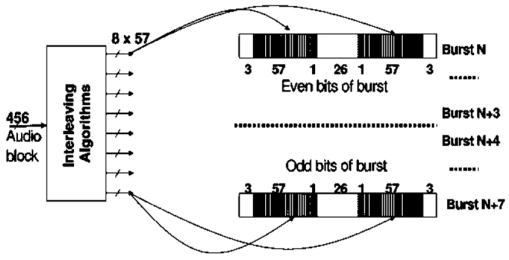

Fig. 7 GSM Interleaving.

D. The Demodulator:

BFSK ,BPSK , QPSK and 8PSK Demodulator schemes have been used in our GSM system in the demodulator part. Each of them has its performance metric in terms of bit error (p_e) and signal to noise ratio $(\frac{E_b}{N_0})$

1) ***BFSK Demodulator:*** To detect the original binary sequence given the noisy received signal x(t), and the receiver as shown in Fig. 8.

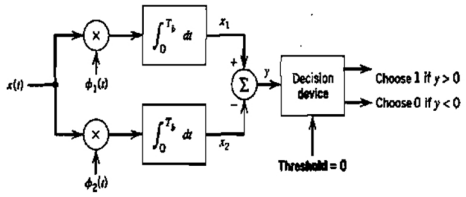

Fig. 8 BFSK Demodulator.

In a binary FSK system, symbols 1 and 0 are is described respectively by

$$s_i = \begin{cases} \sqrt{\frac{2E_b}{T_b}}\cos(2\pi f_i t), & 0 \le t \le T_b \\ 0, & \text{elsewhere} \end{cases} \quad (1)$$

Where i = 1, 2, and E_b is the transmitted signal energy per bit; the transmitted frequency is F_i

$$f_i = \frac{n_c + i}{T_b} \quad \text{for some fixed integer } n_c \quad (2)$$

From equations (1) and (2), the signals $S_1(t)$ and $S_2(t)$ are orthogonal, but not normalized to have unit energy. We therefore deduce that the most useful form for the set of orthonormal basis functions is

$$\emptyset_i(t) = \begin{cases} \sqrt{\frac{2}{T_b}}\cos(2\pi f_i t), & 0 \le t \le T_b \\ 0, & \text{elsewhere} \end{cases} \quad (3)$$

where *i* = 1, 2.

A coherent binary FSK system is characterized by having a signal space that is two-dimensional (i.e., N = 2) are defined by the

$$s_1 = \begin{bmatrix} \sqrt{E_b} \\ 0 \end{bmatrix} \quad (4)$$

And

$$s_2 = \begin{bmatrix} 0 \\ \sqrt{E_b} \end{bmatrix} \quad (5)$$

The bit error for coherent binary FSK is

$$p_e = \frac{1}{2}\text{erfc}\left(\sqrt{\frac{E_b}{2N_0}}\right) \quad (6)$$

2) ***BPSK Demodulator:*** To detect the original binary sequence of 1s and 0s, as shown in Fig. 9.

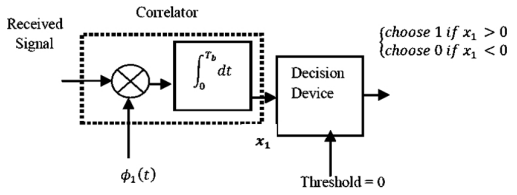

Fig. 9 BPSK Demodulator.

In coherent binary PSK system, the pair of signals $S_1(t)$and $S_2(t)$ used to represent binary symbols 1 and 0, respectively. They are defined by

$$s_1(t) = \sqrt{\frac{2E_b}{T_b}}\cos(2\pi f_c t) \quad (7)$$

$$s_2(t) = \sqrt{\frac{2E_b}{T_b}}\cos(2\pi f_c t + \pi) = -\sqrt{\frac{2E_b}{T_b}}\cos(2\pi f_c t) \quad (8)$$

Where $0 \le t \le T_b$, and E_b is the transmitted signal energy per bit. in the case of binary PSK, there is only one basis function of unit energy, namely,

$$\emptyset_1(t) = \sqrt{\frac{2}{T_b}}\cos(2\pi f_c t), \quad 0 \le t < T_b \quad (9)$$

A coherent binary PSK system has two coordinates of the message points

$$s_{11} = \int_0^{T_b} s_1(t)\,\emptyset_1(t)\,dt = \sqrt{E_b} \quad (10)$$

And

$$s_{21} = \int_0^{T_b} s_2(t)\,\emptyset_1(t)\,dt = -\sqrt{E_b} \quad (11)$$

The bit error rate for coherent binary PSK is

$$p_e = \frac{1}{2}\text{erfc}\left(\sqrt{\frac{E_b}{N_0}}\right) \quad (12)$$

3) ***QPSK Demodulator:*** In quadriphase-shift keying (QPSK), as with binary PSK, information carried by the transmitted signal is contained in the phase [12].

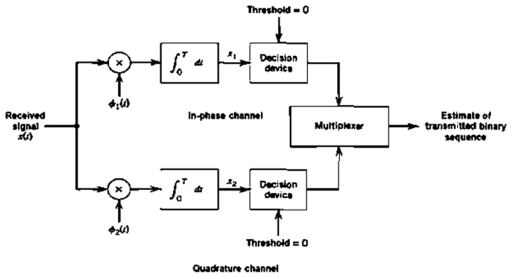

Fig. 10 QPSK Demodulator.

In quadriphase-shift keying, the phase of the carrier takes on one of four equally spaced values . Then the transmitted signal is defined as

$$s_i(t) = \begin{cases} \sqrt{\frac{2E}{T}} \cos\left[2\pi f_C t + (2i-1)\frac{\pi}{4}\right], \\ 0, \qquad \text{elsewhere} \end{cases} \quad 0 \le t \le T \qquad (13)$$

Where i = 1, 2, 3, 4; E is the transmitted signal energy per symbol, and T is the symbol duration. Each possible value of the phase corresponds to a unique dibit. There are two orthonormal basis functions, $\phi_1(t)$ and $\phi_2(t)$ as shown in Fig. 10, which defined by a pair of quadrature carriers:

$$\emptyset_1(t) = \sqrt{\frac{2}{T}}\cos(2\pi f_c t), \qquad 0 \le t \le T \qquad (14)$$

$$\emptyset_2(t) = \sqrt{\frac{2}{T}}\sin(2\pi f_c t), \qquad 0 \le t \le T \qquad (15)$$

There are four message points, and the associated signal vectors are defined by

$$s_i = \begin{bmatrix} \sqrt{E}\cos\left((2i-1)\frac{\pi}{4}\right) \\ -\sqrt{E}\sin\left((2i-1)\frac{\pi}{4}\right) \end{bmatrix}, \quad i = 1,2,3,4 \qquad (16)$$

The average probability of symbol error in terms of the ratio E_b/N_o, we may write

$$P_e = \text{erfc}\left(\sqrt{\frac{E_b}{No}}\right) \qquad (17)$$

With Gray encoding used for the incoming symbols, the bit error rate of QPSK is exactly

$$BER = \frac{1}{2}\text{erfc}\left(\sqrt{\frac{E_b}{No}}\right) \qquad (18)$$

From this equation a coherent QPSK system achieves the same average probability of bit error as a coherent binary PSK system for the same bit rate and the same E_b/N_o but uses only half the channel bandwidth. For a prescribed performance, QPSK uses channel bandwidth better than binary PSK, which explains the preferred use of QPSK over binary PSK in practice.

4) ***MPSK Demodulator:*** The average probability of symbol error for coherent M-ary PSK is

$$P_e = \text{erfc}\left(\sqrt{\frac{E}{No}}\sin\left(\frac{\pi}{M}\right)\right) \qquad (19)$$

Also 8PSK has advantages of having higher data rate compare to BPSK. This is due to support of three bits per carrier in 8PSK compare to one bit per carrier in the case of BPSK.

E. Frequency Hopping Spread Spectrum

The Frequency Hopping Spread Spectrum (FHSS) transceiver as in Fig. 11 is designed to provide the secure communication. This system is very popular because it is a secure communication model which utilizes the Pseudo Random Noise (PN) Sequence as a carries signal and the communication channel used as Additive white Gaussian Noise (AWGN) Channel is preferred in this model then the Bit Error Rate is estimated to illustrate difference in performance with/without frequency hopping.

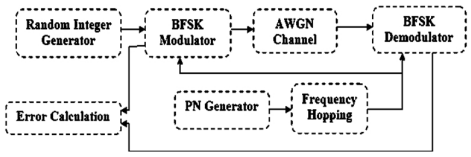

Fig. 11 Architecture of FHSS.

In modulator the baseband signal is combined with the hop frequency or carrier frequency generated by the frequency hopping block. The carrier frequency generated by this will be random since it is controlled by PN- sequence generator [13]. The modulated output will be sum of these two, which is spread over entire frequency band. At the receiver the demodulator gets the coded signal back from the spread spectrum signal as in Fig. 12. For this purpose the demodulator requires the same sequence which was used at the transmitting end. Hence the random sequence pattern generators at the transmitter and receiver side operate in synchronization with each other. The decoder at the receiver then gets the binary information sequence back after passing through AWGN channel [14].

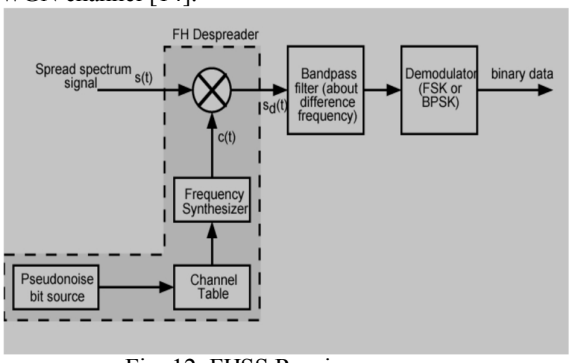

Fig. 12 FHSS Receiver.

III. MATLAB SIMULINK DESIGN IMPLANTATION

A. Simulation Implementation of CVSD Encoder/ Decoder

Fig. 12 shows the MATLAB / Simulink based implementation of 1-bit, 13 kbps CVSD speech encoder and decoder. The results are shown in Fig. 13; top plot is the encoded speech signal, second one is the original speech signal and a recovered speech signal, and finally last plot is the decoded speech signal.

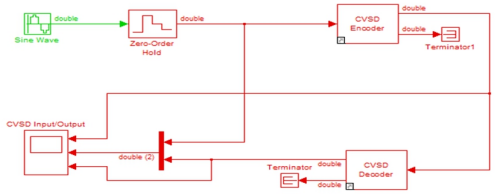

Fig. 13 Simulink based implementation of 1-bit CVSD Encoder and Decoder.

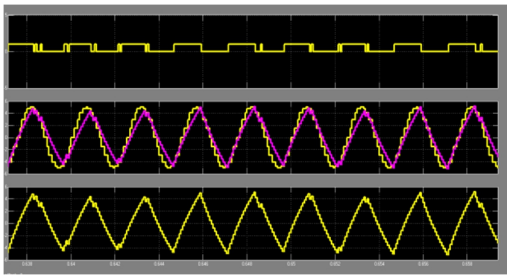

Fig. 14 Expanded form of encoded speech signal, Recovered speech and original speech signals, and Decoded speech signal.

B. Simulation Implementation of Channel Encoding/ Decoding

MATLAB / Simulink base implementation of channel coding and decoding are shown in Fig. 14. Channel Decoding design is shown in Fig. 15. Encode &decoded signals are shown in Fig. 16. The following parameters have been taken for Viterbi Decoder, k (constraint length)= 5,Trellis structure: poly2trellis(5, [33 23]),Traceback depth = 100, Decision type: hard decision.

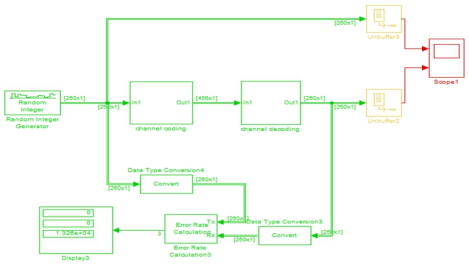

Fig. 15 Simulink based implementation of Channel Coding and Decoding.

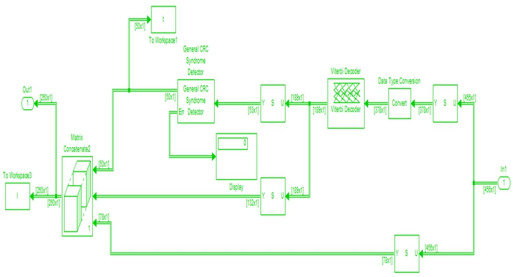

Fig. 16 Channel Decoding Design.

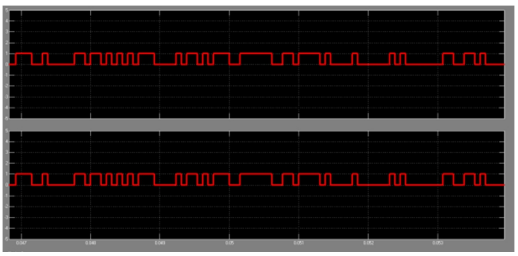

Fig. 17 Encoded & Decoded signals.

C. Simulation Implementation of Interleaving/ De-interleaving

MATLAB / Simulink based implementation of interleaver and de-interleaver is shown in Fig. 17. The signals before matrix interleaver and after matrix de-interleaver are shown in Fig. 18.

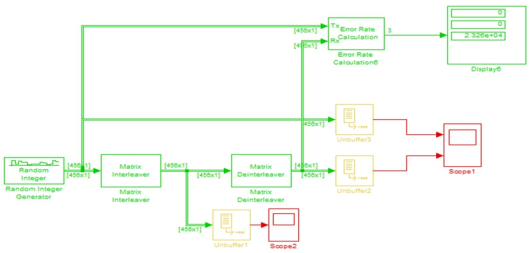

Fig. 18 Simulink based implementation of Interleaver and De-interleaver.

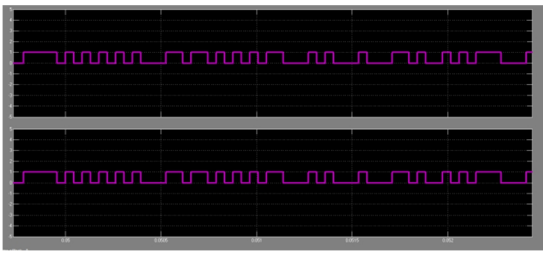

Fig. 19 The un-interleaved and de-interleaved signals.

D. Simulation Implementation of BFSK Modulator/ Demodulator

MATLAB / Simulink based implementation of BFSK modulator/ demodulator. First model BFSK baseband modulation has been implemented using

BFSK Baseband Modulator/Demodulator with values: "ΔF (frequency separation)= 57 KHz, Samples per symbol=10, i/p data rate=22.8Kbps" shown in Fig. 19. Second model BFSK passband demodulation has been implemented with values: "Fs (space frequency)=114Khz, Fm (mark frequency)=228Khz, i/p data rate=22.8Kbps" and the BFSK signal are shown in Fig. 20 and Fig. 21 respectively. The input signal and output signal from BFSK modulator/ demodulator are shown in Fig. 22.The BFSK spectrum is illustrated in Fig. 23.The two different models giving the same data rate 2Mbps.

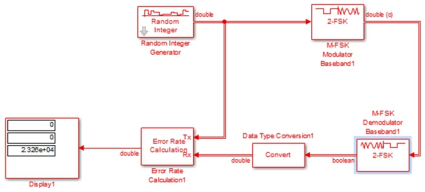

Fig. 20 BFSK Baseband Modulator/Demodulator.

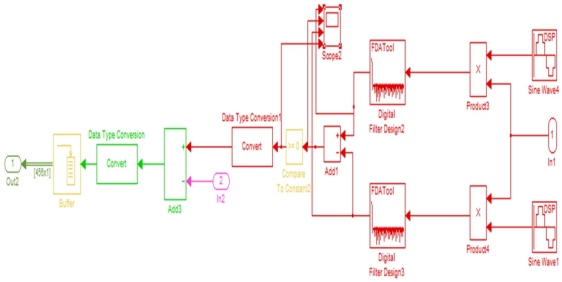

Fig. 21 BFSK Passband Demodulation.

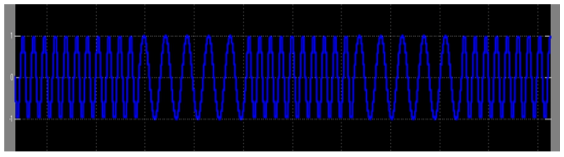

Fig. 22 BFSK Signal.

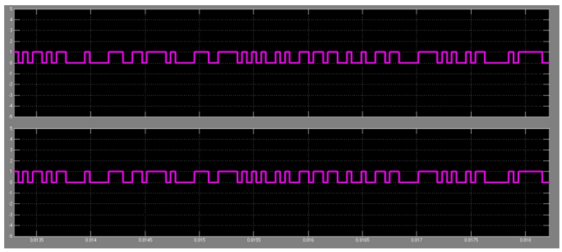

Fig. 23 The input signal and output signal from BFSK Modulator/ Demodulator.

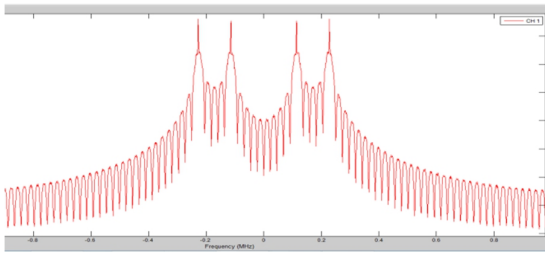

Fig. 24 BFSK Spectrum.

E. Simulation Implementation of different Demodulation schemes in AWGN Channel

A model for the simulation of binary FSK system in AWGN channel is shown in Fig. 24.

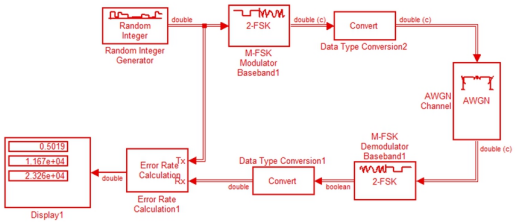

Fig. 25 Simulation model for BFSK system.

A model for the simulation of binary PSK system in AWGN channel is shown in Fig. 25.

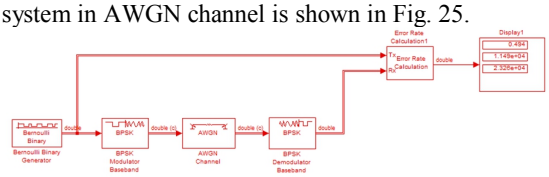

Fig. 26 Simulation model for BPSK system.

A model for the simulation of QPSK system in AWGN channel is shown in Fig. 26.

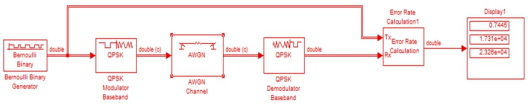

Fig. 27 Simulation model for QPSK system.

A model for the simulation of 8PSK system in AWGN channel is shown in Fig. 27.

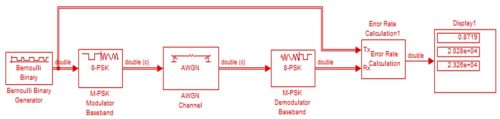

Fig. 28 Simulation model for 8PSK system.

F. Simulation Implementation of Frequency Hopping Spread Spectrum

The FHSS System simulink model is shown in Fig. 28, the input data is generated by using Random interger generator. The Random integer

generator generates the binary values. The binary values are modulated using BFSK which uses the carries as frequency hopping signal [15], then the signal is transmitted over Additive white Gaussian noise (AWGN) channel. And the transmitter output is obtained using FFT scope. At the receiver side the signal is demodulated using the same Frequency hopping signal .

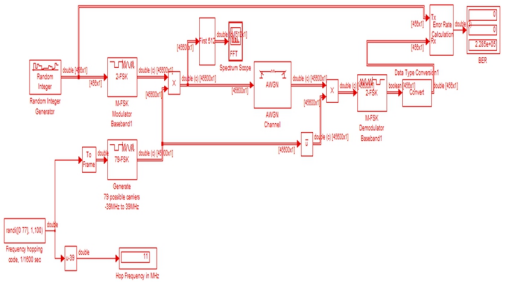

Fig. 29 Simulation Model for FHSS Transceiver System.

IV. SIMULATION RESULTS

The comparative analysis of simulated curves for BER vs. E_b/No (signal to noise ratio) for BFSK, BPSK and MPSK over AWGN channel are given in Fig. 29.

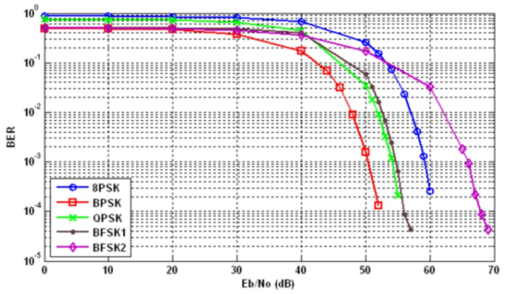

Fig. 30 Performance analysis of BFSK, BPSK, QPSK and MPSK over AWGN Channel using MATLAB Simulink.

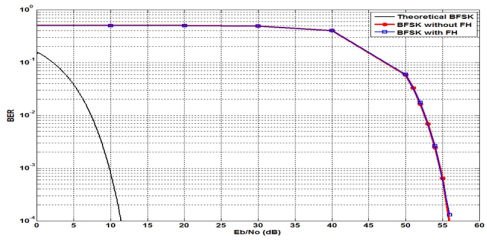

Fig. 31 Performance analysis of theoretical BFSK & simulated BFSK with/without FH.

V. CONCLUSIONS

The implementation of baseband section of GSM receiver which includes Source Decoding, Channel Decoding, De-interleaver has been shown in Fig. 13, 15, 16, 18, 20, and 21 using MATLAB/ Simulink. Moreover; Fig. 14, 17, 19, 22 and 23 shows the waveforms of input and the output of the GSM receiver sections.

Furthermore, The performance of our simulated GSM physical layer with AWGN channel is evaluated by means of the BER for different modulation schemes BFSK, BPSK, and QPSK, and 8PSK using models in Fig. 25, 26, 27 and 28. It has been proven by simulation results that BFSK model achieves the best performance under AWGN channel. While the 8PSK attains the highest data rate models as illustrated in Fig. 30. In addition, the SDR implementation of BFSK with FH has been shown in Fig. 29. The simulation result shows that applying FHSS with BFSK modulation does not affect the performance of BER as shown in Fig. 31 but FHSS provides protection against eavesdropping and jamming. These results will support our aim for improving the performance of GSM receiver using SDR technology by changing the modulation scheme according to the environmental conditions.

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