Oversampling Technique for Optimizing the Signal to Quantization Noise Ratio for A/D Converter

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Abstract
The circuits we are using in daily life are processing digital signals but the real world data or the data sensed by the sensor are analog in nature and there are very fewer sensors which are providing us the digital data which means the data conversion is very much important[8]. We know very well that whenever we are converting the analog data to the digital format we are going to take the samples of the analog signal and the accuracy of this conversion process is completely depend upon the number of samples and the number of bits of data that is taken of the analog signal[1]. During this transition, the error occurs in the original signal and reconstructed signal is known as quantization noise. This noise can be minimized by using more number of bits or by increasing the number of samples. The number of samples are enhanced by oversampling technique, which will directly increase the signal to noise ratio. In this paper, some graph are explaining the impoved signal to noise ratio in A/D by using oversampling technique[9].

Keywords: *oversampling, A/D converter, multirate signal processing, single-bit quantization, multi-bit quantization.*

I. INTRODUCTION

The real world signals like speech, music, multimedia signals or the data received from the sensor are continuous in nature and not discrete in nature[10]. But all the processing system works on discrete or digital form of data which means most of such signals like for telephony, industrial measurement and instrumentation signals, wireless radio signals and other audio signals are processed by digital signal processing techniques[2]. The inputs given to these processors are mainly in analog form so some interface stages are required which will convert the analog signal in digital form needed by processing core to final provide you the required output. It is also very necessary to provide the conversion with very less noise so that the system will give you the desired output as the noise will finally effect the output so it is useful to relate analog and discrete signals both in time and frequency domain[3].

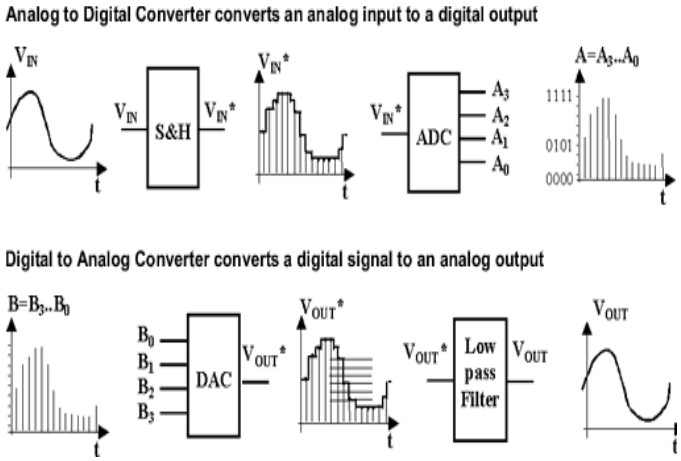

Figure 1: Analog to digital convertor and digital to analog convertor

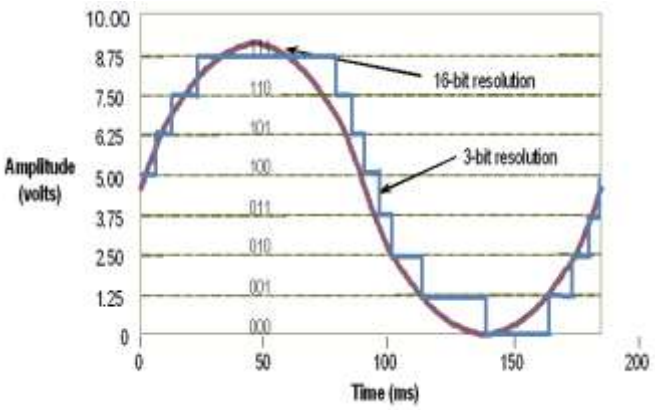

Figure 2: 3 bit digital data using analog signal

An analog to digital converter is used to get the discrete samples of a continuous analog voltage and finally gives you the discrete binary representation of the signal[7]. Characteristics of ADC are: input voltage range, resolution, and bandwidth (conversion rate). When analog signal is converted into digital form analog data gets converted into a staircase like waveform.

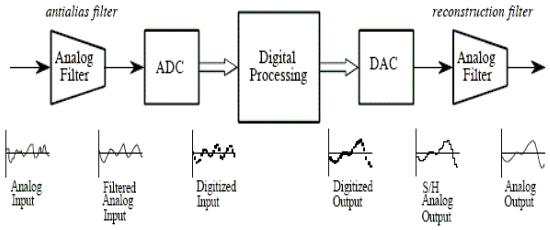

Figure 3: Block diagram representation of A/D and D/A

The Nyquist-Shannon Sampling Theorem states that the minimum sampling rate should be at least twice the frequency of the highest frequency component present in the target signal (Nyquist Frequency). For example, to recreate or get the original signal of the analog signal with up to 20 kHz bandwidth, you must sample it at a minimum of 40 ksps[6]. Analog signal contains desired frequency components and also high frequency components so the sampling frequency should be greater or equal to the twice of analog signal frequency. While using converters at nyquist rate the accuracy can be achieved at 12 to 14 bit due to the dependency on matching components used, more than that it will be impractical to implement [4].

II. OVERSAMPLED DATA CONVERTER

These converters uses oversampling technique where more number of samples of the data are taken to reduce quantization noise to very low levels. Oversampling means sampling the signal at a rate significantly higher than the Nyquist Frequency[5]. The ADC resolution is not directly improved by increasing sampling rate, but by taking more samples, this input signal is tracked more accurately. The oversampling technique improves the digital representation of the signal only down to the physical dynamic range limit (minimum step size) of the ADC. Sampling frequency reduces the quantization noise as it is inversely propotional to the sampling frequency.

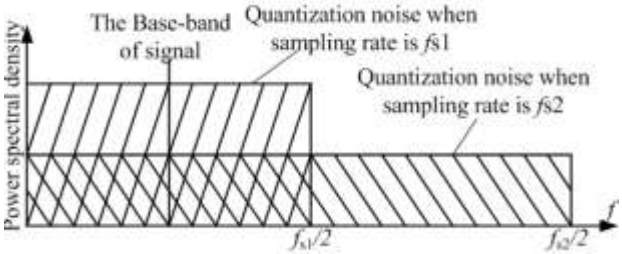

Figure 4: At different sampling frequency the quantization noise

III. Oversampling A/D Conversion

An Example is taken to analyze the oversampling A/D conversion with low resolution A/D converter. Here we have taken number of samples to 4 in figure 5 and number of samples to 7 in figure 6 and number of samples to 10 in figure 7.

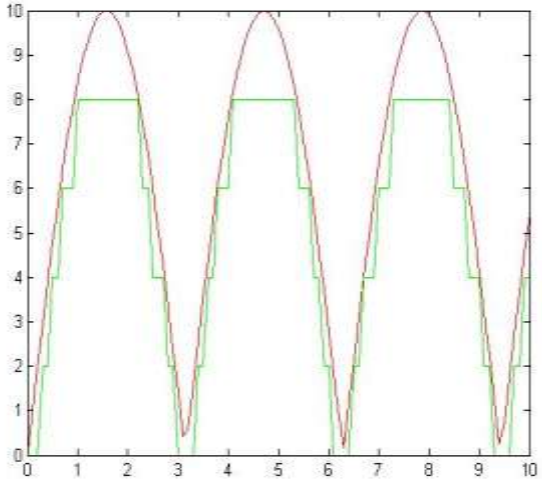

Figure 5: number of samples taken are 4

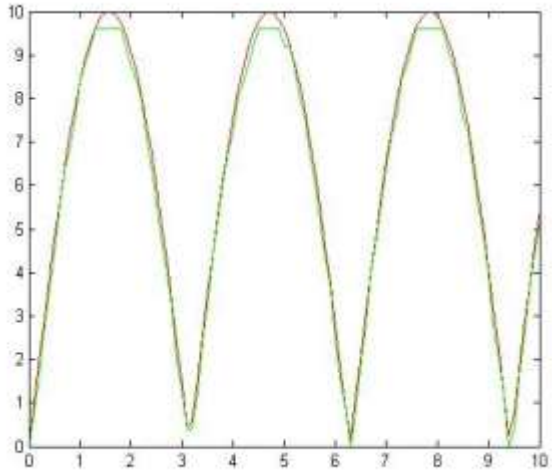

Figure 6: number of samples taken are 7

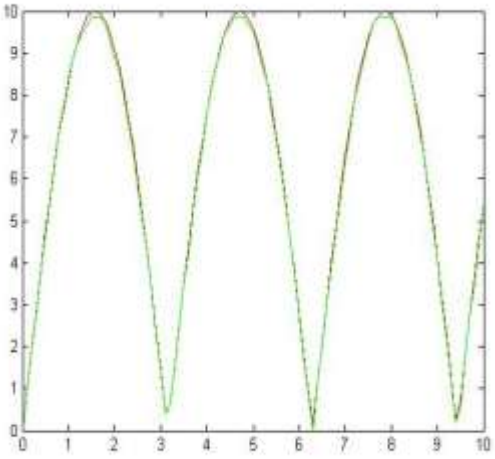

Figure 7: number of samples taken are 10

IV. CONCLUSION

So we have studied here the effect of oversampling technique to reduce the noise and improve the signal to noise ratio in analog to digital conversion process. In this paper the results are shown at different sampling rates to improve output signal quality.

REFERENCES

[1] Sanjit K Mitra "Digital Signal Processing" Tata McGRAW-Hill, ISBN 0-07-060109-7, pp171, pp920-921, Third Edition, 2006

[2] G. C. Temes, "An Overview of Nyquist-Rate and Oversampled Data Converters in Telecommunications," Actas I. Conferencia Nacional de Telecommunicacoes, Aveiro, Portugal, pp. 15-18, April 10-11, 1997.

[3] Emmanuel C. Ifeachor, Barrie W. Jervis "Digital Signal Processing" Pearson Education, ISBN 978-81-317-0824-8 2007, pp86-87, Second Edition, 2007.

[4] Gabor C. Temes "Oversampling A/D And D/A Converters" Dept. of Electrical and Computer Engineering, Oregon State University, Corvallis, OR 97331, USA

[5] Sugreev Kaur, Rajesh Mehra, "High Speed and Area Efficient 2D DWT Processor based Image Compression" Signal & Image Processing" An International Journal(SIPIJ) Vol.1, No.2, December 2010

[6] Shaminder Kaur, Rajesh Mehra, "FPGA Implementation of OFDM Transceiver using FFT Algorithm" International Journal of Engineering Science and Technology (IJEST), ISSN : 0975-5462, Vol. 4 No.04 April 2012

[7] Rajesh Mehra, Garima Saini, Sukhbir Singh, "FPGA based high speed BCH encoder for wireless communication applications", Communication Systems and Network Technologies (CSNT), 2011 International Conference pp576-579.

[8] Lipika Gupta, Rajesh Mehra, "Modified PSO based adaptive IIR filter design for system identification on FPGA", *International Journal of Computer Applications (0975 – 8887) Volume22– No.5, pp1-7 May 2011*

[10] Rajesh Mehra, Abhishek Singh, "Real time RSSI error reduction in distance estimation using RLS algorithm", Advance Computing Conference (IACC), 2013 IEEE 3rd International, pp661-665, 2013.

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