Design & Simulation of GSM FH Transmitter Using SDR Technology

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***Abstract*—** *Software Defined Radio (SDR) is a computer based system that emulates the behavior of traditional radio systems by processing digitized radio signals. A SDR replaces the traditional fixed hardware radio with a system that may be reconfigured, both during operation to provide greater flexibility and by providing software upgrades to add new capabilities without requiring new hardware. Due to these powerful reasons, a wide range of radio applications like GSM, Bluetooth, GPS, Radar, GPRS, etc. can be implemented using SDR technology. In this paper, the global system of mobile communications (GSM) frequency hopping transmitter using SDR technology is designed and simulated with Matlab/Simulink. It has been implemented using 1-bit Continuously Variable Slope Delta-Modulation (CVSD) for speech coding, then channel coding using Block codes and Convolutional codes is designed. After that Diagonal Interleaver is used. Then BFSK modulation is designed. Finally BFSK modulation with Frequency Hopping is used which provide protection against eavesdropping and jamming. The performance analysis according to data rate of input and output signals is presented and discussed.*

Keywords— *SDR, GSM, Matlab, FH.*

I. INTRODUCTION

Recently, many communications systems implemented much of their functionality in dedicated hardware. Dedicated modulators, demodulators, detectors and encoders made these systems static and difficult to upgrade. As general purpose processor (GPP) and digital signal processor (DSP) technology improved, a growing number of signal processing steps such as error correction, equalization, frequency hopping (FH), modulation, demodulation, spreading, despreading and timing recovery could be achieved purely in software. While it is common for modern communications systems to include some software, a system is not considered a software-defined radio until its baseband operations can be completely defined by software [1]. A SDR provides radio users with much greater flexibility than is available from traditional hardware defined radio. When a new standard is developed, rather than replace the entire radio, only the software needs replacing. When two groups of people who normally use incompatible standards must work together, their radios could be loaded with software that allowed them to communicate with each other. Over the lifetime of a hardware design, new improved radio standards can be installed on the radio without requiring replacement hardware. These characteristics of SDR provide cost savings by extending the life cycle of hardware and provide more capability from a given set of hardware [2].

The main aim of this paper was primarily getting familiarized with the exciting technology of SDR. In order to do that, one of the fairly wide spread communication systems is implemented. Hence implementation of a GSM FH transmitter using SDR technology is chosen. First speech encoding, channel encoding, interleaver are implemented using Matlab/Simulink and achieving a bit rate of 13 kbps, 22.8 kbps, 22.8 kbps respectively according to the GSM standard. Then BFSK with 2Mbps transmission speed is implemented. Finally BFSK with frequency hopping spread spectrum is implemented and the result is shown.

The rest of this paper is organized as follow: Section II gives an overview of the GSM system. Section III describes in details the GSM transmitter which we designed. Section IV presents The GSM transmitter Simulations and results using Matlab. Finally, Section V summarizes the conclusion of this paper.

II. GSM SYSTEM

The basic system block diagram of GSM is shown in Fig. 1. GSM is a digital communications standard, but voice is analog, and therefore it must be converted to a digital bit stream. GSM uses Pulse Coded Modulation (64 kbps) to digitize voice, and then the Rectangular Pulse Excited Linear Predictable coding with Long Term Prediction (RPE-LTP) technique which removes the redundancy in the signal and achieve a bit rate of 13 kbps. Depending on the relative importance of the bits, the channel coding function arranges the bits into blocks and adds some error correction codes achieving a bit rate of 22.8 kbps. The encoded bits are then applied to interleaver, which shuffles the bit positions in the blocks to reduce the effect of burst errors and achieve a bit rate of

22.8 kbps. The interleaved bit blocks are assembled with some training bits, and control bits to form normal speech GSM bursts. These bursts are encrypted using A5 algorithm so that any other device than the intended receiver cannot interpret it. Finally the GSM bursts are modulated by GMSK modulation technique before sending to RF amplifier and antenna. The process in the receiver side is the reverse of the transmitter.

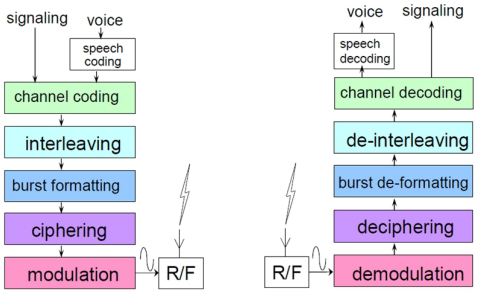

Fig.1 Complete GSM system

III. PROPOSED SYSTEM

The system model has been implemented as shown in Fig. 2. Speech encoding (CVSD), channel encoding, interleaver, binary frequency shift keying and frequency hopping are designed and simulated using Matlab/Simulink to achieve the bit rate of the GSM transmitter.

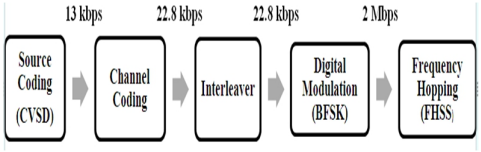

Fig. 2 System model

A. Source Encoding

Speech coder maps speech into digital blocks. Coder used in GSM compresses the speech signal to 13 kbps rate using the Rectangular Pulse Excited Linear Predictable coding with Long Term Prediction (RPE-LTP) technique. This algorithm produces a speech block of 260 bits every 20 ms.

Here we are presenting a 1-bit Continuously Variable Slope Delta-Modulation (CVSD) [3, 4] with data rate 13 kbps for speech coding. CVSD is a modification of Delta Modulation (DM) [5]. DM is a differential waveform quantization / coding technique. A DM encoder uses the error between the original signal to be coded and the coded signal itself to create a differentially-quantized data stream. This data stream is a lower-bit-rate signal that can be decoded by a matched decoder on the receiver side and thus achieves data compression resulting in low data transmission rates. But the performance of the DM encoder is limited by two types of distortion: slope overload and granular noise. Issues with granularity and slope overload can be drastically reduced by making dynamic adjustments to the quantizer step size. Adaptive DM (ADM) algorithms attempt to do this by making step size small for slowly changing signals and large for rapidly changing signals. The most publicized ADM algorithm is known as CVSD.

CVSD is a linear delta modulation with the addition of an adaptive step-size. In the encoded bit-stream, each 1 bit increases the amplitude by the step-size as compared to the previous decoded signal sample. A 0 bit decreases the amplitude by the step-size. By adjusting or adapting the step-size to the changes in slope of the input signal, the encoder is able to represent low-frequency signals with greater accuracy without sacrificing much performance due to slope-overload at higher frequencies. When the slope of the input signal changes too rapidly for the encoder to keep up with it, the step-size is increased. Conversely, when the input signal slope changes slowly, the step-size is decreased. A slope-overload detector and syllabic filter are used in conjunction with a Pulse Amplitude Modulator (PAM) to accomplish the step-size adaption. A slope-overload detector and syllabic filter are used in conjunction with a Pulse Amplitude Modulator (PAM) to accomplish the step-size adaption. The block diagram of CVSD encoder is shown in Fig. 3.

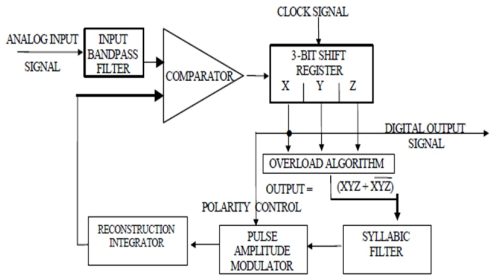

Fig. 3 CVSD encoder

B. Channel Encoding

Channel coding introduces redundancy into the data flow in order to allow the detection or even the correction of bit errors introduced during the transmission [6]. The speech coding algorithm produces a speech block of 260 bits every 20 ms (i.e. bit rate 13kbit/s). The 260 bits of the speech block are classified into two groups. The 78 Class II bits are considered of less importance and are unprotected. The 182 Class I bits are split into 50 Class Ia bits and 132 Class Ib bits (e.g. Fig. 4) Class Ia bits are first protected by 3 parity bits for error detection using Cyclic Redundancy Check (CRC) protection. Class Ib bits are then added together with 4 tail bits before applying the convolutional code with rate r=1/2 and constraint

length K=5. The resulting 378 bits are then added to the 78 unprotected Class II bits resulting in a complete coded speech frame of 456 bits (e.g. Fig. 5)

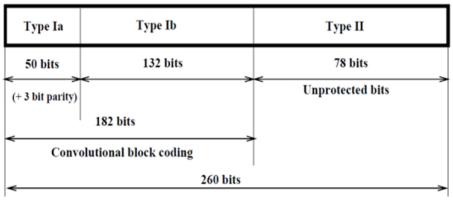

Fig. 4 Audio sample: 1 block = 260 bits (20 ms)

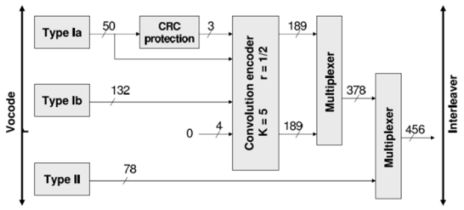

Fig. 5 Channel encoding in GSM

1) ***Cyclic Encoding:*** The Class IA bits are encoded using a cyclic encoder to add three bits of redundancy code to enable assessment of the correctness of the bits which are more sensitive to errors in the speech frame (the category Ia 50-bits). If one of these bits is wrong, this may create a loud noise instead of the 20 ms speech slice. Detecting such errors allows the corrupted block to be replaced by something less disturbing. The polynomial representing the detection code for category Ia bits is G(X) = X3 +X + 1 [7], as shown in Fig. 6.

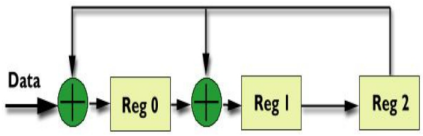

Fig. 6 Cyclic encoding

2) ***Convolutional Coding:*** The GSM convolutional code consists in adding 4 bits (set to "0") to the initial 185 bit sequence and then applying two different convolutions: polynomials are respectively G1(X) = X4+X3+1 and G2(X) =X4 +X3+X +1, as shown in Fig. 7. The final result is composed of twice 189 bits sequences.

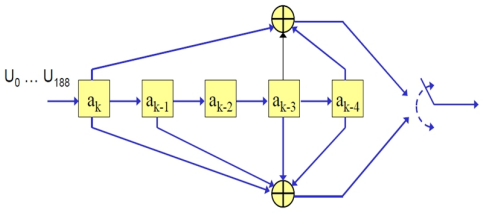

Fig. 7 Convolutional encoder for GSM speech (Rate=1/2, K=5)

The GSM convolutional coding rate per data flow is 378 bits each 20 ms, i.e.: 18.9 kb/s. However, before modulate this signal, the 78 unprotected Class II bits are added. So, the GSM bit rate per flow is 456 bits each 20 ms i.e. 22.8 kb/s.

C. Interleaving

Interleaving [8] means to de-correlate the relative positions of the coded bits within the code words. Interleaving algorithms avoid the risk of loosing consecutive data bits.

In GSM, 456 bits of speech block from the channel encoder is split into eight groups of 57 bits, as shown in Fig. 8. Each group of 57 bits is then carried in eight different bursts. Group of 57 bits is carried by a different burst and in a different TDMA frame. Burst contains 148 bits including two successive 57 bits of 456 bits speech code. These two speech blocks are in even and odd blocks in a burst (i.e. block A and block B), block A takes the even positions inside the burst and bits of block B, the odd positions.

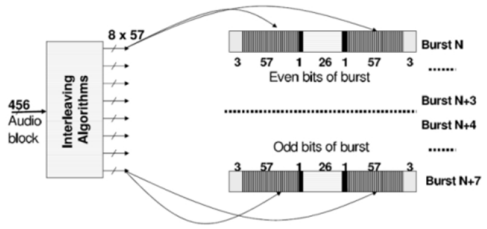

Fig. 8 GSM interleaving

D. BFSK Modulator

In frequency shift keying (FSK), the frequency of the carrier is shifted between two discrete values, one representing binary "1" and representing binary "0" but the carrier amplitude does not changes. The simple form of FSK is BFSK [9]. A typical pair of sinusoidal waves is described by

$$s_i(t) = \begin{cases} \sqrt{\frac{2E_b}{T_b}}\cos(2\pi f_i t), & 0 \le t \le T_b \\ 0, & \text{elsewhere} \end{cases} \quad (1$$

Where i = 1, 2, and E_b is the transmitted signal energy per bit; the transmitted frequency is

$$f_i = \frac{n_c + i}{T_b} \text{ for some fixed integer } n_c \text{ and } i=1, 2 \quad (2)$$

Thus symbol 1 is represented by $S_1(t)$, and symbol 0 by $S_2(t)$.

A block diagram of BFSK modulator is shown in Fig. 9. The incoming binary data sequence is first applied to an on-off level encoder, at the output of which symbol 1 is represented by

constant amplitude of $\sqrt{E_b}$ volts and symbol 0 is represented by zero volts. By using an inverter in the lower channel in Fig. 9, when we have symbol 1 at the input, the oscillator with frequency F_1 in the upper channel is switched on while the oscillator with frequency F_2 in the lower channel is switched off, with the result that frequency F_1 is transmitted. Conversely, when we have symbol 0 at the input, the oscillator in the upper channel is switched off and the oscillator in the lower channel is switched on, with the result that frequency F_2 is transmitted. BFSK modulated signal, carrier signals and transmitting signal are shown in Fig. 10.

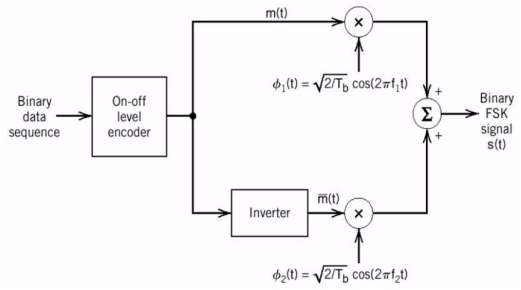

Fig. 9 BFSK modulator

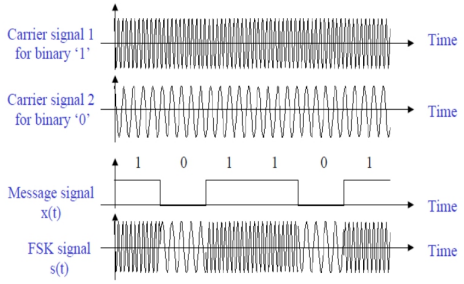

Fig. 10 BFSK waveforms

E. Frequency hopping Spread Spectrum

The type of spread spectrum in which the carrier hops randomly from one frequency to another is called a frequency hopping spread spectrum (FHSS) [10], [11], [12], [13], [14]. Frequency hopping was first used for military electronic countermeasures, because the transmitted signal that uses frequency hopping is difficult to detect and monitor. A typical FHSS transmitter is shown in Fig. 11.

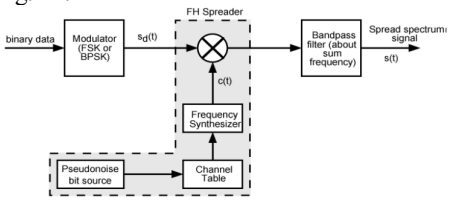

Fig. 11 Frequency Hopping Spread Spectrum transmitter

IV. SIMULATIONS AND RESULTS

This section presents the simulation of CVSD encoder, channel encoder, interleaver, BFSK, and FHSS systems and the results obtained.

A. Simulink Implementation of CVSD encoder

Fig. 12 shows the Matlab/Simulink based implementation of 1-bit, 13 kbps CVSD speech encoder. CVSD encoder takes analog input signal and produces digital output signal with bit rate 13kbps as shown in the display where the simulation time is 10 sec. The results are shown in Fig. 13; top plot is the original speech signal and second one is the encoded digital signal.

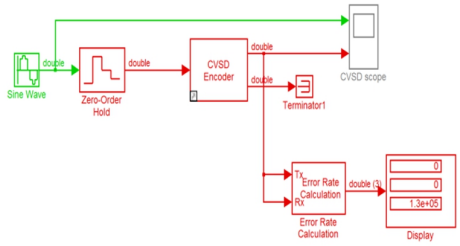

Fig. 12 Simulink based implementation of 1-bit CVSD encoder

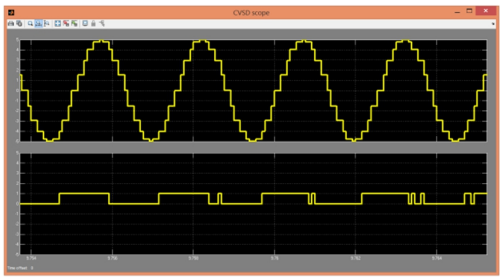

Fig. 13 (a) original speech signals, and (b) encoded speech signal

B. Simulink Implementation of Channel encoding

Matlab/Simulink based implementation of channel encoding is shown in Fig. 14. Channel encoder takes output signal from CVSD encoder and adds extra bits to the signal, so it produces digital signal with bit rate of 22.8 kbps. To achieve this bit rate, channel encoding is implemented as shown in Fig. 15 which consists of CRC generator with generator polynomial [1 0 1 1] come from polynomial G(X) = X3 + X + 1 and convolutional encoder with poly2trellis (5, [33 23]) where K=5 and [33 23] come from polynomials G1(X) = X4+X3+ X +1 and G2(X) =X4 +X3+ 1 respectively. The results are shown in Fig. 16; top plot is the encoded CVSD signal and second one is the channel encoded digital signal.

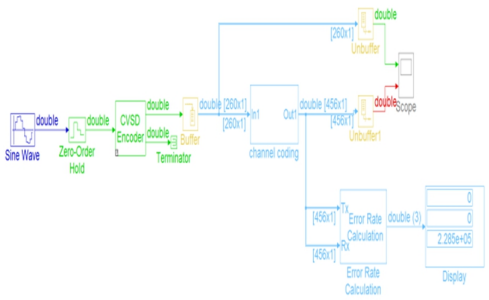

Fig. 14 Simulink based implementation of channel coding

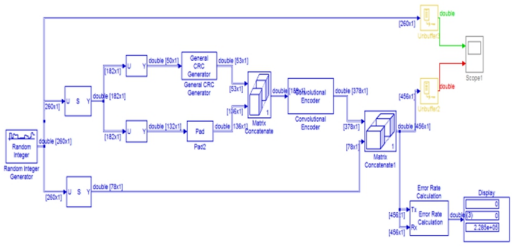

Fig. 15 Simulink implementation of channel encoder in details

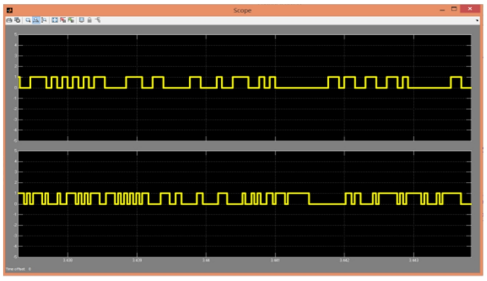

Fig. 16 (a) CVSD encoded signal, and (b) channel encoded digital signal

C. Simulink Implementation of Interleaving

MATLAB / Simulink based implementation of interleaver is shown in Fig. 17. The interleaver takes digital signal from channel encoder and shuffles the bit positions, so it keeps the same bit rate of 22.8 kbps as channel encoder. The signals before matrix interleaver and after matrix interleaver are shown in Fig. 18.

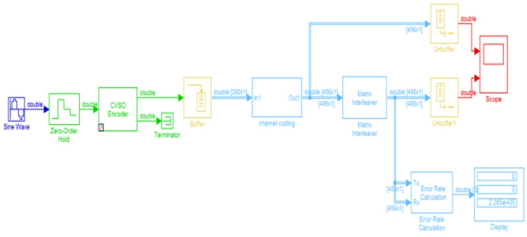

Fig. 17 Simulink based implementation of interleaver

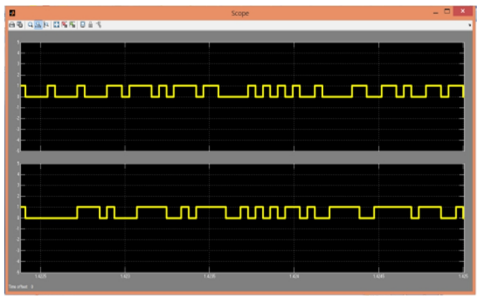

Fig. 18 The un-interleaved and interleaved signals

D. Simulink Implementation of BFSK Modulator

MATLAB / Simulink based implementation of BFSK modulator is shown in Fig. 19. BFSK modulator takes signal from interleaver and produces modulated signal with data rate 2 Mbps. BFSK modulator which we build is shown in Fig. 20. BFSK modulation has been implemented with values: "Fs (space frequency) =114 KHz, Fm (mark frequency) =228 KHz, input data rate= 22.8 Kbps". The simulation results are shown in Fig. 21. The spectrum of BFSK modulator output is illustrated in Fig. 22.

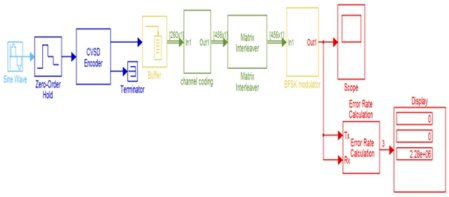

Fig.19 Simulink based implementation of the BFSK modulator

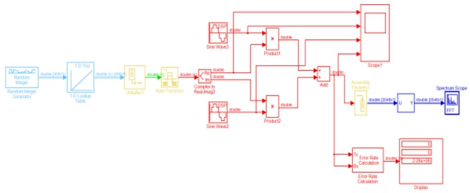

Fig. 20 Simulink based implementation of the building blocks of BFSK modulator

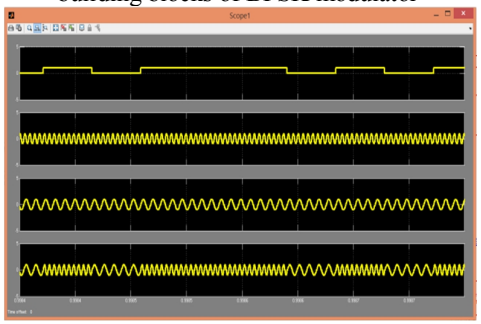

Fig. 21 Waveforms on the scope (a) message signal (b) carrier signal 1 for binary 1 (c)

Carrier signal 2 for binary 0 (d) BFSK modulated signal

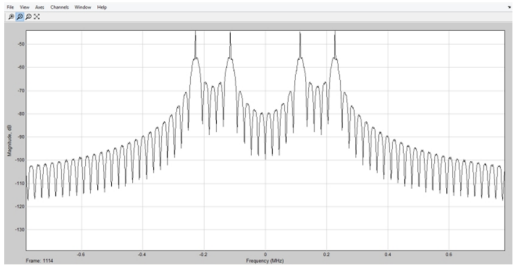

Fig. 22 The spectrum of BFSK modulator output

E. Simulink Implementation of FHSS Transmitter

The Frequency Hopping Spread Spectrum transmitter simulink model is shown in Fig. 23, with 1600 hops per sec and 79 possible carriers at 1Mbps data rate. Also FHSS transmitter result which is obtained using FFT scope is shown in Fig. 24.

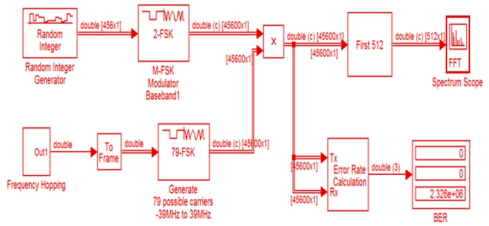

Fig. 23 Simulink model of FHSS transmitter

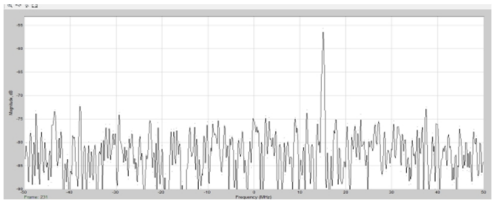

Fig. 24 Matlab-Simulink result of FHSS transmitter Model

F. Simulink Implementation of GSM FH transmitter

In our work SDR technology is used to implement FH GSM Transmitter as in Fig. 2. First 1-bit Continuously Variable Slope Delta-Modulation (CVSD) is chosen for achieving 13 Kbps bit rate for speech coding. Then channel coding using Block codes and Convolutional codes is designed to get 22.8 Kbps. After that Diagonal Interleaver with the same bit rate as channel coding is used. Then BFSK modulation with data rates 2 Mbps is designed. Finally BFSK modulation with Frequency Hopping is used which provide protection against eavesdropping and jamming, as shown in Fig. 25.

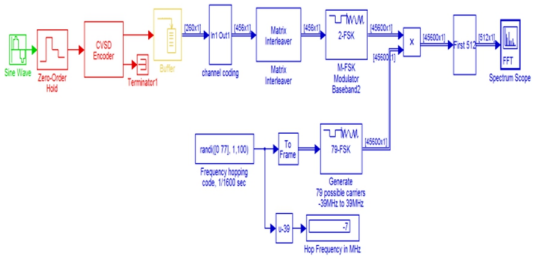

Fig. 25 Simulink implementation of GSM FH transmitter

V. CONCLUSIONS

Design and simulation of GSM FH transmitter using SDR technology is presented here. In the simulink design Fig. 25 shows the complete GSM FH transmitter which consists of speech encoding (CVSD), channel encoding, interleaver, BFSK modulation, and frequency hopping. The outputs of each stage are shown with the designs; Fig. 12, 13 show input/output signals of the CVSD encoder and achieve a bit rate of 13 kbps. Fig 15, 16 show input/output signals of the channel encoder and achieve a bit rate of 22.8 kbps. Fig 17, 18 show input/output signals of the interleaver and achieve a bit rate of 22.8 kbps. Fig 20, 21 show input/output signals of BFSK modulator and achieve data rate of 2 Mbps. From these results, our system model shown in Fig. 2 is achieved.

REFERENCES

[1] Gerald Youngblood. A software-defined radio for the masses, part 1, 2002.

[2] Islam Abd Al-Rahman Galal Al-Dein Abd Al-Latif, "Software Defined Radio Based Implementation of a Wireless Transceiver," Master of Science thesis, August 2013.

[3] D. S. Taylor. Design of continuously variable slope delta modulation communication systems. Application Note AN1544/D, Motorola, Inc, 1996.

[4] Continuously variable slope delta modulation: A tutorial. Application Doc. #20830070.001, MX-COM, Inc., Winston-Salem, North Carolina 1997.

[5] J. G. Proakis. Digital Communications. McGraw Hill, third edition, 1995.

[6] Wakerly, J. \Error detecting codes, self-checking circuits and applications", Computer design and architecture series, the computer science library, Edward J. Mc-Cluskey Editor, 1978.

[7] S. Grech ,"Channel Coding Standards in Mobile Communications," [Online document], September 1999,AvailableHTTP: http://www.tml.hut.fi/Studies/Tik110.300/1999/Wireless/channel_1.html.

[8] Thierry Turletti. Towards the software realization of a gsm base station. IEEE Communication Magazine, vol.17 (no.4), April 1999.

[9] S. Haykin, Communication Systems, 4th Edition, New York: John Wiley & Sons, Inc., 2001.

[10] R. M. Buehrer. *Code Division Multiple Access (CDMA)*. Morgan & Claypool Publishers, 2006.

[11] R. L. Peterson, R. E. Ziemer, and D. E. Borth. *Introduction to Spread Spectrum Communications*. Prentice Hall, Inc., 1995.
[12] R. Dixon. *Spread Spectrum Systems with Commercial Applications*. John Wiley & Sons, Inc., third edition, 1994.
[13] R. L. Pickholtz, D. L. Shilling, L. B. Milstein. *Theory of Spread-Spectrum Communications - A Tutorial*. In IEEE Transactions on Communications, 1982.
[14] D. Torrieri. Principles of Spread-Spectrum Communication Systems. Springer, second edition, 2011.