Design and Simulation of SRAM to Reduce Leakage Current using Enhanced Galeor Approach

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Abstract

In this VLSI design era, low power memory is a need of all computing devices with high performance. The power is most important aspect for today's technology. So design a memory with low power is a vital role. With the rapid progress of technology development, threshold voltage is scale down very narrowly i.e., 180nM from 22nM. Reducing threshold voltage is the major cause of occurring leakage current in SRAM architecture. Enhanced GAted LEakage transistOR (EGALEOR) is a novel technique presented in this paper to reduce leakage current in SRAM architecture. The proposed technique will reduce 40% of static (leakage) power in write operation and 43% of static (leakage) power in read operation. This technique is designed and simulated in Tanner Software.

Keywords

Leakage current, 6T SRAM, threshold voltage, GALEOR and KGALEOR.

I. INTRODUCTION

Rapid growth in VLSI fabrication process results in the increase of the densities of integrated circuit by scaling down the technology. But the devices with such high densities lead to high power consumption and run time failure. Supply voltage has been scaled down to maintain low power consumption. Hence to control drive current and to achieve high performance, transistor threshold voltage scaling leads in the exponential increase of the sub threshold leakage current. Static Random access memory is used in most of the embedded and portable devices because of the high speed. Due to the strong demand of the SRAM memory, reduction of power consumption and leakage current of SRAM memory is very important.

The logical construction of small 4bit SRAM architecture is shown in figure 1. This ram consists of four words of four bits each and has a total of 16 binary cells. The small blocks labelled BC represents the binary cell with its three inputs and one output. A memory with four words needs two address lines. The two address inputs go through a 2*4 decoder to select one of the four words. The decoder is enabled with the memory-enable input. When the memory enable is 0, all outputs of the decoder are 0 and none of the memory words are selected. With the memory select at1, one of the four words is selected, dictated by the value in the two address lines. Once a word has been selected, the read/write input determines the operation. During read operations, the four bits of the selected word go through or gates to output terminals. During write operation, the data available in the input lines are transferred into the four binary cells of the selected word[7]. The binary cells that are not selected are disabled, and their previous binary values remain unchanged. When the memory select input that goes into the decoder is equal to 0, none of the words are selected and the contents of all cells remain unchanged regardless of the value of the read/write input [12].

In this architecture, only four basic cells are operated at a time, remaining basic cells are in standby mode. In standby mode, Leakage current plays a predominant role in SRAM power consumption. So the leakage power consumes more power than dynamic power; it affects the speed of the SRAM operation. To overcome the performance degradation of SRAM, EGALEOR

technique is implemented in SRAM architecture to reduce the leakage current in it.

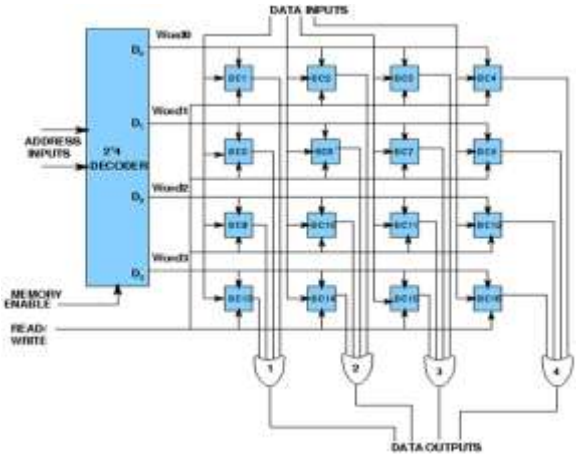

Figure 1 4bit SRAM architecture

1.1 LINEAR REGULATOR

A voltage regulator is a voltage stabilizer that is designed to automatically stabilize a constant voltage level. A voltage regulator circuit is also used to change or stabilize the voltage level according to the necessity of the circuit [11]. Thus, a voltage regulator is used for two reasons:

1. To regulate or vary the output voltage of the circuit.
2. To keep the output voltage constant at the desired value in spite of variations in the supply voltage or in the load current.

A linear regulator is a system used to maintain a steady voltage. The resistance of the regulator varies in accordance with the load resulting in a constant output voltage. The regulating device is made to act like a variable resistor, continuously adjusting a voltage divider network to maintain a constant output voltage, and continually dissipating the difference between the input and regulated voltages as waste heat. Linear regulators may place the regulating device in parallel with the load (shunt regulator) or may place the regulating device between the source and the regulated load (a series regulator). Simple linear regulators may only contain a zener diode and a series resistor as shown in figure 2. The shunt regulator works by providing a path from the supply voltage to ground through a variable resistance (the main transistor is in the "bottom half" of the voltage divider). The current through the shunt regulator is diverted away from the load and flows uselessly to ground, making this form usually less efficient than the series regulator. It is, however, simpler, sometimes consisting of just a voltage-reference diode, and is used in very low-powered circuits where the wasted current is too small to be of concern[4]. This form is very common for voltage reference circuits. A shunt regulator can usually only sink (absorb) current.

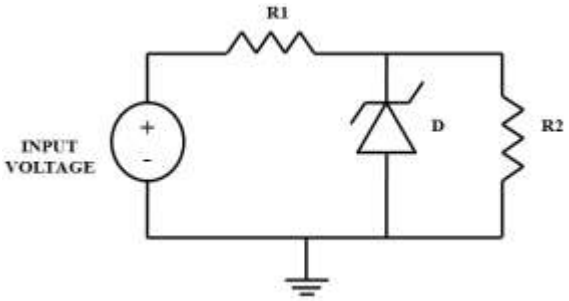

Figure 2 Shunt linear regulators

II. MATERIALS AND METHODOLOGY

2.1 EXISTING METHOD: GALEOR APPROACH

In GALEOR approach, one gate leakage high VT NMOS transistor is introduced between the output and the pull up network and another gated leakage high VT PMOS transistor in inserted between output and the pull down network [2][6] as shown in figure 3. Due to the threshold voltage loss caused by high VT MOS transistors, this technique suffers from significant low voltage swing where low logic level appears much above than 0 and high logic level occurs much below than VDD. Increase of propagation delay is result of low output voltage swing [1][5].

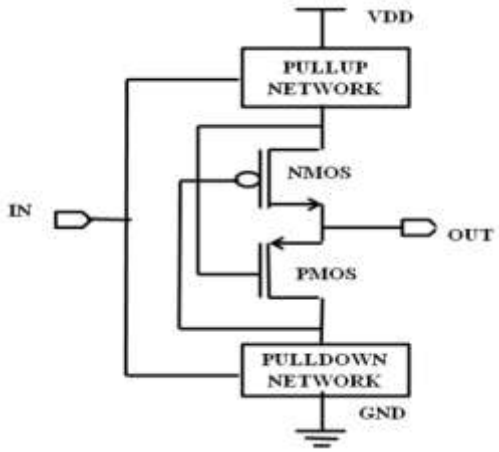

Figure 3 GALEOR approach

2.2 PROPOSED METHOD: ENHANCED GALEOR APPROACH

Enhanced GALEOR method overcomes the disadvantage of GALEOR technique.This technique is the combination of GALEOR technique and simple shunt regulator as shown in figure 4. simple shunt regulator is used to balance the output voltage swing. It consists of resistor and zener diode. zener diode is mainly used to avoid floating output.

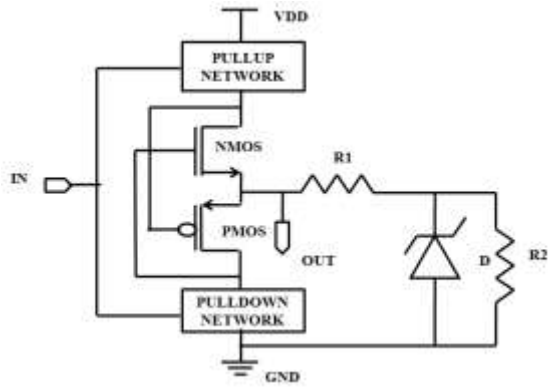

Figure 4 EGALEOR approach

2.2.2 OPERATION

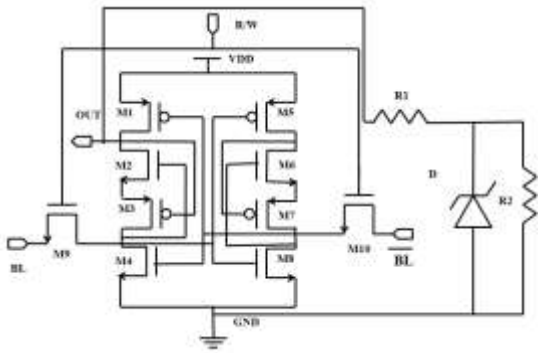

Figure 5 Basic SRAM Cell with EGALEOR Approach

READ OPERATION

To read the data '0(1)' to the SRAM cell, logic values are set on $\overline{BL}$=1(0) and BL=1(0). The W/R input is always high value to shift the data between the data lines, BL, $\overline{BL}$ and the internal load lines [10][13]. The data line (BL or $\overline{BL}$) connected to the load line with logic value'0' will not show any changes in the logic value after transfer of data or otherwise small change occur in the logic value[9]. Due to the driving capacity of the cell the data transfer produces a low value output when logic '0(1)'at the internal load line is shared with the logic '0(1)'of the data line.

WRITE OPERATION

To write the data '1(0)' to the SRAM cell, logic values are set on $\overline{BL}$=1(0) and BL=0(1). The W/R input is always high value to transfer the data between the data lines, BL, $\overline{BL}$ and the internal load lines [8]. The data line (BL or $\overline{BL}$) connected to the load line with logic value'1' will not show any changes in the logic value after transfer of data or otherwise small change occur in the logic value[4]. Due to the driving capacity of the cell the data transfer produces a high value output when logic '1'at the internal load line is shared with the logic '1'of the data line.

The operation summary is shown in the table 1

PROCESS	CONTROL SIGNAL	TRANSISTORS	
		ON	OFF
TO READ "1"	$\overline{BL}$=0, $\overline{BL}$=0	M1,M5,M9, M10	M2,M3,M4,M6, M7,M8
TO WRITE "0"	BL=0, $\overline{BL}$=1	M2,M3,M4, M5,M8,M9, M10	M1,M6,M7
TO WRITE "1"	BL=1, $\overline{BL}$=0	M1,M2,M3,M8, M9,M10	M4,M5,M6,M7
TO READ "0"	BL=1, $\overline{BL}$=1	M4,M8,M9, M10	M1,M2,M3,M5, M6,M7

III. RESULTS AND DISCUSSION

The implementation of EGALEOR technique in SRAM is done using TANNER software. The design is simulated using tanner S-edit window. This technique is verified by using this software which performs simulation of the designed system.

The Schematic diagram for basic SRAM cell with GALEOR technique is shown in figure 6

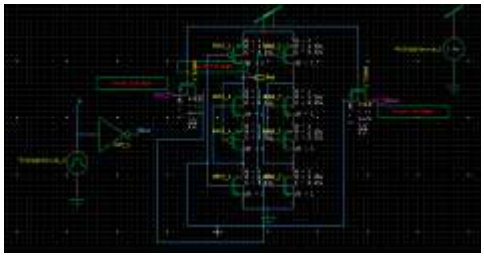

Figure 6 Basic SRAM Cell with GALEOR Approach

The Schematic diagram for basic SRAM cell with EGALEOR technique is shown in figure 7

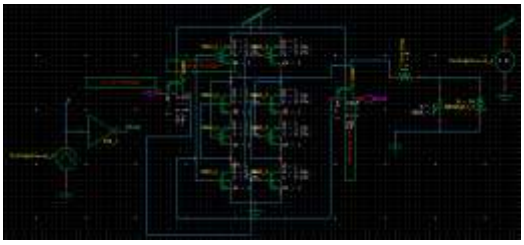

Figure 7 Basic SRAM Cell with EGALEOR Approach

The Simulation waveform of write operation of SRAM cell is shown in figure 8

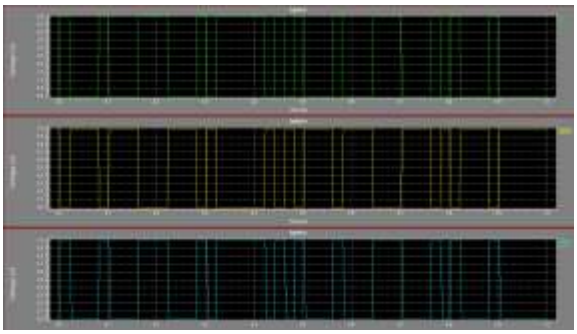

Figure 8 Simulated output of write operation

The Simulation waveform to read 0 operation of SRAM cell is shown in figure 9

Figure 9 Simulated output to read 0

The Simulation waveform to read 1 operation of SRAM cell is shown in figure 10

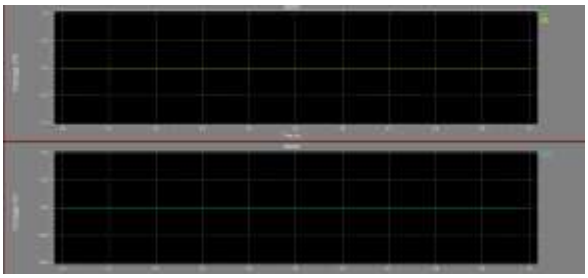

Figure 10 Simulated output to read 1

OPERATION	POWER (*10^{-5})W		PERFORMANCE ANALYSIS
	GALEOR	EGALEOR	
TO READ 0	6.24	5.127	17%
TO READ 1	5.1232	1.9032	62%
TO WRITE 0	3.127	1.298	58%
TO WRITE 1	5.69788	4.022	29%

Table 2 Performance Analysis

4. CONCLUSION

EGALEOR technique has been designed for high speed computations and low power consumptions in SRAM. This technique can be used for meeting the challenges in all portable devices and communication devices by its faster operations. The power consumption of the SRAM is reduced since the leakage current in SRAM is decreased. The static power in SRAM gets reduced by 43 percentages in write operation and 40 percentages in read operation.

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