Impact Analysis of DGMOSFET using High-k Dielectric material

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ABSTRACT

Scaling of MOSFET Devices is an important factor in the advancement of Silicon Technology. This paper examines the Performance Evaluation of a DG MOSFET Devices in the presence of High-k dielectric material like HfO_2, ZrO_2 as compare to conventional bulk SiO_2. A New device structure known as DG MOSFET is simulated, discussed and its efficiency in suppressing short channel effects (SCEs) like Threshold voltage, Leakage current(I_{off}), Drain induced barrier lowering(DIBL),Sub-threshold-slope(SS) has been analyzed. It is observed that using High-k dielectric material HfO_2, ZrO_2 there is decrease in leakage current of about 14% in HfO_2 and 25% in ZrO_2 having L_G of 25nm has been observed as compare to conventional Bulk SiO_2 material. Also, there is significant decrease in Sub-threshold slope is observed about 46% in HfO_2 , 96% in ZrO2 with L_G=24nm and 141% in HfO_2 ,172% in ZrO_2 with L_G=12nm as compared to SiO_2.

Keywords: *Dielectric, High-k, MOSFET, Scaling, SCEs, Leakage, DIBL, SS*

1. INTRODUCTION

Silicon Technologies have been growing faster year to year. One of the main technology advancement factor is gate oxide scaling. Scaling down of device is strongly needed to achieve very high integration density and better device performance [1]. But the main problem which must be focused about silicon technologies is side effects of reducing the dimensions of devices [2]. Due to reduction in channel length, short channel effects and the leakage current become vital issues that degrade the performance of the device. To overcome this issue a Double Gate DG-MOSFET with high-k dielectric material like HfO_2, ZrO_2 are preferred as compared to SiO_2 with dielectric strength lies between 30 and 40, thus makes it possible to increase 6-10 times in equivalent oxide thickness(EOT) for better device performance than conventional bulk MOSFET [3]. The EOT is basically the sum of EOTs of the high-k dielectric and interfacial layer. The semiconductor industry employs a Roadmap the "ITRS", which sets up speed for MOSFET Development.

The Dielectric constant K is a parameter which defines the ability of material to store charge. The value of K usually calculates the value of capacitance of device. With high-k dielectric coupling between two conducting plates is strong and with low-k dielectric coupling is weak. However, in silicon technology, reference value of k for SiO_2 is 3.9. Dielectric having k greater than 3.9 are referred to as high-k dielectric material whereas dielectric having value less than 3.9 referred to as low-k dielectric material. From the past few years, high-k dielectric based on Hafnium (HfO_2) with DG-MOSFET has been introduced to enhance device performance while reducing gate leakage as EOT is increased [4]. The decrease in Threshold voltage (V_{th}) with decrease in channel length and increase in drain voltage is usually due to presence of short channel effects in recent CMOS Technologies. In this paper, a Simulation Analysis using 3-D TCAD simulator COGENDA GENIUS is done to see the impact of the leakage current on the device performance by using high-k dielectric material HfO_2 as compared to SiO_2. For the Simulation, we have used different diffusion, mobility density gradient quantum correction model. Also, Enhanced Lombardi mobility degradation model was activated which accounts for mobility degradation at silicon-SiO_2, HfO_2 interface. To find accurate threshold voltage, constant current method is used.

2. SHORT CHANNEL EFFECTS

Scaling of MOS dimensions is very important in order to design high performance VLSIs. Short Channel effects (SCEs) are the severe aftereffects of scaling. SCEs cause the dependence of device threshold voltage upon channel length [5]. SCEs degrade the controllability of gate voltage upon drain current, which results in the degradation of the sub-threshold slope and significant increase in drain off-current [6]. The first SCE model was proposed by Poon and Yau [7] which gave description of charge sharing effect by respective gate and drain electric fields in the depletion channel. A MOSFET device is considered to be short when the respective channel length is the same order of magnitude as the source and drain junction depletion-layer widths. As the channel length is further reduced to enhance speed as well as density, short channel effects (SCEs) came into effects. Use of High-k dielectric material like HfO_2 and ZrO_2 as compared to SiO_2 is one of the effective way of reducing short channel effects. There are

various SCEs in MOSFETs. In this paper, following SCEs has been discussed and analyzed:

2.1 Threshold Voltage

The Threshold Voltage of an n-channel MOSFET is usually given [8] by:

$$V_{th}=\Phi_{MS}-\frac{Q_{SS}}{C_{OX}}+2\Phi_F+\frac{qN_aX_{d\max}}{C_{ox}} \quad (1)$$

Where Φ_{MS} is the work function difference between the gate and the channel , Q_{ss} is the surface state charge of the channel, Cox is the gate capacitance and equal to $\frac{\varepsilon_{ox}\varepsilon_o}{t_{ox}}$, here t_{ox} is the gate oxide thickness. Φ_F is the Fermi potential, equal to $\frac{KT}{q}\ln\frac{(N_a)}{n_i}$, where N_a is the channel doping concentration, X_{dmax} is the maximum depletion width. As there is change in channel length, threshold voltage changes . In case of long channel MOSFETs, gate has control over the channel and supports most of the charge. But in case of Short channel lengths, the threshold voltage begins to decrease as the charge in the depletion region increases [9].

2.2 Drain Induced Barrier Lowering (DIBL)

The Source and Drain depletion regions can interfere into the channel even without bias as these junctions are usually brought together in short channel devices. This effect is usually known as charge sharing. Since, drain and source also takes part in charge region of the channel which would otherwise was only controlled by the gate. As with the increase in bias drain depletion region continues to rise so that it can actually make interaction with the source to channel junction which in turn decrease the potential barrier [10]. DIBL is usually given by equation:

$$\text{DIBL} = -[\frac{V_{th},sat-V_{th},lin}{V_d,sat-V_d,lin}] \quad (2)$$

Where(V_{th},sat)= saturated threshold voltage, (V_{th},lin)= linear threshold voltage, (V_d,sat)=Drain voltage applied in saturation region, (V_d,lin)= Drain voltage applied in linear region. Here, we have use (V_d, sat) = 0.75 V and (V_d, lin)=0.05 V.

2.3 Sub-threshold Slope

It usually defines the way that how effectively the flow of drain current of a device can be stopped whenever V_{gs} is decreased below threshold voltage (V_{th}). Steeper the I_d-V_g curve , more improvement will be there in sub-threshold slope of the device. Sub-threshold Slope [11] is given by:

$$\text{SS}=[\frac{d(\log_{10}I_{ds})}{dV_{gs}}]^{-1}=\frac{KT}{q}(1+\frac{c_d}{c_i})$$

(3)

Where C_d= depletion layer capacitance
C_i=gate oxide capacitance

A device which is characterized by steeper sub-threshold slope undergoes faster transition between off current and on current.

3. TRANSPORT DESCRIPTION

The Cogenda TCAD Device simulates the I_D-v_G performance of DG-MOSFET using the basic drift-diffusion transport model.

3.1 Drift diffusion model

The conduction in this model depends upon the Poisson's equation (3) and continuity equation of the carriers (4), (5). The Poisson's equation which transforms the electrostatic potential V to the density of charge is given by [12]:

$$\nabla^2V=-\frac{q}{\varepsilon}[p-n+N^+{}_D+N^-{}_A+n_T]$$

(3)

Where n and p represent the densities of the electrons and the holes, respectively, N_D^+ and N_A^- are the ionized donor and acceptor impurity concentrations respectively, n_T is the density of carriers due to the centre of recombination[12] and ε is the respective dielectric constant. The current densities of electrons and the holes are given by the transport equations usually composed of two components, drift and diffusion [12].

$$J_n=q\mu_nnE+qD_n\nabla_n \quad (4)$$

$$J_p=q\mu_ppE-qD_p\nabla_p \quad (5)$$

Where μ_n, μ_p are respective electron and hole mobilities, D_n and D_p are the diffusion coefficients of electrons and holes ∇_n,∇_p are the corresponding two dimensional concentration gradients of electrons and holes respectively. E is the electric field which is being applied. The equations of continuities demonstrate the carriers conservations in a particular volume element for the corresponding electrons and holes respectively.

$$\frac{\partial n}{\partial t}=GR_n+\frac{1}{q}\nabla J_n \quad (6)$$

$$\frac{\partial p}{\partial t}=GR_p-\frac{1}{q}\nabla J_p \quad (7)$$

The GR_n and GR_p usually describe the process of recombination-generation and J_n , J_p are their respective current densities [12]. The EOT (Equivalent Oxide Thickness) is given as[13]

$$\text{EOT}=\frac{Ksio_2}{K_{High-k}}(T_{high-k}) \quad (8)$$

Where K_{sio2}, $K_{High\text{-}k}$ are the respective dielectric constant of SiO_2 and the High-k dielectric and $T_{high\text{-}k}$ represents the thickness of high-k material.

4. DEVICE STRUCTURE

The Double Gate MOSFET is shown below in Figure1. This particular symmetrical structure consists of heavily doped n-type source and drain regions of length 24 nm. The structure contains a p-type doped Silicon channel of width 8nm.The polysilicon gates are separated from the silicon channel by an equivalent oxide layer with a power supply voltage VDD of 0.7V**.** In this paper in order to highlight the performance of DG-MOSFET device at channel length (L_G) 12nm & 24 nm and effect of EOT, we have carried out simulations using three gate dielectrics SiO2, HfO_2 and ZrO_2. The varying Parameters are oxide thickness (1.5nm), channel length (12nm and 24nm) and dielectric constant using the same silicon channel width of 8nm. The values of Gate work function which is one of the most important parameters between high-k material and silicon substrate are 4.45eV and 4.9eV. The values of Dielectric constants used in this device are 3.9 for SiO_2 [14], 21.2 for HfO_2 [14] and 25 for ZrO_2 [15].

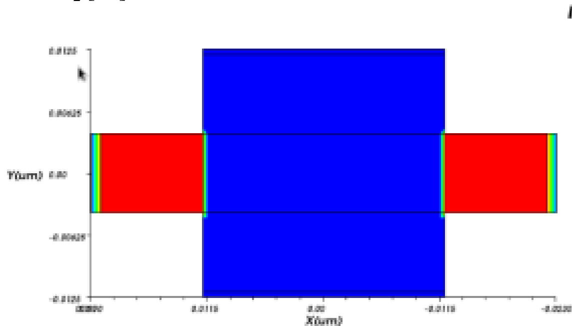

Figure1. Symmetrical DG structure of MOSFET

One of the vital parameters [16] between the high-k materials and silicon substrate is the conduction band offset (CBO). The values used are 3.1eV for SiO_2 [17], 1.4 eV for ZrO_2 [18] and 1.3 eV for HfO_2 [19]. The various parameters used for device in our simulations are summarized in Table1.

Table1. Different Parameters used for device simulation

Parameter	DG MOSFET
Channel Doping	10^{15} cm ^{3}
Source and Drain Doping	1×10^{20} cm ^{3}
Channel length (L_G)	Varies from 12 to 24nm
Oxide thickness	1.5nm
Channel width	8nm
Work function of metal gate	4.45eV,4.90eV

5. RESULTS AND DISCUSSION

Using the proposed model, the $I_D(V_{GS})$ curves having gate dielectrics as SiO_2, HfO_2 and ZrO_2 for EOT=1.5nm at $V_{DS}=V_{DD}=0.7V$ are plotted in Figures 2-4, respectively. These Figures shows the variations of the Drain current with respect to gate voltage for DG MOSFET devices having different channel lengths 12 and 24nm.Some important parameters for device operation derived from $I_D(V_{GS})$ characteristics are summarized in Tables 2-4. These parameters usually includes DIBL, Sub threshold Slope, Threshold Voltage and Leakage current at V_{GS}=0[18]. From the Table 2, it is clear that SiO_2 layer shows a leakage current density equal to 1.29×10^{-6} A/µm at V_{GS}=0 V for a gate length of 24nm. However, a large decrease in I_{off} current of 14 and 25 times is achieved when the conventional SiO_2 is replaced with HfO_2 and ZrO_2 as gate dielectric respectively. The large reduction in gate leakage current can be demonstrated by the fact that the use of a high-k gate material makes possible a thicker physical insulator [20], which reduces tunneling currents. The higher leakage current obtained from HfO_2 as compared to ZrO_2 can be explained with the fact that HfO_2 has lower conduction Band offset as well as thinner physical thickness as compared with ZrO_2. However, the injection of electrons from the inversion channel is characterized by the thickness of the insulator layer and its conduction band offset with respect to the silicon channel [20].

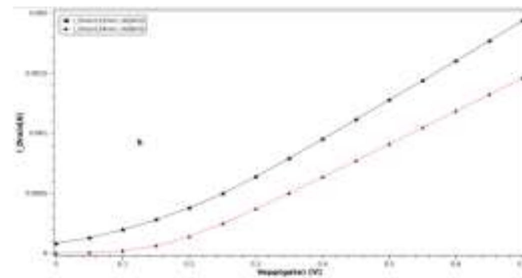

Figure2. I_{DS} versus V_{GS} curve of DGMOSFET with EOT= 1.5nm Gate Dielectric=SiO_2, L_G=12nm, 24nm, H=8nm, V_{DS}=0.7V, N_a=1x10^{15} .

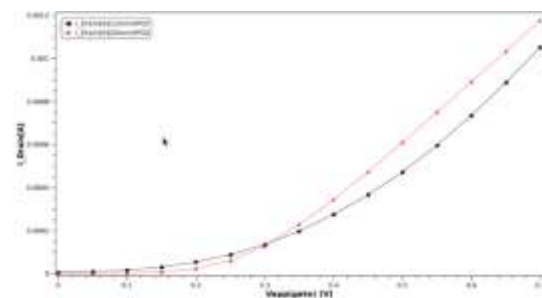

Figure.3 I_{DS} Versus V_{GS} curve of DGMOSFET with EOT = 1.5 nm. Gate dielectric=HfO_2, L_G=12nm, 24nm, H=8nm, V_{DS}=0.7V, N_a=1x10^{15}

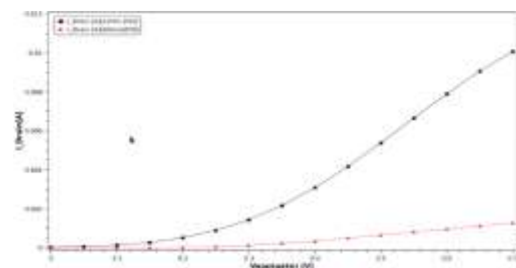

Figure.4 I_{DS} Versus V_{GS} curve of DGMOSFET with EOT = 1.5 nm. Gate dielectric=ZrO_2, L_G=12nm, 24nm, H=8nm, V_{DS}=0.7V, N_a=1x10^{15}

From Table2-4, it is clear that Threshold voltage is Channel length dependent. With the increase in channel length (L_G), Threshold voltage increases, due to increase in Work function from equation (1) which in turn results in decrease in Leakage current. Threshold voltage can be found from I_{DS} - V_{GS} curve using Constant current method. As far as Sub-threshold Slope (SS) is concerned, there is significant decrease in HfO_2 and ZrO_2 as compared to conventional SiO_2. In case of HfO_2, there is 46% and in ZrO_2 its about 96% decrease in SS for channel length 24nm .But However in case of channel length 12 nm, there is 141% in HfO_2 and 172% in ZrO_2 decrease in Sub-threshold Slope as compared to Bulk SiO_2. So, there is huge degradation of SS with the decrease in channel length .So, Sub-threshold characteristics are clearly better than SiO_2 which should be below 80 mV/dec as far as ITRS Recommendation [21] . As we decrease channel length from 24 to 12nm, there is some increase in DIBL, which is due to increase in threshold voltage for V_{DS}=0.05V and V_{DS}=0.7V.

Table2. Simulation results for DG MOSFET with SiO_2 as Gate Dielectric

Parameter	L_G=24nm EOT=1.5nm	L_G=12nm EOT=1.5nm
Sub-threshold Slope(mV/dec)	110	210
OFF(Current)A/μm	1.29e-06	3.035e-05
Threshold Voltage(V)	0.17	0.15
DIBL(eV)	0.0230	0.0235

Table3. Simulation results for DG MOSFET with HfO_2 as Gate Dielectric

Parameter	L_G=24nm EOT=1.5nm	L_G=12nm EOT=1.5nm
Sub-threshold Slope(mV/dec)	75	87
OFF(Current)A/μm	8.68e-11	5.02e-06
Threshold Voltage(V)	0.16	0.14
DIBL(eV)	0.0153	0.0160

Table4. Simulation results for DG MOSFET with ZrO_2 as Gate Dielectric

Parameter	L_G=24nm EOT=1.5nm	L_G=12nm EOT=1.5nm
Sub-threshold Slope(mV/dec)	56	77.01
OFF(Current)A/μm	4.98e-11	2.36e-7
Threshold Voltage(V)	0.15	0.135
DIBL(eV)	0.0076	0.00769

6. CONCLUSION

In this paper, Double Gate structure and High-k Dielectric material are used to compare their performance with conventional SiO2 with respect to Short channel effects. With the decrease in channel length, threshold voltage decreases which results in increase in I_{off} current and DIBL as well as Sub-threshold Slope. But however, we can decrease these effects using High-k material like HfO2 and ZrO2 having high Work function. The Simulations were performed by 3-D TCAD COGENDA GENIUS Simulator which makes use of Drift-Diffusion model for respective transport of carriers. Using High-k Dielectric material having high work functions, there is significant decrease in I_{off} current, lowers Sub-threshold Slope, takes optimum value of DIBL and increase On current. So, in turn maximizing Ion/Io_{ff} ratio.

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