# Efficient Pixel Architecture of CMOS Image Sensor using CMOS 180 nm technology

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***Abstract-*** *This paper describes CMOS Active Pixel Sensor (APS) that has huge demand in imaging systems. The pixel architecture consists of number of NMOS transistors and reverse biased p-n junction diode act as photo sensing element designed in 0.18um CMOS technology. The ($64^{H}X64^{V}$) pixel array have presented and described. The sensor design contains 5T pixel architecture to investigate the effects by measuring its parameters. The Image Sensor presented in this paper achieves better well capacity, voltage swing and conversion gain. The measured results of sensor have pixel bucket with capacity of (28089 $e^{-}$), voltage swing of (1.2V) and conversion gain of (79.1uV/$e^{-}$). By measuring these parameters, the presented pixel architecture can be optimized for several applications.*

**Index terms-** *CMOS Image Sensor (CIS), Active Pixel Sensor (APS), Photodiode.*

## I. INTRODUCTION

In large scale system design, CMOS Image Sensor plays a significant role in imaging systems suitable for different purposes and it has greater demand in market of imaging system [1]. CMOS Image Sensor (CIS) have rapid developments than CCD due to its number of advantages. These are generally higher speed and have larger data throughput as compare to CCD technology, There are such applications of CMOS Image Sensor (CIS) i.e. fluorescence, spectroscopy, time-of-flight imaging, radiation therapy, proton radiography and blue free projectile tracking [2]. There have been several researches done to improve the parameters to produce the high performance Image Sensor. So many applications areas caused that CMOS technology breakthrough on two fronts in 2000: sensors for computers and cell phones on the low end, and ultra high speed, large format imaging on the high end. Moreover, new technologies and architectures appeared due to scale effects [3]. In the world of technology, the demand of CMOS devices rising day by day and their popularity depends on small area and long life time with optimized parameters. So, devices must be design to be used in application by consuming less power [4]-[6]. Technology scaling of CMOS design is one of the driver behind improvement in performance in the integrated circuits [7]-[8]. The CMOS Imager can be voltage mode and current mode. Current mode of CMOS Imager have disadvantage of poor linearity and high fixed pattern noise as compare to the voltage mode CMOS Image Sensor [9]. The Image Sensor of high charge collection efficiency with better conversion gain is often required by scientific, commercial and consumer applications [10]. CMOS Active Pixel Sensor (APS) technology was originally considered as inferior, later improvements in such parameters of Image Sensor i.e. Cost, Power consumption, Dynamic Range, blooming effect, readout scheme, speed and smartness have occurred to achieve high performance equal to or better than CCD technology [11]. Novel technologies coming into focus to provide integration [12] of imaging and processing functions on a single chip, reducing cost and size of CMOS Image Sensor. The traditional imaging readout function enables quick processing of images [13]. In CMOS Active Pixel Sensor (APS), the major source of noise is the reset noise that is occurred when the sense node capacitance is reset [14]. CMOS APS (Active pixel sensor) is made to improve scalability to the large array formats and higher speed readout as compare to the Passive pixel sensors. In CMOS Active Pixel Sensor array, the pixel area is constructed of two functional parts. The first part consist of geometrical shape of sensing element: act as active area to absorb incident illumination energy and convert that energy into charge carriers in silicon substrate. The second part described by control circuitry designed used for readout operations using NMOS transistors because there is no requirement of n-well layer in NMOS transistors. Due to this feature, it consumes less area as compare to the PMOS transistors [15]. In this paper, the CMOS Active Pixel Sensor designed in 0.18um, 3.3V CMOS process consists of 64X64 pixel array with row decoder and column decoder. The array employs pixel level parameters have been measured and optimized. This paper also focuses on the reset noise. In equation form, the reset noise [in volts root mean square (rms) is $\sigma_{reset}(V)= \sqrt{KT/C}$ or, in $e^{-}$units $\sigma_{reset}(e^{-})= \frac{\sqrt{KTC}}{q}$, where C is capacitance of sense node, T is temperature and q is electron charge. The well capacity and conversion gain are of concern. In pixel structure, large well is required, so that blooming effect can reduced to prevent charge overflow from pixel bucket that starts to fill adjacent pixel.

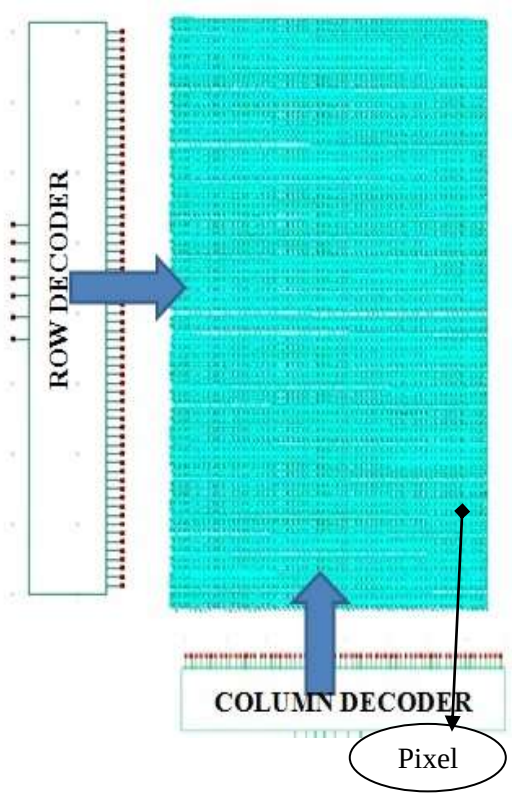


Fig.1 - Block of CMOS Image Sensor

The system architecture of CMOS Image Sensor is shown in fig.1. It consists of Pixel array with number of rows and columns. Row and column decoder implemented by decoder for scanning pixels in the array. Row decoder is Y-addressing line to select the particular row of the pixel array. Column decoder is X-addressing line to read out the column busses that connect the select row the pixel.

## II. Pixel Description and Operation

The pixel act as picture element forms basic unit of image sensor consist of detector and readout circuit to make complete transfer of charge to the external terminal for data acquisition [16].

### *A. The 5T Pixel Architecture*

5T pixel is a variation of 4T pixel that is solving several issues related to imager with four transistors. The main drawback of 4T transistor is due to slightly shifting of start and stop duration of exposure which results to image deformation for fast moving objects. The design of 5T is quite similar to the 4T architecture, except for extra reset transistor to reset all rows simultaneously and for exposure control. The pixel circuitry shown in fig. with single reverse-biased p-n-junction diode (PD) for incident photon conversion to charge, and five transistors i.e. the photodiode reset transistor (M1), transfer gate (M2) to make complete transfer of charge generated by the incident photon during integration period, Floating diffusion reset transistor (M3) to reset floating diffusion node for the next period of integration, Source follower transistor (M4), Row select transistor (M5). There are two major components of junction capacitance of the photodiode: bottom plate and side wall. Both of these components play an important role in the performance of the Active pixel sensor.

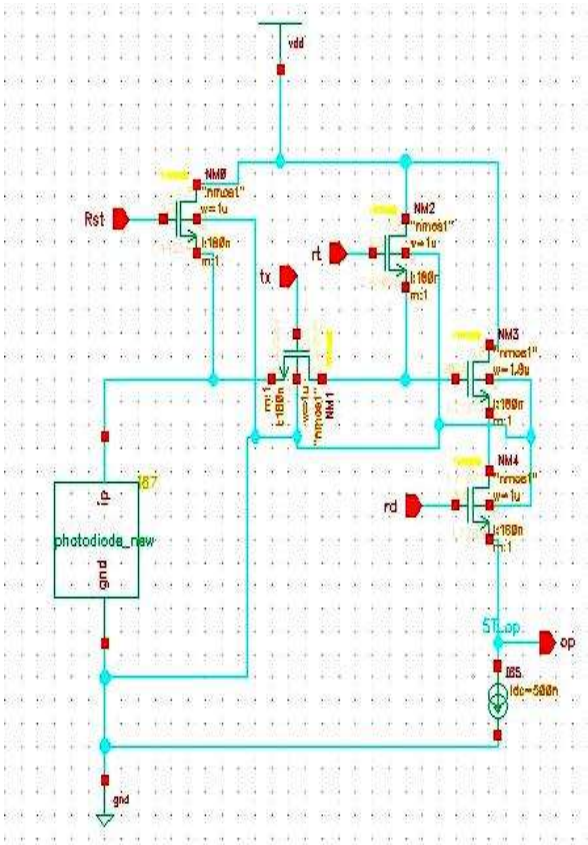


Fig.2- 5T Pixel Architecture

### *B. Operating modes of APS*

There are three operating modes for Active Pixel Sensor: Reset mode, Integration mode, Readout mode. These modes of operation works sequentially for every cycle until the entire rows of array are read out at the column line.

***1) Reset mode:*** Initially, the reset transistor M1 and M3 reset the photodiode and floating diffusion node simultaneously and reset values are readout at the column line.

***2) Integration mode:*** The integration of incident photons starts after reset mode of operation. In this mode, photons are sense by photo sensing element. During this process, the transistor M2 (transfer gate) is on to transfer the photo charge from photodiode node to floating diffusion (FD) node, where FD node act as conversion and memory node because it convert charge to voltage and store charge transferred from FD node until, the RS (Row select) transistor is on.

***3) Read out mode:*** In this mode, row select transistor is responsible for read out the signal through column line by scanning each row of the pixel array.

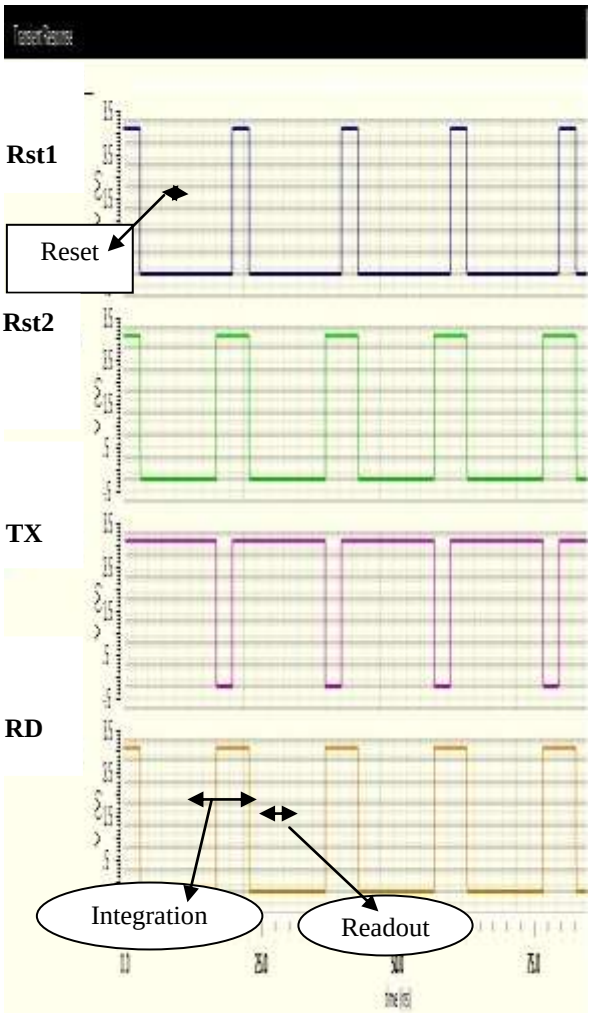


Fig.3- Control Signals for Pixel circuit

Fig.3 shows the waveform of control signals (Rst1, Rst2, TX, and RD) for pixel architecture, where Rst1 is photodiode reset signal, Rst2 is Floating diffusion reset signal, TX is signal for transfer gate and RD is control signal for row select signal. Initially, reset phase takes place. In this phase, Reset transistors (Rst1 and Rst2) are 'on' to reset the charge on photodiode and FD node and reset value is obtained by turning on the Row select transistor (RS). The calculated noise occurred due to reset transistor called Reset noise is $89e^-$ (in terms of $e^-$) and $0.28mV_{rms}$ (in terms of voltage). In next phase, integration of incident illumination takes place. In this phase, the TX transistor is 'on' to transfer charge from PD to FD node. During this integration period, the row select transistor switch to off state. Charge is stored in the floating diffusion node and the accumulated charge convert into voltage in this node. After integration, this voltage is readout by turning on the RD transistor. During this phase, the Rst2 transistor again turns on to make double sampling at the output terminal. After completion of one cycle, these three modes of operation again repeat for the next cycle of operation.

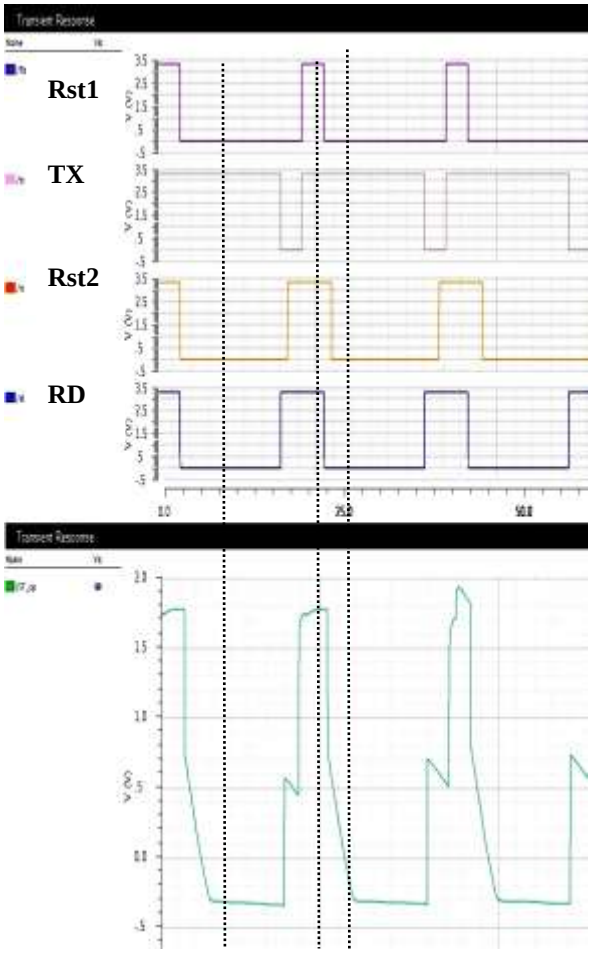


Fig.4- Output waveform for Pixel

The waveform in fig.4 shows the signal obtained on the output of Pixel. At the end of each cycle of pixel operation, two values are obtained i.e. reset value and signal value. Throughout the array, these two values are obtained on output with the column line by turning on their respective row select transistor.

## III. Simulation Results

In this Paper, Spectre simulation is performed using Cadence virtuoso. This design is based on 0.18um CMOS technology.

**TABLE I**
Measured performance of Pixel

| Parameter | Paper [10] | This work |
|---|---|---|
| Technology (um) | 0.18 | 0.18 |
| Pixel Array | 64X64 | 64X64 |

| | | |
|---|---|---|
| Number of transistors per pixel | 4 | 5 |
| Full well capacity ($e^-$) | 19200 | 28089 |
| Conversion Gain at FD (uV/$e^-$) | 69.3 | 79.1 |
| Signal swing (V) | 1.067 | 1.2 |

## IV. CONCLUSION

CMOS Image Sensor technology has excellent performance for the new generation of sensors. In this paper, CMOS Image Sensor ($64^H X64^V$) pixel array has been designed in 0.18um technology and simulated pixel architecture. The Pixel architecture of CMOS Image Sensor presented in this paper improves well capacity by (46.2%), voltage swing by (14.1%) and conversion gain by (12.4%). Future works in CMOS Image Sensor includes the optimization of Column level circuit of the pixel array.

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