# A drowsy cache method based 6T SRAM cell with different performance parameter at 32 nm Technology

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**ABSTRACT**

*Now a day, speedy growth of portable or hardly applications are need of technology. These hardly applications bounded the static random access memory (SRAM) topologies to consider about low leakage current and reduce power consumption. To reduce leakage current and enhance stability many topologies proposed in conventional 6T SRAM cell. This paper presents a drowsy cache method in conventional 6T SRAM cell to boost cell performance at 0.9V power supply. In this paper, we propose a method to achieve 8x and 6x time enhancement in leakage current and power dissipation respectively compare to conventional 6T SRAM cell. Simulations results are improved in read stability read/ write delay, $I_{ON}/I_{OFF}$, leakage current and power dissipation using 32 nm technologies.*

**Keywords-** *Leakage current, power dissipation, Read stability, Read/ Write delay*

## 1. INTRODUCTION

These days, High stability and low leakage current is need of manifold operation system which accessible in solitary apparatus like mobile device [1].Mobile or Portable devices need low leakage current at ultra low power supply to operated for long time and Achieving high stability is beneficial for low data loss[1].Here, main consent for portable device performance are low leakage current with high stability. Consequently, in this paper we illustrate different parameter according to explain different topologies performance in low power supply. There is a drawback in conventional 6T SRAM cell performance due to unwanted time taken by access transistors in pull up and pull down ratio with high power [2].

Now a day, microprocessors require low leakage current for high performance in memory cell and nanometer scaling is requirement in improved technology. Where, Scaling of technology increases leakage current variations. High leakage current can generate difficulty of power consumption in system. Nanotechnology integrated circuits hold up complex designs to enhance performance of memory cell but leakage current effect cell performance by increasing power dissipation.

Read delay and Write delay is measure time delay in sensing the data in output through sense amplifier [3].Delay is affects the performance of SRAM cell and reduce working efficiency of cell. Accessibility of the cell is depending on read/write delay. Proposed technique used in 6T SRAM cell shows less delay compare different topologies of SRAM cell [3].

This work presents a drowsy cache method in 6T SRAM Cell at 32 nm Technology using 0.9v. In this paper we show the assessment of technique in 6T SRAM cell with other topologies of SRAM cell and compare them in a variety of parameters for analyses in ultra low power variation. The leakage, power dissipation, read/write delay and $I_{ON}/I_{OFF}$ ratio are measured in read, write and hold operation.

This paper is assembly as follows. An overview of the literature review is presented in Section II. Experimental results has been discussed in Section III where N-curve, read delay, write delay, $I_{ON}/I_{OFF}$ , leakage and power dissipation parameter has been compared with proposed technique. Section IV has conclusion where we summers overview of all results.

## 2. LITERATURE REVIEW

This article presents the simulation of 6T, 7T, 9T and drowsy cache method in 6T SRAM Cell. The entire simulations have been happened at spice tool.

### *2.1 Conventional 6T SRAM cell*

The conventional 6T SRAM cell construct by two cross-coupled inverter latch with two access transistors joined to a complimentary bit lines as shown in Figure 1. The access transistors M5 and M6 are connected to the Word Line. Where, Word Line is high for read/write operation. The cross-coupled latch constitutes the storage part and Access transistors are accustomed to move towards the outside. The bit line and bit line bar take action as I/O buses to sense the data through amplifier [4][5].

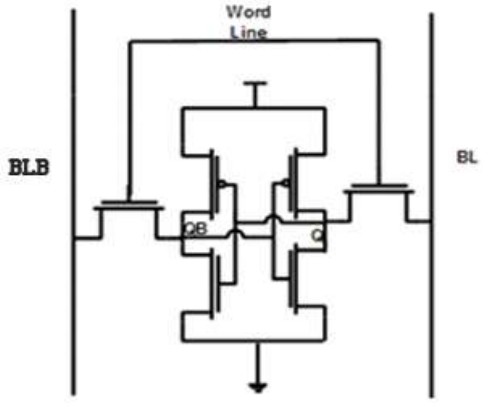


**Figure1.** Conventional 6T SRAM cell

### *2.2 7T SRAM Cell*

The 7T SRAM cell [6] is shown in Fig. 2. Write and read operation take place individually. Write operation in 7T SRAM cell take place alike to 6T SRAM cell. Reading operation happen when read signal (RWL) is 1 and write signal is 0. In this design of SRAM cell NM2 node provides a higher possibility of the outline of Tdischarge and Tfalchllp to be lesser than the Tll'f. Hence, write-ability of the 7T SRAM cell higher than the conventional 6T-SRAM cell [6].

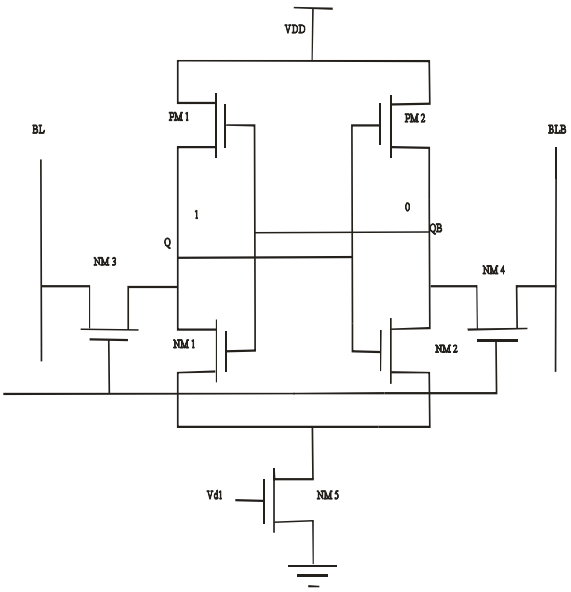


**Figure2. 7T SRAM Cell**

### *2.3 9T SRAM Cell*

The 9T SRAM cell [7] is shown in Fig. 2. Write and read operation take place separately. Write operation in 9T SRAM cell occurs like to 6T SRAM cell where N1, N2, P1 and P2 take place in the operation. Reading operation happen when RD going '1' (high) and access N7 transistor. This 9T SRAM cell has a disadvantage of high bit line capacitance on the bit line of SRAM cell.

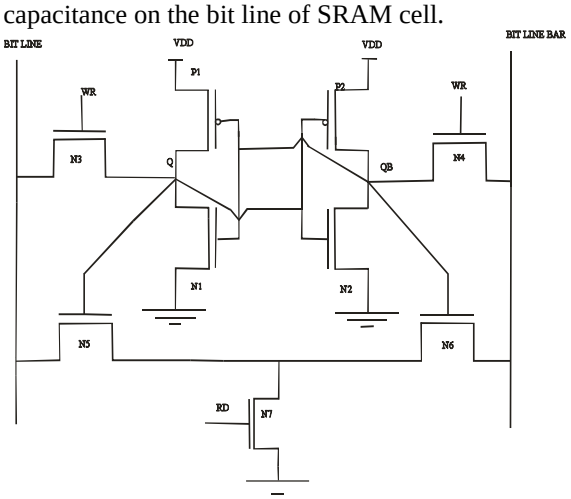


**Figure3**. 9T SRAM cell

### *2.5Drowsy Cache Method (Proposed Technique)*

The proposed drowsy cache technique in 6T SRAM cell has been constructing with the help of PMOS and NMOS transistor shown in Figure 4. Both PMOS and NMOS transistor is used to give positive feedback and they are used to decrease leakage current compare to other SRAM cell structures [8]. The read, write and hold operation simulation result has been discussed.

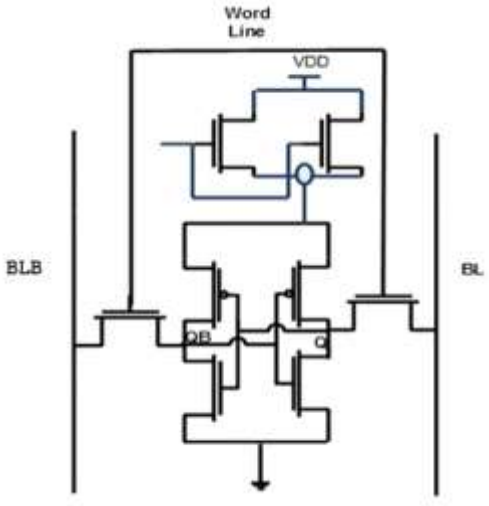


**Figure4.** Proposed 12T SRAM cell

## 3. Experimental results

In this section, stability, read delay, write delay, $I_{ON}/I_{OFF}$, leakage current and power dissipation has been analysis for different topologies of SRAM cells. All parameter are calculated in 0.9v power

supply. Every outcome is measured in spice simulator at 32 nm technology [9]. Figure 5 show the simulation result of N-curve of Conventional 6T SRAM cell for analysis read/write stability. Measurement of write ability of 6T, 7T, 9T and proposed design technique is shown in Table1. Similarly simulation results of Conventional 6T, 9T, 10T, 11T and proposed drowsy cache technique in read/ write delay, leakage, power dissipation and $I_{ON}/I_{OFF}$ are show in respectively.

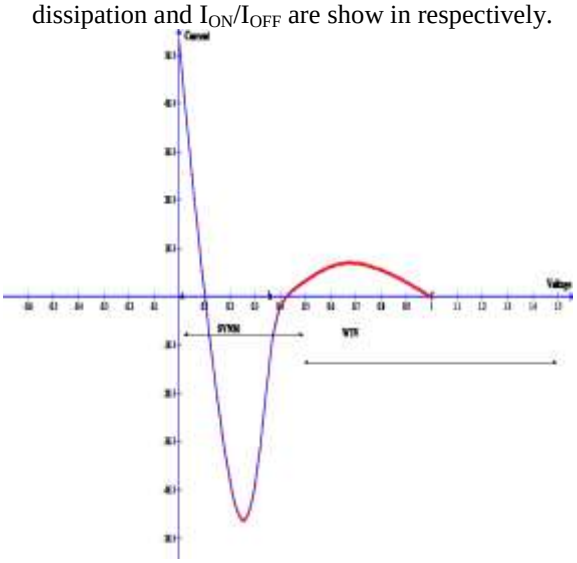

**Figure5.** Write, Read and Hold waveforms of proposed 12T SRAM cell

### *3.1 Read Delay*

Read delay is the hold-up occupied in allowing the bit lines to discharge by about 10 percent of the peak value or the hold-up between the function of the WL signal and the reply time of the sense amplifier. Read delay of proposed drowsy cache technique is minimum compare to 7T and 9T SRAM cell and equal to conventional 6T SRAM cell assuming '1' initially value in supply voltage shown in figure 6 [3].

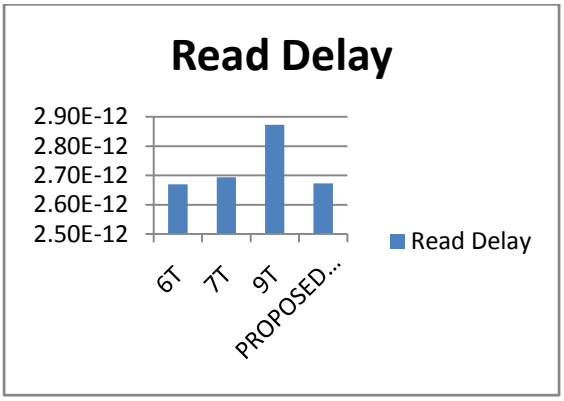


**Figure6.** Comparative value of Read Delay of SRAM cell

### *3.2 Write Delay*

Write delay is the delay between the functions of the word line signal and the point in time at which the data is actually written. The proposed drowsy cache technique is lower compare to conventional 6T, 7T and 9T SRAM cell assuming '0' initially value in supply voltage shown in figure 7 [10].

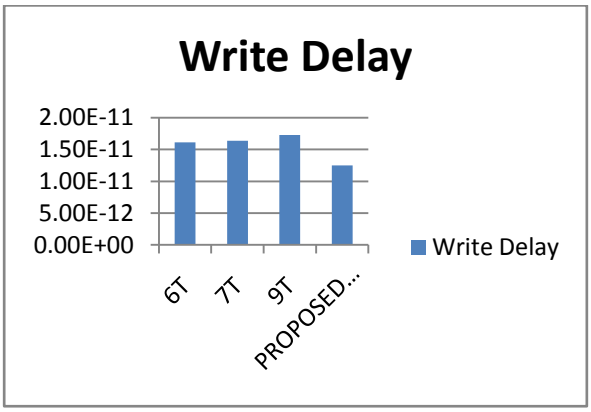


**Figure7.** Comparative of value Write Delay of SRAM cell

### *3.3 Leakage Current*

Leakage current is occurred in standby mode. The Leakage current is the current leak through transistors in SRAM cell. The sub-threshold current is main source of leakage current compare to gate and drain current. Leakage current is creates large power dissipation in SRAM cell. Practically leakage current create drawback in SRAM cell performance mainly during hold operation [11]. The proposed drowsy cache technique showing minimum leakage current compare to conventional 6T, 7T and 9T SRAM cell. This technique is working effectively in performance of 6T SRAM cell shown in figure 8.

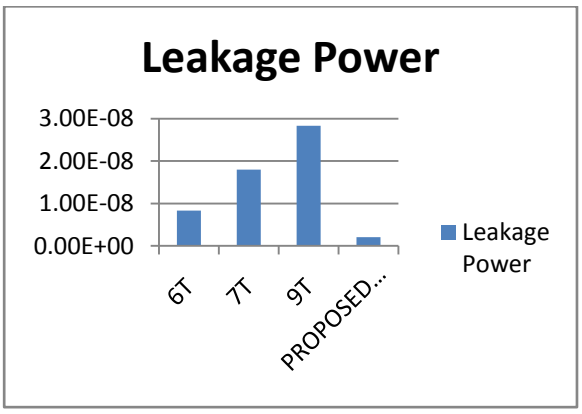


**Figure8.** Comparative value of Leakage Current of SRAM cell

### *3.4 Power Dissipation*

Power dissipation is grouping of static and dynamic power dissipation. Static power dissipation is a major aspect of the overall power dissipation. Static dissipation is the power dissipated in a SRAM cell in the lack of any switching action and is defined as the result of supply voltage and leakage current [12]. The proposed drowsy cache technique showing minimum power dissipation compare to conventional 6T, 7T and 9T SRAM cell shown in figure 9.

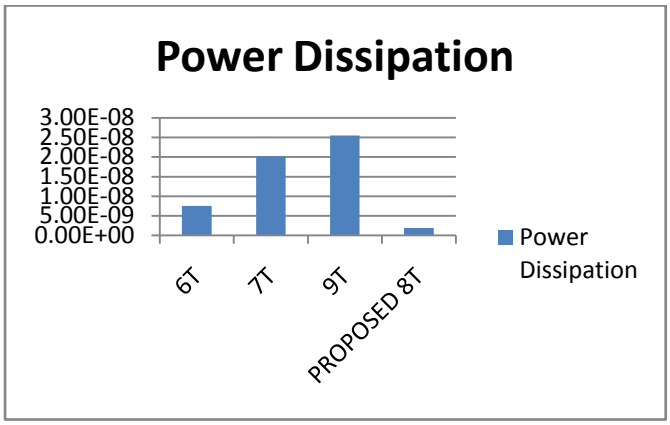


**Figure9.** Comparative value of Power Dissipation of SRAM cell

### *3.5 $I_{ON}/I_{OFF}$ Ratio*

$I_{ON}$ current is drain current of access transistor and $I_{OFF}$ current is leakage current in SRAM cell topology. So, $I_{ON}/I_{OFF}$ ratio shows the convenience of NMOS and PMOS transistor [13]. Here, The proposed drowsy cache technique showing higher $I_{ON}/I_{OFF}$ ratio compare to conventional 6T SRAM cell and equal to 7T and 9T SRAM cell shown in figure 10.

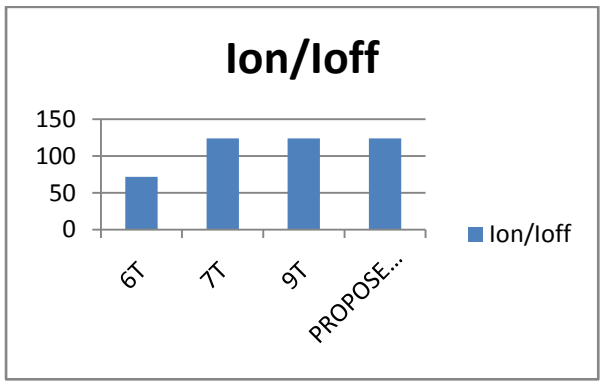


**Figure10.** Comparative value of $I_{ON}/I_{OFF}$ Ratio of SRAM cell

**Table1.** Comparative table of Read Delay, Write Delay, $I_{ON}/I_{OFF}$ Ratio, Leakage power of SRAM cell

| CELL / PARAMETER | Conventional 6T SRAM cell | 7T SRAM cell [5] | 9T SRAM cell [6] | Proposed Technique |
|---|---|---|---|---|
| Leakage power | 8.32 E-09 | 17.991 E-09 | 2.83E-06 | 2.04E-09 |
| Power Dissipation | 7.48E-09 | 1.0162E-06 | 2.55E-06 | 1.89E-09 |
| Write Stability | 2.204E-06 | 7.7E-07 | 7.3196 E-06 | 6E-08 |

## 4. Conclusion

In this work, we propose a technique to achieve low leakage current. Simulate result with conventional 6T, 7T, 9T SRAM cell with spice simulator. The proposed technique improved read stability, read delay, $I_{ON}/I_{OFF}$ , leakage current and power dissipation compare to conventional 6T, 7T, 9T SRAM cell at 0.9 v. Also proposed method reduced leakage current remarkable compare to conventional 6T SRAM cell. Simulation and analysing performance of Proposed SRAM cell at 32nm technology.

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