A Darlington Pair Based CMOS Two Stage Operational Amplifier at 32nm Technology

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ABSTRACT
The low power chip designing is a field of immense interest to the technology for electronics chip designing industries. Operational amplifiers (Op-Amps) are an integral parts of many analog and mixed signal systems. There is need to investigate the performance of the forthcoming scaled channel length CMOS devices. In this work a two stage CMOS Operational Amplifier with gain boosting technique, Darlington pair is proposed. The proposed Op-Amp shows high gain as well as high CMRR with reduced leakage current and power supply. This amplifier is highly useful for wireless communication because of low power consumption, high bandwidth, high gain and high CMRR. The designed operational amplifier gain is 93 dB, Unity-Gain Bandwidth is 538 MHz, CMRR is 100dB, slew rate is 20.13V/µS, power dissipation is 10pW, leakage current is 2.17pA, phase margin is 86º, and settling time is 95ns. The designed circuit is simulated using H-Spice tool at 32nm technology.

Keywords: *Two Stage CMOS Operational Amplifier, Spice Tool, Darlington Pair, Gain, CMRR, Leakage Current, and Power Dissipation.*

1. INTRODUCTION

The operational amplifier has turned into of the bulk versatile and imperative building blocks in analog electronics. Op-Amp plays essential role in analog circuit design as logic gate plays in digital circuitry [1]. Op-Amps are the staple elements in analog processing systems. Operational Amplifiers have been used by control engineers for many decades as crucial components in analog computers, and all integrated circuits etc [2], [3]. They are still one of the most staples of electronic elements in the world. Operational amplifiers are used in arithmetic operations like summation, multiplication, integration, division etc. With diminished channel length devices the designing of operational amplifiers poses new challenges in low power applications. Analog devices based on transistors conducting in the sub-threshold region consumes lesser energy for active process and dissipates lesser leakage power than higher voltage alternatives but conduct more gradually [4]. Two stage Op-Amps are the common preferred for low voltage operations [5]. Op-Amps along with immense open loop gain and unity gain frequency are needed in order to fit both fast settling requirements and accuracy [6].

The performance of Op-Amp in integrated circuits affects overall performance of the system, thus the leakage current and power consumption of Op-Amp need to be minimized. It is important to design the high performance integrated circuits along with the dogged trend toward decreased supply voltage [7]. In this work, we assumed optimum design, process variation and scrutiny of low-power, low-voltage CMOS two stage Operational Amplifier.

Several architectures of operational amplifiers and Darlington pairs have been described [3].

The CMOS technology is downscales day by day to limit power consumption, leakage current and other parameters of integrated circuits and devices [8]. The current demands of any IC technology are low cost, robustness, flexibility, portability, high noise immunity, high package density, high performance, high integration etc. For this ambition CMOS technology is a good candidate. The CMOS technology provides the flexibility of device scaling. The advantage of scaling MOS transistors are – increased device packing density, improved frequency response, increased current driving capability. There are also some conflicting effects of reducing channel length such as- reduced mobility of carriers, drain induced barrier lowering, punch through, at higher electric fields normally encountered in small channel length deices due to velocity saturation effects.

The objectives of the proposed design are to achieve a high gain and high CMRR with low power consumption.

1.1 Designing of two stage CMOS Op-Amp

Op-Amps are one of the important and basic devices which have broad applications in so many analog circuits like algorithmic, switched capacitor filters, ∑Δ A/D converter, sample and hold amplifiers, pipelined converter etc [9].

1.2 Conventional Two Stage CMOS Op-Amp

Fig. 1 illustrates the block diagram of CMOS two stage Op-Amp with an output buffer which consists mainly four sections: Input Differential Amplifier, Compensation Circuitry, High Gain Stage, and Bias Circuit. At first, two inputs are provided to input differential amplifier and this section provides good part of overall gain to improve offset performance and noise. Then the high gain stage circuit section allows maximum output swing. The compensation circuitry is used to maintain the stability of overall circuit. To establish a proper operating point for each transistor the bias circuitry is used.

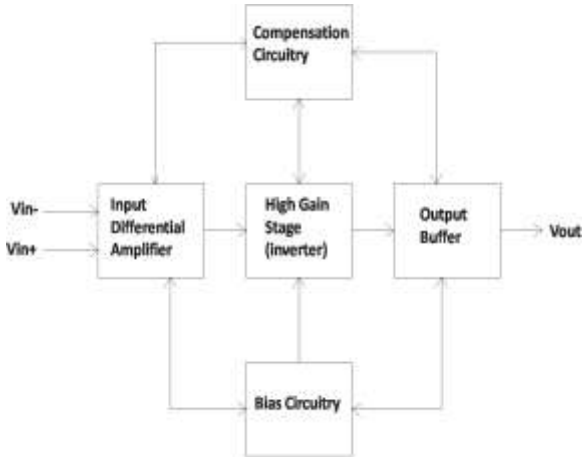

Figure 1. Block diagram of two stage CMOS Op-Amp.

Simplified Block diagram of Two Stage CMOS Op-Amp is described in fig. 2 which composite in three sections: Input Differential Stage, Second Gain Stage and Output Buffer Stage. Compensation Circuit is used to fill the loss of the overall circuit, thus this circuit is not required in some architecture, so this block is not considered.

1.3 Schematic of Conventional Two Stage CMOS Op-Amp

The schematic design of conventional Two Stage CMOS Op-Amp described in fig. 3. In this, transistors M1, M2, M3 and M4 constitute the first stage of the operational amplifier that is differential amplifier. The overall DC gain of the circuit is calculated on the output resistance of NMOS and PMOS transistors as well as. The gain of this differential amplifier is written as

$$| AV | = g(m_{1,2})(r_{on} r_{op}) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots$$

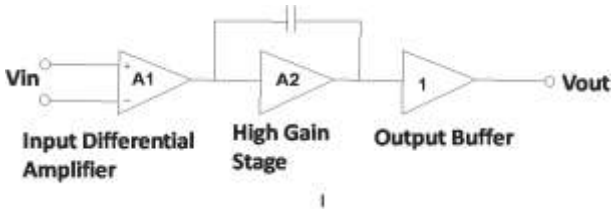

Figure 2. Simplified Block diagram of Two-Stage CMOS Op-Amp.

Where $g(m_{1,2})$ is the transconductance of transistor of M1 and M2. r_{op} is the output resistance of differential amplifier of two stage CMOS Op-Amp.

M1 and M2 operate in weak inversion [10] Transistors M6 and M7 form the second gain stage, which gives additional gain to the device. Transistor M8 and a reference current source make a simple current mirror biasing network that provides a voltage betwixt source and gate of M5 and M7.

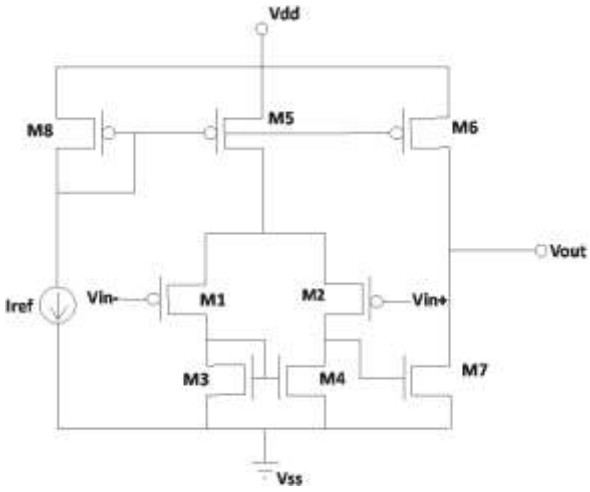

Figure 3. Pull-up diagram of two stage CMOS Op-Amp.

2. DARLINGTON PAIR (PROPOSED DESIGN)

In recent times the increasing the requirement of Darlington devices for the high data rate communication system [11]. Where a high signal is required at particular low frequency along with high selectivity for present-day professional application high gain and high bandwidth is required Darlington topology and Darlington cell [12].

The Darlington pair based two stage CMOS operational amplifier is shown in figure 4. In this, use of biasing current source I_{BIAS} is to establish the quiescent DC operating current in the Darlington pair transistor D1, this current source may be absent in some circuits or may be replaced by a resistor. The Darlington pair of these configurations, the effect of transistor D1 is to enhance the current gain through the stage and to enhance the input resistance. For the ambition of the low-frequency, small-signal scrutiny of circuits, the two transistors D1 and D2 can be consider as a single composite Transistor, as illustrated in fig 4. The small-signal identical circuit of this composite device is shown in figure 5, assuming that the effects of the r_o of D1 are negligible. We will now calculate effective values for the g_m and r_o of the composite device. M10 and M11 used as a biasing circuit for Darlington pair.

$$GB = \frac{g_{m7}}{C_{gs6,7}} \quad \text{.....(2)}$$

Where GB= Gain Bandwidth
G_m= Transconductance
C_{gs}= Gate to Source capacitance
However, a dominant shortcoming confronted along with its performance. At peak frequencies its feedback turns into weaker than that of a single transistor amplifier. To overthrown this dilemma, so many modifications are applied in Darlington pair amplifiers either by including some additional biasing resistances in the device or by applying Triple Darlington topology the previous published Darlington amplifiers [13]. In this work, a transparent circuitry high performance two stage CMOS operational amplifier at 32 nm channel length MOSFET Darlington configuration is proposed. The designed amplifier used small channel-length (32 nm) to beaten the problems in consumption power, control in bandwidth, and leakage current. The diminish channel length will reduce the threshold value of MOSFETs and capable the designer to use value of small supply current and voltage.

3. SIMULATION & RESULTS

The presented circuit is simulated at 32nm technology with the help of Spice tool. Channel length of each transistor is 32mn. The Op-Amp operates at low supply voltage of 1V at room temperature. Simulation result is presented in table 1. From table 1, it can be seen easily that leakage current and power consumption are significantly reduced in the proposed design circuit. Unity-Gain Bandwidth is increased up to 300MHz. Gain is also increased by 30dB. The simulation result of the operational amplifier concluded in 93dB DC gain, 100dB CMRR, 538MHz Unity Gain Bandwidth, 95ns settling time, leakage current is of only 2.17pA, 86º degree phase margin, and 20.13V/µS slew rate.

3.1 Approximation of power dissipation

Now-a-days the difficulty of power as well as heat dissipation expands to the Op-Amp design, which conventionally has represented low costs and low power densities. The transient response of power consumption versus time for conventional Op- Amp is shown in figure 6.In CMOS, process, power dissipation can be characterized into two categories: dynamic and static power dissipation i.e.

$$P_{total} = P_{static} + P_{dynamic} \quad (3)$$

Table 1 .Performance summary and comparison to conventional two stage CMOS Op-Amp.

Performance Parameters	Conventional Op-Amp	Proposed Op-Amp
Supply Voltage (V)	1	1
Technology (nm)	180	32
Gain (dB)	63.8	93
CMRR (dB)	83.7	100
UGB (MHz)	110	538
Power Dissipation (pW)	18.4	10
Slew Rate (V/µS)	12.78	21
Settling Time (nS)	-	95
Leakage Current (pA)	-	2.17
Phase Margin (degree)	66.5	86
Note L = 32 nm (for all transistors)		

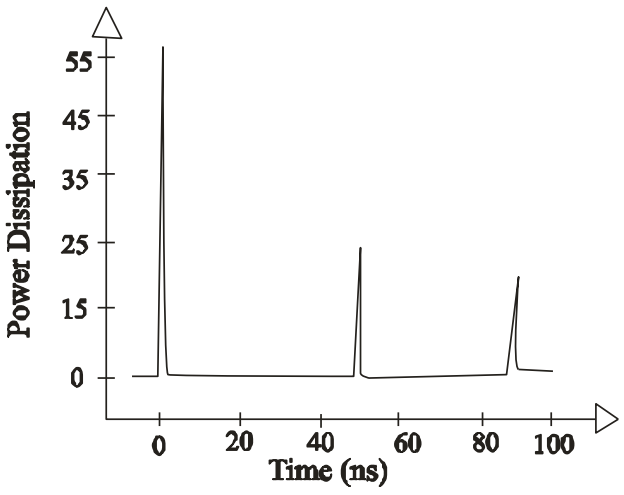

Figure 6 Response of Power vs. Time for Conventional Two-Stage Op-Amp.

Where P_{total} is the total power dissipation, P_{static} static is the static power dissipation and $P_{dynamic}$ is the dynamic power dissipation. Intuitively, static power is an important design consideration for low power battery operated or portable devices. Static power is due to the leakage current, which flows when the transistor is in off state or standby mode. On the other hand, dynamic power dissipation is the power dissipated when the device is in active mode. Dynamic power is due to transistor switching and so it depends on switching rate [14].

3.2 Approximation of DC Gain

Normally, gain is defined as the ratio of the output of that device. It is required to have high open loop gain along with wide frequency response, and in the same time high output swing especially in low voltage applications where signal to noise ratio is an important factor [15]. The response for gain versus frequency is shown in figure 7.

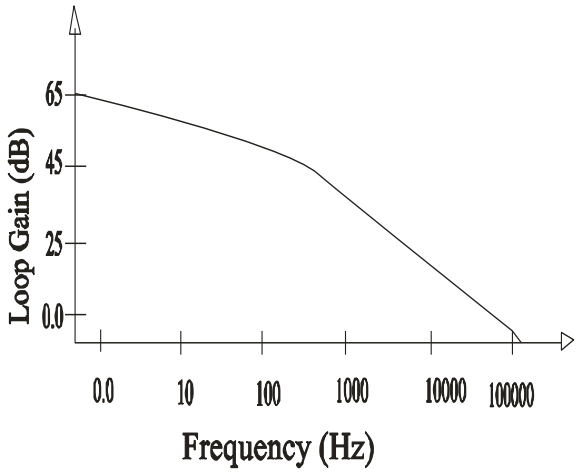

Figure 7. Response of Loop Gain vs. Frequency for Conventional Two-stage Op-Amp.

3.3 Approximation of slew rate

One of the most important parameter of an Op-Amp is the "slew rate", it defines the rate at which the output voltage change. The transient analysis shown in figure 8 has been carried out to perform the slew rate simulation. **T**he term leakage means an unwanted parameter which has never been desired to be exhibited by the device, however comes into picture while operation. The figure illustrates the response between leakage current for conventional two-stage Op-Amp.

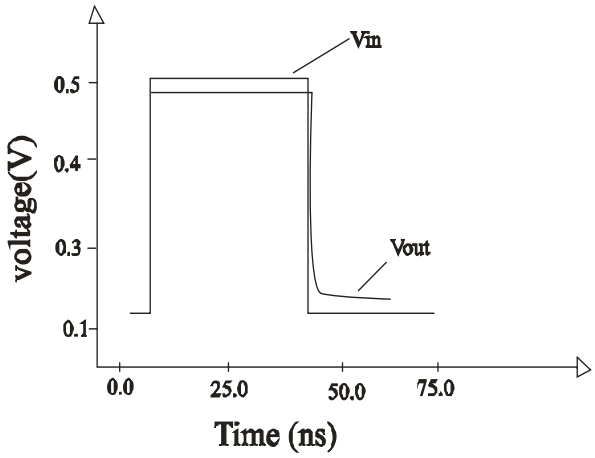

Figure 8. Transient Response of Voltage vs. Time Showing Slew Rate for Two-Stage Op-Amp

3.4 Approximation of leakage current

The term leakage means an unwanted parameter which has never been desired to be exhibited by the device, however still comes into picture while operation. Figure 9 illustrates the response between leakage current and time for conventional two-stage Op-Amp.

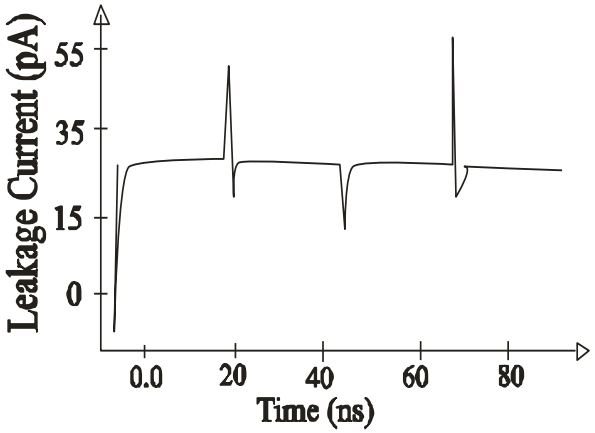

Figure 9 Transient Response of Leakage current vs. Time for Conventional two-Stage.

4. CONCLUSION

The design of Darlington pair based two stage CMOS amplifier has been discussed and simulated at 32nm technology. In this paper, a modern access has been granted for designing immense gain amplifiers and outcome of the designed Op-Amp is a high FOM with immoderate power consumption of 10pW.

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