A Survey on Low-Power High Speed Full Adder Circuit in DSM Technology

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Abstract:- *Adders are one of the most basic building blocks in digital components present in the Arithmetic Logic Unit (ALU) .the performance of an adder have a significant impact on the overall performance of a digital system. The existing design is compared with some existing designs for power consumption, delay, PDP at various frequencies viz 10 MHz and 300 MHz. the simulations are carried out on HSPICE by using CMOS technology and the simulation results are analyzed to verify the superiority of the design over the existing designs. Maximum saving of power delay product is at low frequency of circuit is 96.8% with respect to C-CMOS and significant improvement is observed at other frequencies also. The power consumption increases at a slow rate in comparison to other adders with increase in frequency. In this paper we study about various adder circuit and find the merits and demerits of the adder circuit for further development of adder circuit which consume low power and area.*

Keywords (Size 10 & Bold) — *Low power, GDI, SERF, Hybrid adder*

I. INTRODUCTION

Efficiency of implementation of arithmetic circuits in the execution of dedicated algorithms such as digital filtering, correlation and convolution largely affects the performance of application specific integrated circuits and digital signal processors. The increasing density of transistors hence complexity in the integrated circuits demands for high speed, power efficient designs. The researchers over the time have developed numerous CMOS Logic styles to meet the requirement of the rapidly growing industry. Lowering the supply voltage is a means of reducing the power consumption of the circuit in ultra deep submicron technology but it results in degraded driving capability and increased circuit delay of the designed cells.

Full adder proves to be the most fundamental circuit employed in many complex arithmetic operations such as addition, subtraction, division, multiplication, exponentiation etc [1], [2]. Adder circuit must have a fast carry generation mechanism because the critical path in the above mentioned applications generally goes along the entire carry-in to carry-out path of the full adders. Slower carry-out generation results as increase in worst case delay and glitches in the later stages, which leads to higher power consumption. The full adder circuit also demands for simultaneous generation of the sum and carry output to reduce glitches in the lower stages of the full adder. The rapid increase in demand of portable battery operated devices has urged for low power and high speed devices and various logic styles have been developed over the years to fulfill these goals. The most basic design is the conventional static CMOS full adder[3,4] which comprises of a regular CMOS structure. The adder provides full voltage swing output with good driving capability owing to the conventional pull up and pull down transistors structure. The large number of PMOS transistors used in the design result in high input capacitance, declined speed and more area. Complementary transistor logic(CPL) is another conventional design which provides full voltage swing and good driving capability at high speed with increased number of internal nodes and transistors, Although this increases the power dissipation in the circuit [5]. Another modern design technique is the GDI (gate diffusion input) technique. the adders based on GDI technique utilize a regular GDI cell structure to carry out adder functionality. The primary disadvantage of the GDI adder is degraded voltage swing at the output which results in reduced driving capability [6,7].

In this paper a low power design for a single bit full adder circuit. The existing design gives very good performance at high speeds with satisfactory voltage swing at the output. The rest of the paper is organized as follows. The section II consist of the description of the previous work with their advantages and disadvantages. The sections III and conclusion respectively.

II. Literature Review of Full Adder Circuit Designs

Survey includes the different power optimization methods at various level of digital circuit design process from system level to physical level. Different sources responsible for power dissipation in CMOS circuits are also reviewed. Techniques to reduce the effect of such sources in different research articles are discussed here.

Reto Zimmermann and Wolfgang Fichtner*, 1997 *[1], Implemented a 32 bit adder using different logic styles. The CPL (Complementary Pass Transistor) technique which generate complemented outputs in same design like AND/NAND, OR/NOR and XOR/XNOR together. This is one form of pass transistor logic only. The advantages of CPL are high function design with less number of transistors and small input capacitances. But these advantages are partially undone because CPL needs additional swing restoration circuit and dual-rail encoding to improve its overall performance.

From this paper we have understand the working of the pass transistor logic on conventional gates which reduces the overall area of the circuit without degradation of the performance of the circuit we take the logic of pass transistor in upcoming research.

***Gustavo A. Ruiz,* 1998 [2],** Proposed a new generate signal (*N*) in differential logic to design a ripple carry (RC) adder, carry look ahead (CLA) adder and binary carry look ahead (BCL) adder. Mathematical expression for signal (*N*) has been derived in this paper. The signal is used to enable iterative shared transistor structures in adders. Use of new generate signal in differential cascode voltage switch logic achieves better speed and lower area than a conventional logic. Based on this signal, circuits for above mentioned 32-bit adders have been fabricated in a standard 1.0 µm two level metal CMOS technology.

In this paper we understand the scaling of the technology on CMOS transistor for building a n-bit transistor for achieving the high speed of the circuit without degradation of performance of the circuit we understand how to built a n-bit adders for making a complex designe.

***D. Markovic et. al.,* 2000 [3],** Developed a general synthesis method based on Karnaugh map. General rules of method are explained to synthesis logic gates in three forms of pass transistor logic such as CPL, DPL (Dual Pass transistor Logic) and DVL (Dual Value Logic). The method is applied to design two-input and three-input logic gates and it shows versatility with good efficiency.

Here this method is applied to design two-input and three-input logic gates and it shows versatility with good efficiency. In over research the method is efficiently synthesizing logic gates which have balanced loads on true and complementary input signals is taken into consedration.

***A. Morgenshtein, et. al.,* 2000 [4],** This overhead is caused by the additional pre-computation circuitry. On the other hand, a Shannon-based GDI design does not require a special pre-computation circuitry because of its particular MUX-like nature, so that most area overhead is eliminated [94]. The presented approach can be used in combination with existing cell library-based synthesis tools to achieve an optimized design.

In this Paper we make the MUX circuit with the help of GDI technique. We use the GDI technique to reduce the area and Power consumption for generating EXOR gate to get proper SUM operation in adder circuit.

***Kaushik Roy et. al.,* 2003, [5],** Reviewed all causes of leakage current in transistor that includes gate drain leakage, gate-oxide tunneling, drain-induced barrier lowering and weak inversion effect. They observed that the low threshold voltages, gate leakage and sub-threshold voltages are the dominant sources of leakage current in deep sub-micron meter devices. Effect of such sources will increase with technology scaling. The GIDL and BTBT (base to base tunneling) may also have a significant effect on advanced CMOS devices. The solution should be considered both at circuit level and process technology level in deep sub-micron meter CMOS circuits.

For calculation of various static power in the transistor when circuit is in ideal state we study this paper. In over paper all type of leakage is calculated with the help of this paper Low power with high speed – power consumption of CMOS is largely determined by switching power caused by charging and discharging of capacitances.

***Adarsh Kumar Agrawal et. al.,* 2009 [6],** Presented a design of full adder using Mixed Gate Diffusion Inputs topology based on static CMOS inverter. For this, in the long chain of full adders, the GDI full adders are followed by inverters to improve the performances with respect to conventional single full adder chain. The propagation delay, dynamic and leakage power dissipation can be optimized by changing the number of full adders between two consecutive inverters. HSPICE simulation using TSMC 0.35µm and 0.18µm CMOS technologies evaluated propagation delay and average power for minimum power design.

In this paper scaling of technology is discuses over power consumption of the circuit we use HSPICE tool for further reduction of power in GDI technique.

***Junbo Yu et. al.,* 2010 [7],** Proposed a two-stage thermal dependent leakage power minimization algorithm by using dual-V_{th} library during behavioral synthesis. Their experimental results shows an average of 17.8% saving in leakage power consumption and a slightly shorter runtime compared to the previous best known work.

In this paper for minimization of static power the threshold voltage can be change for mitigation of leakage power in DSM technology. In his paper we understand how to generate the High Vth transistor for reduction of leakage power in adder circuit.

***A.Bazzazi and B. Eskafi,* 2010 [8],** Proposed a 24 transistor one bit full adder using GDI based XOR – XNOR functions. The post layout simulation of adder with HSPICE tool at 0.18 µm CMOS technology shows great improvement in terms of power-delay product. The power dissipation is also very less as compared to other logic styles.

In this paper we have study how to make XOR and XNOR gate with the help of GDI technique for reduction of power, delay and area of the circuit. We use GDI adder for generating XOR and XNOR transistor in over research.

***Baliga, A., and Yagain, D.,* 2011 [9],** Designed a high speed, parallel-prefix adders such as Brent-Kung, Sklansky, Kogge-Stone and Ling adders, by Kogge-Stone implementation, using CMOS logic and transmission gate logic. The design and simulations are done using 130 nm deep sub micron technology file for 8, 16 and 32 bit adders. The power, area and delay for the two implementations are compared and it is found that the power, area and delay in the transmission gate logic are much lower than those in CMOS logic.

In this paper P-DTGAL buffer with large device sizes are inserted between power-clocks and virtual power-clocks of power-gating switches in transmission gate adiabatic logic circuits. We can use power gating technique for leakage reduction in CMOS adder circuit designe.

***T. Kalavathidevi and C. Venkatesh,* 2011 [10],** Implemented a Viterbi decoder using GDI cell at 0.25µm technology with 3.5V V_{dd} and a frequency of 25MHz. The outputs of the convolutional encoder designed for the constraint lengths K=4, 5, 6, 7 and rate ½ are fed to the designed Viterbi decoder. The comparison results showed 29% reduction in power consumption and 66% reduction in area by using GDI circuit than the CMOS circuit.

We do the Implementation of an 8-bit full adder with proposed scheme saves leakage power from 73.1% to 79.5% in 90 nm process and 82% to 89.6% in 45 nm process for clock rates ranging from 100 to 300MHz.

***Prathyusha Konduri and Magesh Kannan.P,* 2011 [11],** Shows the implementation of RAM in GDI technique and its simulation is done in 0.18µm TSMC technology with the supply voltage of 1.8V. Their result shows 16% reduction in power and 49% reduction in delay as compared with traditional CMOS technique.

In this research we use the better suited for large fan-in gates because each input connects to a single transistor, presenting a smaller load to the preceding gate. Reduced complexity of logic and hence, lower capacitance, and faster speed

***R.Uma and P. Dhavachelvan,* 2012 [12],** Introduced Modified Gate Diffusion Input (MGDI) Technique. They presented new design structure of basic digital gates using two transistors for AND, OR, XOR, NAND, NOR and XNOR gates. Design is compared with basic GDI technique. Implemented of MGDI technique to design 5 different topologies of full adder has been done using various Boolean equations.

The architecture can tolerate multiple defects across the logic gates of a CMOS logic circuit. It is shown that the technique imposes little delay overhead (less than 6%) but incurs power dissipation overhead (less than 20%) in the presence of defects.

***Eitan N. Shauly,* 2012 [13],** Presented a review paper that discusses the issues associated with transistor scaling and related solutions for leakage and power reduction in terms of topological design rules and layout optimization for digital and analog transistors.

In this paper reduce the transistor count for occupation of lesser area in the circuit by using transmission gate in DSM technology. This logic completely eliminates static currents and provides rail-to-rail swing.

***J.Sudhakar et. al.,* 2012 [14],** Reviewed various techniques to minimize power dissipation due to glitches in their paper. They conclude that by gate sizing, glitch transitions are reduced by 38.2 % on average, which results in the reduction of total transitions by 12.8 %. The power dissipation is reduced by 7.4 % on average and by 15.7 % maximum from the minimum-sized circuits.

In this paper we understand the sizing of the transistor for achieve proper logic and to reduce the further leakage power sizing of transistor is taken into consideration.

***Chiraz Khedhiri et. al.,* 2012 [15],** Presents a new differential logic unit with duplicated functional outputs. Outputs of logic functions with their complemented form are designed within a single logic unit cell. This requires fewer transistors with respect to traditional CMOS logic style. They designed one bit ALU (Arithmetic Logic Unit) that perform 8 logic operations with two control signals using only 16 transistors.

In this paper the BCL adder has high speed with increase in chip area. The shared transistor structure of CLA adder reduces the number of interconnection lines but it increases 20% area as compared to RC adder and average delay is also slightly greater than both adders

***Vahid Foroutan et. al.*, 2014 [16],** Presented two new symmetric designs for low- power, high speed full adder cells using GDI structure and hybrid CMOS logic style. The ULPD (Ultra Low- Power Diode) logic-level restorer is used in adders for full-voltage swing. The circuits are optimized for energy efficiency at 0.13 µm and 90 nm partially depleted (PD) SOI CMOS process technology. Simulations performed on HSPICE and the comparison with standard full adder cells shows excessive improvement in terms of Power, Area, Delay and Power-Delay-Product (PDP).

In this paper a new leakage reduction is introduce between PUN and PDN which increases the resistance of the circuit arrangement of the transistor is such a way that one of the transistor are always in cut-off region. We can increase resistance of the circuit.

***Partha Bhattacharyya, et. al.*, 2015 [17],** In this paper, a hybrid 1-bit full adder designemploying both complementary metal–oxide–semiconductor (CMOS) logic and transmission gate logic is reported. The design was first implemented for 1 bit and then extended for 32 bit also. The circuit was implemented using Cadence Virtuoso tools in 180- and 90-nm technology.

In this paper the detail methodology of GDI is explained. Here we explained few research findings about GDI technique and implemented in over work. Simulations of basic GDI gates under process and temperature corners in 40nm CMOS achieves 70% leakage and 50% active power reduction while having the same delay as compared to CMOS.

OBJECTIVES OF THE RESEARCH

With shrinking technology reducing power consumption and over all power management on chip are the key challenges below 100nm due to increased complexity. For many designs, optimization of power is important as timing due to the need to reduce package cost and extended battery life. Power optimization is possible at each level of design process from higher architecture level to lower physical level. At the circuit level, optimization of power has a good impact on overall power dissipation of chip [2]. Hence, the objective of this research is also to find out the circuit/transistor level technique to design digital system which provides least power dissipation with less delay and less area compare to standard CMOS technique and other currently used techniques.

PROBLEM SPECIFICATIONS

From the literature survey, it is found that the three main sources of power dissipation in CMOS are: Static, Dynamic and Short Circuit power dissipation [14]. Static power dissipation occurs when the transistors are at steady state, either in ON state or in OFF state, whereas dynamic and short circuit power dissipation occurs during switching from one state to other state. Hence dynamic and short circuit power dissipation are jointly called switching power dissipation. The reasons for static or leakage power dissipation are leakage currents, reverse biased currents and substrate injection currents, which flow through the transistors in its steady states. Switching power dissipation arises due to the charging and discharging of output load capacitance during switching. Short- Circuit power dissipation is caused by currents flowing directly from supply to ground for a very short period of time when the p-device is being turned OFF and the n-device is being turned ON during switching.

Advantages

1. Simulation results of different digital circuits using proposed hybrid GDI technique shows improved performance as compared to other existing and standard techniques in terms of power, delay and area.

2. Real time implementation will surely give benefit for the design of fast processed and portable electronics devices. Design of portable computing, communication and multimedia devices such as laptops, palmtops, cell phones, cameras etc with proposed technique may give better result.

3. Hybrid GDI needs less number of transistors as compared to standard CMOS technique. Need of less transistors leads to low cost of device.

4. The basic gates like two-input AND, OR and XOR gates are designed using conventional standard CMOS technique, other parallel techniques such as PTL, TG and existing GDI technique. The GDI technique is emerging as a strong alternative of CMOS for digital circuit design but is suffers from low threshold drop problem.

5. The performances of such circuits are compared with the conventional static CMOS technique and GDI technique with swing restoration buffers. Comparison is done in terms of power, delay and number of transistors used in the circuit.

Disadvantage

1. Low power with high speed – power consumption of CMOS is largely determined by switching power caused by charging and discharging of capacitances. As the circuits get faster, the frequency goes up as does the power consumption.

2. Insensitive to device variations- Small size transistors allowed dense layout of circuit although interconnectivity limits the density.

3. Rail-to rail swing with $V_{OH} = V_{dd}$ and $V_{OL} = GND$

4. Degradation of logic level by using pass transistor. When noise does not exceed the margins, the gate eventually will settle to the correct logic level.

5. Robustness against voltage scaling and transistor sizing are main disadvantage of Adder circuit.

6. Number of transistors required to implement an N fan-in gate is 2N. This can results in a significant large implementation area.

7. Requires both nMOS and pMOS transistors on each input and pMOS transistors add significant capacitance with relatively large logical effort.

RESEARCH METHODOLOGY OVERVIEW

The reduction of the power dissipation and the improvement of the speed require optimizations at all levels of the design procedure. In this research, different circuit style and methodologies are analyzed. Several circuit design techniques are compared in order to find their efficiency in terms of speed and power dissipation. Each one has its own merits and demerits. Conventional static CMOS has been a technique of choice in most digital design. Alternatively, Pass Transistor Logic has been suggested for low power, high speed systems. The GDI cell is similar to a CMOS inverter structure. In a CMOS inverter, the supply voltage (V_{dd}) and the ground voltage (V_{ss}) are connected to the source of the pMOS and nMOS respectively whereas in a GDI cell it is not necessary to connect supply and ground voltage with MOS diffusions. There are few other differences between the two cells.

II. Adder Circuit

The hybrid logic design style involves the division of larger circuit into smaller sub-circuits and each sub-circuit is optimized using various logic design style. The hybrid design methodology for a full adder circuit is shown in Fig.1. As shown in the figure the full adder circuit is divided into three modules and these modules are designed using various different design styles to exploit the advantages of the different design styles and extract the desired performance. Module 1 produces XNOR and XOR functions of the inputs A and B [15,16]. the module1 can be either XNOR based or XOR based depending on the primary output generated within the module the primary output is utilized to get the other output using an inverter. Module 2 and Module 3 comprises of the circuitry to produce the desired sum and carry outputs of the full adder by utilizing the intermediate outputs generated by Module 1 circuit.

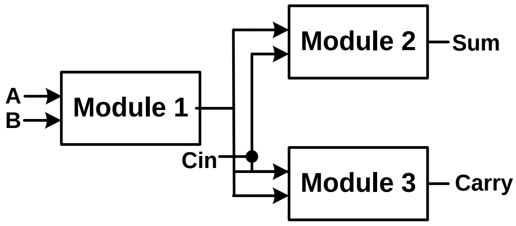

Fig. 1 Hybrid design methodology

In this paper a 13 transistor design of a single bit full adder based on Hybrid GDI logic design style. As the design suggests the adder circuit exploits the advantages of GDI technique, pass transistor technique and transmission gate technique to carryout excellent low power and high speed characteristics. In Further research we implement 8bit and 16bit full Adder.

III.CONCLUSION

Hybrid GDI full adder circuits give superior performance in terms of power consumption, propagation delay and Power Delay Product (PDP) than all the reference full adder circuits and the existing circuits are also free from the voltage degradation problem that existed for the most of the reference circuits. The comparison of adder with existing adder circuits shows that The XNOR based single bit full adder cell circuits produce reduction in power consumption a maximum of 86.8 % in comparison to the existing SERF adder, produces reduction in delay a maximum of 93.7 % in comparison to the SERF adder and a huge reduction in PDP a maximum of 99.2 %in comparison to SERF adder at 100 MHz frequency. Significant improvement in above mentioned parameters is achieved at higher frequencies also.

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