Implementation of Aging-Aware Multiplier Design for Area and Power Critical Applications

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ABSTRACT

The main constraint in VLSI system design is to achieve low power devices. In any digital filter, multipliers are the major elements. The throughput is the major parameter of multiplier that influences the performance of multiplier. For long term usage, aging becomes the main constraint that affects the performance of the system. Majorly aged systems fail due to delay problems. There are many approaches to design multipliers that reduce this aging effect. But these systems require large area, power. Moreover, timing violations occur when fixed latency designs are used.

For reducing these timing violations and for implementing an aging reliable low power multiplier, adaptive hold logic is used. The transistor speeds are influenced by both negative and positive bias temperatures, for long term applications due to aging effect, the system may fail to perform because of timing violations. Therefore, it is necessary to implement the high performance designs. Here we propose a reversible Wallace Tree multiplier design with razor flip flop based multiplier circuit. This design is able to provide high throughput for area power critical applications. The proposed method can be digital filters to enhance the performance in the real time environment.

KEYWORDS: AGING EFFECT, REVERSIBLE WALLACE TREE MULTIPLIER, RAZOR FLIPFLOPS, AHL.

1. INTRODUCTION

In performance circuits, multiplication operation is the one that which consumes more arithmetical operations. Based on the importance of multiplication operation, researchers deal with high speed multipliers with low power consumption. Any multiplication operation has two main basic operations as, generation of partial products and the other is to generate the sum of these partial products for obtaining actual result of the multiplier. For generating sum for the multiplier we have two methods as serial and parallel. The serial algorithm uses sequential circuits along with feedbacks, whereas the parallel multiplication algorithms are using combinational circuits and these structures never uses feedbacks.

Digital signal processing (DSP) systems the multiplier is one of the key hardware blocks. Multiplier plays a critical role in DSP like digital filtering, spectral analysis and digital communications multiplier plays an important role. The current DSP applications are being portable and becoming battery operated systems. The battery dependency making the device to low power designs. As the multiplier is a complex circuit complex and operates on the high frequency rates, this is becoming essential to reduce the multiplier design for obtaining the fruitful results.

Within the integrated circuits, the major topic to research is aging behavior of digital designs. Which makes a huge body of work that which address the aging effects at the hardware level. Optimization techniques that are resistant are the aging affect are produced by Wu and Marculescr. At chip level different processes variations are studied and characterized. The problems that are faced by the unreliable hardware are coped by the software, which includes the devising reliable aware instruction set, using appropriate instruction scheduling reliable aware compilation techniques. To maximize the lifetime of SoC, an allocation framework based on a heuristic are presented by Huang et al.

In this paper, time dependent dielectric breakdown (TDDB), electron migration (EM) and negative bias temperature instability (NBTI) these are considered as the hard errors are to be permanent. Hard intrinsic failures are researched over decades, in recent days it is again gaining interest and increasing

adverse effects with technology scaling. A life time reliable RAMP aging aware architecture is proposed by srinivasan et al. The structure aware lifetime reliable estimation framework is presented by Shin et al. the above two models are concentrated on the life time reliability os single core processor.

2. AGING AWARE MULTIPLIER

The aging reliable multiplier architecture consists of two n-bit inputs (n is a positive number), one 2n- bit output, one Wallace multiplier, 2n 1-bit Razor flip-flops, and an AHL circuit.

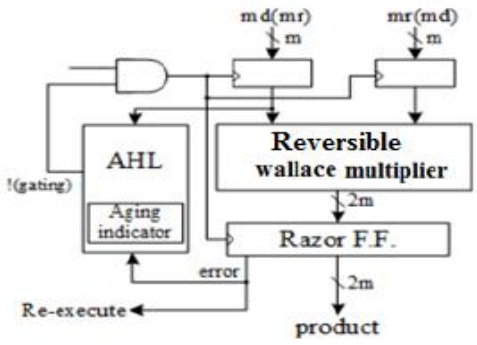
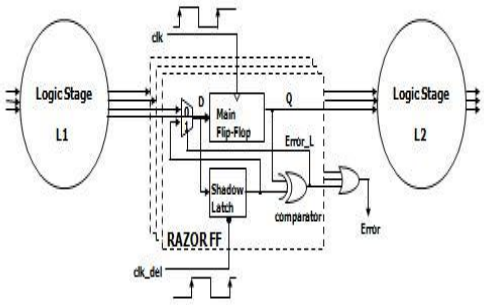


Fig.1: proposed aging aware multiplier.

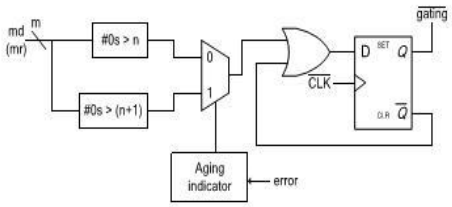
The input signals of the AHL in the architecture with Wallace multiplier which has a



multiplicand (md) and multiplier (mr).

Fig.2 Razor flip flop architecture.

Fig.3 Diagram of AHL (md means multiplicand mr means multiplier).



The timing violations that occur before and after the input pattern activities are detected by using Razor flip flop. A Razor flip flop mainly contains a shadow latch, XOR gate multiplexer and a main flip flop. The Razor flip flop and the shadow latch catches the execution results by using a combination logic with normal clock signal for main flip flop and a delayed clock signal for the shadow latch that which is slower than the normal clock signal. If the output of the main flip flop is different than the output of shadow latch, this indicates that the system has created the path delay, i.e. the clock cycle exceeds by one cycle period, and caches the wrong result. This produces a '1' or 'high' error signal indicating to re-execute the operation and informs the occurrence of error to the AHL circuit.

Fig.3: AHL block.

If the outputs of the main flip flop and the shadow latch are same then the result is executed within two clock cycles. Since the re-execution frequency is low, the overall cost of the system cost is not that much effective. In a variable latency aging aware multiplier the key element is the AHL block. The AHL block contains two judging blocks, aging indicator and a D-flip flop as shown in the fig.3. The performance degradation of the multiplier is indicated by the aging indicator. The aging indicator is nothing but a counter that which counts the number of errors in the razor flip-flop. For too small cycle periods, the Wallace multiplier cannot perform the operation successfully and produces timing violations. These timing violations are detected in the razor flip- flop and it generates error signals.

The second judging block allows smaller number of patterns than the first judging block. The second judging block requires more number of zeros in multiplier/ multiplicand. The results of both the judging blocks arrive at the multiplexer. The multiplexer output is decided by the aging indicator. The multiplexer output and the result are given to an OR gate, the output of D flip-flop is determined by Q^{-}. if the output of the multiplexer is one then the pattern requires one cycle.

The overall architecture flow of the aging aware multiplier is: the Wallace multiplier and the AHL executes simultaneously. The input patterns are decided by the AHL circuit based on the number of zeros in the multiplicand/ multiplier. The clock signal is disabled for the main flip flop when if the AHL requires two clock cycles. The output of AHL is 1 for other normal operations. When the Wallace

multiplier finishes its function, the result is sent to the Razor flip flop. Path delays and timing violations are taken care by the Razor flip-flop.the occurrence of the timing violations are the indicate that the cycle period is not sufficient to complete the current operation and the produced result is incorrect

URDHVATIR YAKBHAYAM MULTIPLICATION ALGORITHM

Ancient Indian mathematics contains a powerful multiplication algorithms based on the Urdhva Tiryakbhayam (UT) sutra. This sutra can be applied to any radix number as binary, decimal, and also for hexa-decimal numbers. Partial products are generated at first and then concurrent addition is performed. By using the Urdhva Tiryakbhayam the partial product generation and summation is done. In the UT process the multiplication process is independent on clock frequency so size of the multiplicand and the multiplier, and is not proportional to the input bit length. By this we have the flexibility of limiting the clock frequency. By using the lower frequency input clock rate the system dissipates less power and is energy efficient. When compared to the other conventional multipliers this method is advantages because the gate delay and area increases slowly.

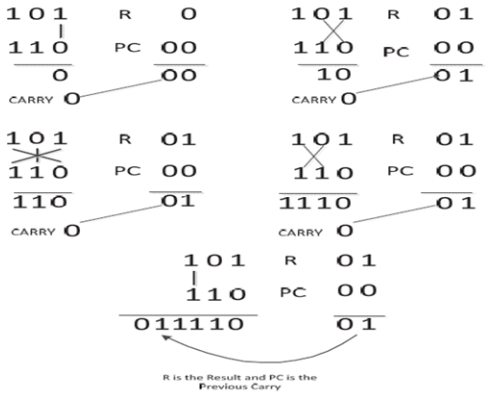


Fig.4 Urdhva Tiryakbhayam procedure for multiplication

DESIGN OF 4X4 URDHVA TIRYAKBHAYAM MULTIPLIER

The 2x2 UT multipliers are used or producing the 4x4 UT multiplier. This method reuses the system resources reducing the hardware consumption. The architecture of designing the 4x4 multiplier using 2x2 multiplier is as shown in below diagram.

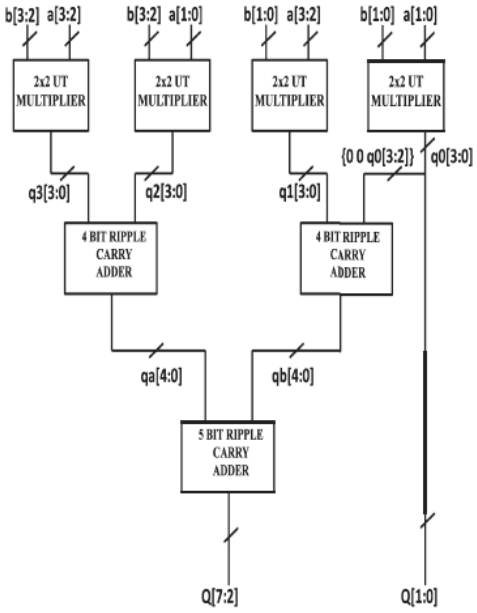


Fig.5: Design of 4x4 multiplier using 2x2 bit multiplier.

For the four bit RCA the inputs are the upper two bits and two zeros. From the second multiplier the other four bits are given to the RCA. This repeats for the another RCA from third and fourth multiplier. The results from this two RCA's are again summed by using 5-bit RCA. This sum is concatenated with the LSB of first 2x2 multiplier.

Adaptive hold Logic

In threshold circuits the main constraint is that to design high level performers that operate with very tight frequencies. in the current decade the recent mobile device battery is almost 60 % efficient than the conventional ones. The devices that are sub threshold ineffective are widely used. The performance conditions are dependent on process voltage and temperature conditions.

The conventional guard band methodology for worst case is no more efficient in present days. This new generation needs some adoptive technology that controls the performance of the devices is required. The track connect functionality is the most critical path for the replicated circuits. The original path and the replica path are the most confusing parts that which to be taken very clearly noticed. For addressing this issue, there were different adaptive techniques.

3. WALLACE TREE MULTIPLIER DESIGN USING REVERSIBLE ARCHITECTUE

The Intel co-founder, Gordon Moore stated that for every 18 months the performance of integrated circuits improves at an exponential rate with performance per unit cost increasing by a factor of 2, which results in reducing the dimensions on integrated structures that can operate at high speeds for the same unit area used before. There is a fundamental event that has to be considered is the quantum energy that is associated with every elementary events with minimized fundamental limit. Here the question arising is, Moore's law going to end? Because of using more and more the present day components are being very compact and the a large number of components are getting packed onto a chip, where power dissipation is being very high in present day electronic devices. The main condition in present day is to reduce this power consumption. The zero information loss and low power dissipation is achieved by Reversible logic gates.

The essential property in future circuit designs is the reversibility. Reversible logic circuits are different from the conventional logic gates. At first, fan-on doesn't exist in reversible logic gates. The input patterns are permutated, and the functions are realized by the reversible gates. For the reversible gates and circuits, the inputs are meant be as the constant inputs and the outputs are not considered as the primary outputs, are called as garbage and the inputs are termed as constant inputs. Let us consider the reversible logic circuit has k inputs then contain it will have k- outputs ie. The reversible gates have k x k input and outputs.

REVERSIBLE LOGIC GATES:

The reversible gates are one to one mapping devices i.e. they have n-inputs and n-outputs. The main application of reversible gates is that the inputs can be regenerated based on the outputs.fan out is not allowed in the synthesis of reversible logic gates. Therefore the fan-out in reversible logic gates is achieved by using additional circuitry. By using minimum number of reversible logic gates the reversible circuit is designed.

Peres Gate: This gate contains 3 inputs and 3 outputs which are nothing but A,B,C and P,Q,R.

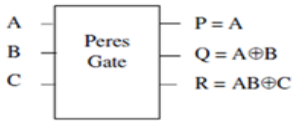


Fig.6 Block diagram of Peres gate

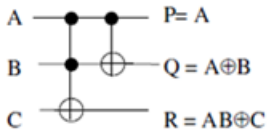


Fig.7 Symbol of Peres gate

CNOT GATE

CNOT gate is also known as controlled-not gate. It is a 2*2 reversible gate. The CNOT gate can be described as:

Iv = (A, B) ; Ov = (P= A, Q= A B)

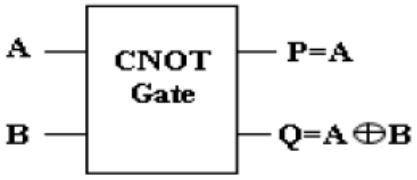


Fig.8: Block diagram of CNOT gate

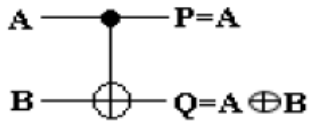


Fig.9: Symbol of CNOT gate

Implementation of Wallace Tree Multiplier

Wallace multipliers are implemented by using simple combinational logic circuits like half adder and full adders. These are fast efficient method for implementing the Wallace tree multiplier. Thus it consist of simple add multiply operations on binary integers. There is no concept of carry propagation the method is fast then the conventional multipliers and adders. The conventional multipliers produce ROM lookup tables. In the shift-add method, the time consumed for calculating the products increases linearly with the number of bits, the size of the RAM increases exponentially along with the operands.

The benefit of the Wallace tree is that there are only O (log n) reduction layers, and each layer has O (1) propagation delay. As making the partial products is O (1) and the final addition is O (log n), the multiplication is only O (log n), not much slower than addition (however, much more expensive in the gate count). Naively adding partial products with

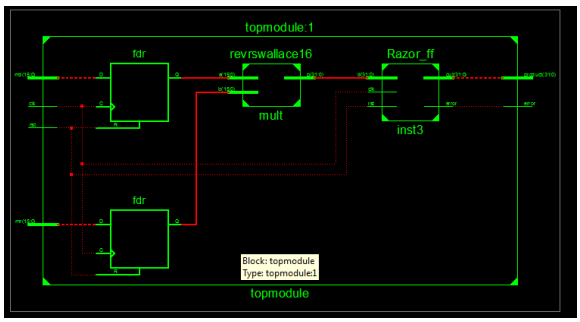
regular adders would require O ($\log^2$ n)time. From a complexity theoretic perspective, the Wallace tree algorithm puts multiplication in the class NC.

The figure below shows how a Wallace Tree Multiplier can be realized for the 8-bit i.e. an 8x8 multiplier.

Fig.10: Figure Example of reduction on 8x8 multiplier

4. RESULTS and DISCUSSION

RTL SCHEMATIC FOR THE TOP MODULE:

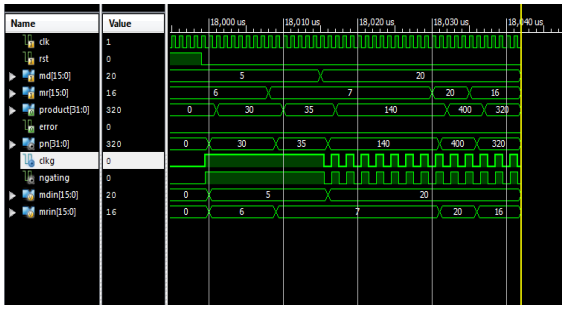


The RTL SCHEMATIC gives the information about the user view of the design. The internal blocks contains the basic gate representation of the logic. This basic gate realization is purely depend upon the corresponding FPGA selection and the internal database information.

OUTPUT WAVE FORM FOR THE TOP MODULE:

METHOD	AREA (In terms of LUT's)	POWER (mw)	Delay (ns)
Urdhva Tiryakbhayam multiplier(16-bit)	986	74.936	20.397
Wallace Tree multiplier(16-bit)	662	50.312	21.639

Table 1:comparision between urdhva tiryakbhayam and reversible wallace multiplier.



In the waveform which is shown above, clk signal represents clock, rst signal represents reset, md represents multiplicand, mr represents multiplier which we are applying as inputs to the design. Similarly product is the output signal for the design. Here clock signal is generated for the positive edge. Initially the reset signal should be force to logic 1 and after one clock cycle made it to logic 0 for performing the corresponding functional operation. To obtain the required outputs force the inputs logic with the required values. The output products get the multiplicity value of the applied inputs md and mr.

Table1: Comparision between existing Urdhva Tiryakbhayam multiplier and proposed reversible Wallace Tree multiplier Aging aware design.

From the above table the power and area is less for the proposed Aging aware reversible Wallace Tree

multiplier than the existing Aging aware Urdhva Tiryakbhayam multiplier.

5. CONCLUSION

Aging problem of transistors has a significant effect on performance of these systems and in long term, the system may fail due to delay problems, which can be reduced by using over-design approaches**.** This paper proposed an aging-aware variable-latency multiplier design with the AHL. The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. The experimental results show that our proposed architecture with 16x16 multiplication using Wallace multiplication approach. It is area and power efficient design compared to the existing Urdhva Tiryakbhayam multiplier. The Verilog language is used for coding. The synthesis and simulation is carried out using Xilinx ISE 12.3i.

6. REFERENCES

[1] Y. Cao. (2013). *Predictive Technology Model (PTM) and NBTI Model* [Online]. Available: http://www.eas.asu.edu/~ptm

[2] S. Zafar*et al.*, "A comparative study of NBTI and PBTI (charge trapping) in SiO2/HfO2 stacks with FUSI, TiN, Re gates," in *Proc.IEEESymp. VLSI Technol. Dig. Tech. Papers*, 2006, pp. 23–25.

[3] S. Zafar, A. Kumar, E. Gusev, and E. Cartier, "Threshold voltage instabilities in high-k gate dielectric stacks," *IEEE Trans. Device Mater.Rel.*, vol. 5, no. 1, pp. 45–64, Mar. 2005.

[4] H.-I. Yang, S.-C.Yang, W. Hwang, and C.-T. Chuang, "Impacts of NBTI/PBTI on timing control circuits and degradation tolerant design in nanoscale CMOS SRAM," *IEEE Trans. Circuit Syst.*, vol. 58, no. 6, pp. 1239–1251, Jun. 2011.

[5] R. Vattikonda, W. Wang, and Y. Cao, "Modeling and miimization of pMOS NBTI effect for robust naometer design," in *Proc. ACM/IEEEDAC*, Jun. 2004, pp. 1047–1052.

[6] H. Abrishami, S. Hatami, B. Amelifard, and M. Pedram, "NBTI-aware flip-flop characterization and design," in *Proc. 44th ACM GLSVLSI*, 2008, pp. 29–34.

[7] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "NBTI-aware synthesis of digital circuits," in *Proc. ACM/IEEE DAC*, Jun. 2007, pp. 370–375.

[8] A. Calimera, E. Macii, and M. Poncino, "Design techniqures for NBTItolerant power-gating architecture," *IEEE Trans. Circuits Syst., Exp.Briefs*, vol. 59, no. 4, pp. 249–253, Apr. 2012.

[9] K.-C. Wu and D. Marculescu, "Joint logic restructuring and pin reordering against NBTI-induced performance degradation," in *Proc. DATE*, 2009, pp. 75–80.

[10] Y. Lee and T. Kim, "A fine-grained technique of NBTI-aware voltage scaling and body biasing for standard cell based designs," in *Proc. ASPDAC*, 2011, pp. 603–608.