Comparative Analysis of Low Power Adiabatic Logic Circuits in DSM Technology

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Abstract— *With the continuous scaling down of technology, in the field of integrated circuit design, low power dissipation has become one of the primary focus of the research. With the increasing demand for low power devices adiabatic logic gates proves to be an effective solution. This paper investigates different adiabatic logic families such as ECRL, 2N-2N2P and PFAL. The main aim of this paper is to simulate various logic gates using conventional CMOS and different adiabatic logic families, and thus compare for the effectiveness in terms of lower power dissipation. All simulations are carried out using HSPICE at 65nm technology with supply voltage is 1V at 100MHz frequency, for fair comparison of results W/L ratio of all the circuit is same. Finally average power dissipation characteristics are plotted with the help of a graph and comparisons are made between different logic families.*

Keywords— ***Low power, CMOS, Adiabatic logic, ECRL, 2N-2N2P, PFAL, Power dissipation, Four phased power clock.***

I. Introduction

The continuous advancement of semiconductor technology in electronic devices, over the years has resulted in better performance and higher circuit densities. However, as the size is getting smaller and the integration density increase, the increasing power dissipation has become a primary concern for further development of VLSI circuit technology. The two main types of power dissipation in semiconductor devices are: static power and dynamic power dissipation. The dynamic power dissipation is due to the energy loss during charging and discharging processes of output capacitance, during switching activities in transistor, while static power dissipation is caused by internal leakage in devices when the circuit is in off state [1].

Dynamic power dissipation has been the primary concern of circuit designers in early period. Various circuit technologies have been introduced for reducing dynamic power like sub-threshold logic [3], multi-threshold technology [4], and adiabatic circuit [2]. The adiabatic logic is a novel low power circuit technology, which utilizes AC voltage supply as opposed to DC voltage supply so as to energy of circuits.

The term 'adiabatic' comes from 'thermodynamics', which is used to describe a process in which no energy exchange with the environment, and hence no dissipation energy loss takes place. While in semiconductor devices, the charge transfer between different nodes is the process of energy exchange and different techniques can be used for minimizing this energy loss due to charge transfer. While fully adiabatic operation is the ideal condition of a circuit operation, in practical cases partial adiabatic operation of circuit is used which gives considerable performance.

In conventional CMOS circuits the energy stored in load capacitors was dissipated to ground. While, adiabatic logic, in contrast, offers a way to reuse this energy and thus prevents the wastage of this energy. By adding the ideas of both the conventional and the adiabatic logic circuit together, power dissipation can be reduced drastically.

Different circuits based on adiabatic logic have been proposed over the years [5-8]. To recycle the energy of circuit nodes, adiabatic logic based devices utilizes AC power clock which has four phase operation. In these circuits, the charge rather flowing from the load capacitance to ground, it flows back to the trapezoidal or sinusoidal supply voltage and thus can be reused [9].

In this paper, power dissipation is calculated for different logic gates using different adiabatic logic circuits and results are compared to see the effectiveness of different adiabatic logic families as compared to conventional CMOS circuits. The rest of the paper is organized as follows: Section 2 overviews the conventional CMOS and adiabatic logic circuits. In section 3, simulation of circuits is done and results of power dissipation are compared. The paper ends with the conclusion given in section 4.

II. Conventional CMOS and ADIABATIC LOGIC

The use of AC power clock as opposed to DC supply makes the adiabatic circuits capable of recovering the stored energy of node capacitors back to the power source, and hence, avoid the dynamic power loss almost completely, theoretically. The use of adiabatic logic principle in designing of low power circuits, is continuously growing, and is proving to be a better selection in comparison to other conventional circuits. The adiabatic operation usually consists of four phases, with a phase difference of one quarter of a period. The four phases of operation respectively are Wait, Evaluate, Hold and Recovery.

A. Conventional CMOS

In order to understand the conventional switching operation, a simple CMOS inverter is used. A pull-up and a pull-down MOS transistor, connected in series with a load capacitance C [Fig. 1].

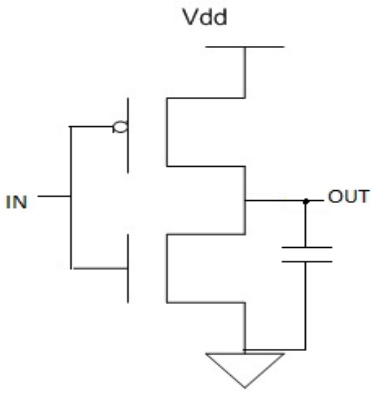

Fig.1: Conventional CMOS Inverter.

Power dissipation in CMOS transistors occurs mainly because of the device switching operations. At each charging and discharging operation, there is an inevitable energy loss of CV_{dd}^2 for static CMOS circuits. During charging operation, the energy dissipation through pull-up block from power supply is CV_{dd}^2 , of which half of the energy (0.5 CV_{dd}^2) is stored in load capacitor. The other half is dissipated through the resistive path, and lost as heat to the environment. Now during the operation of discharging, the residual energy stored in the load capacitor (0.5 CV_{dd}^2), will be released to the ground through pull-down network [11]. And therefore, no energy recovery is possible in the conventional CMOS circuits.

B. Adiabatic LOGIC

The use of AC power clock as opposed to DC supply makes the adiabatic circuits capable of recovering the stored energy of node capacitors back to the power source, and hence, avoid the dynamic power loss almost completely, theoretically. The use of adiabatic logic principle in designing of low power circuits, is continuously growing, and is proving to be a better selection in comparison to other conventional circuits. The adiabatic operation usually consists of four phases, with a phase difference of one quarter of a period. The four phases of operation respectively are Wait, Evaluate, Hold and Recovery [Fig. 2]. In the WAIT phase the power clock stays at low (zero) value, which maintains the outputs at low value, and the evaluation logic generates pre-evaluated results. Now, since the power clock is at low level, the pre-evaluated inputs will not affect the state of the gate. In the EVALUATE phase, the power supply ramps up from zero to Vdd gradually, and the outputs will be evaluated as per the result of pre-evaluation logic. In the HOLD phase, power clock stays high, providing the constant input signal for the next stage in pipelining of adiabatic circuits, and keep the outputs valid for the entire phase. Meanwhile inputs ramp down to low value. In the RECOVERY phase of operation, the power supply ramps down to zero and the energy of the circuit nodes is recovered back to the power source instead of being dissipated as heat [12].

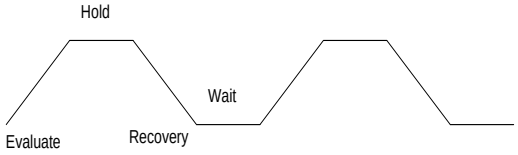

Fig.2: Four Phased Trapezoidal Power Clock

C. EFFICIENT CHARGE RECOVERY LOGIC (ECRL)

Efficient Charge Recovery Logic (ECRL) [5], as shown in Fig. 3, uses two cross-coupled PMOS transistors and two NMOS transistors in the N-functional blocks of ECRL logic block. In order to recover and reutilize the supplied energy, ECRL gates uses AC power clock (pck). Let us assume **In** is at high and **Inb** is at low. At the beginning of a cycle, when power clock 'pck' rises from zero to VDD, **Out** remains at low level because the high input **In** turns the F NMOS logic high. Output **Outb** follows the power clock 'pck' through M1. Now when 'pck' reaches to VDD, the outputs hold valid logic values. During the hold phase these output values are maintained and can be used as inputs for evaluation of next stage. In the next phase of recovery, the power clock falls down to zero level and the energy from the output node can be returned to the 'pck' so as to recover the delivered charge [13]. The major disadvantage of this circuit is the existence of coupling effects, since the two outputs are driven by the PMOS latch, and so the two complementary outputs may interfere with each other.

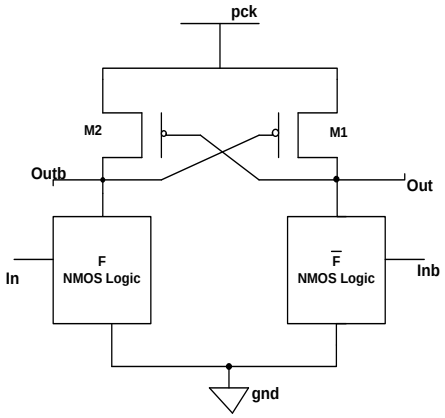

Fig.3: Efficient Charge Recovery Logic (ECRL)

D. 2N-2N2P LOGIC

2N-2N2P Logic family is a variation of ECRL Logic family with two new cross coupled NMOS transistors added parallel to the 2 existing NMOS transistors. The generalized 2N-2N2P circuit diagram is shown in Fig.4. And as the operation is concerned, it is identical to that of ECRL family. This new family is derived in order to reduce the coupling effects in the circuit. Also, the two new NMOS transistors have the advantage of eliminating the floating nodes for large part of the recovery phase. However, the added transistors prevent the circuits form achieving significant power reduction as compared to the ECRL logic circuits [10].

E. POSITIVE FEEDBACK ADIABATIC LOGIC (PFAL)

The Positive Feedback Adiabatic Logic (PFAL) achieves the lowest power consumption as opposed to other similar adiabatic logic families. The generalized PFAL circuit diagram is shown in Fig.5. The latch is made similar to the 2N-2N2P logic circuit with two PMOS transistors and two NMOS transistors. The functional blocks of NMOS logic are connected in parallel with the PMOS transistors of the latch and form the transmission gates. The fact that the functional blocks are in parallel with the PMOS transistors, the equivalent resistance is smaller during the charging of capacitance [13].

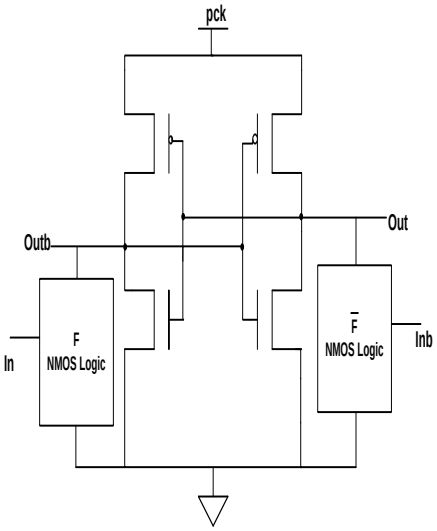

Fig.4: 2N-2N2P Basic Logic circuit

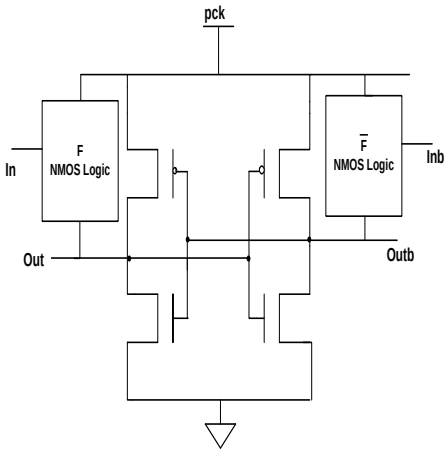

Fig.5: PFAL Basic logic circuit

III. SIMULATION AND RESULT

In order to see the effectiveness of different adiabatic logic families over conventional CMOS circuits, different logic gates have been implemented, first using conventional CMOS logic family and then by using the adiabatic principle of different adiabatic logic families as discussed in this paper and power calculations are made.

All the logic circuits are simulated using HSPICE at '65nm' technology. Table 1 lists the design parameters utilized in the simulation of circuits, and Table II shows the results of power dissipation for different logic circuits with the number of transistors used. Also, a graph has been plotted showing the comparison of average power dissipation.

Table. I. Design Parameters

TYPE	CMOS	Adiabatic Logics
PMOS (width)	260 nm	260 nm
NMOS (width)	130 nm	130 nm
Power supply	1 V DC supply voltage	Trapezoidal power clock, 0v-1v ,frequency: 200MHz
		Rise Time: 1.25 ns, Fall Time: 1.25 ns

Table II. Average Power Dissipation for Different Logic Devices

Logic	Basic Gate	Total Transistors	Average Power (nW)	Delay (pS)	PDP (aJ)
CMOS	Inverter	2 (1-NMOS, 1-PMOS)	174.46	1.249	216.2
	And	6 (3- NMOS, 3-PMOS)	179.64	1.251	224.5
	OR	6 (3- NMOS, 3-PMOS)	168.58	1.250	210.7
	NAND	4(2- NMOS, 2-PMOS)	138.86	1.250	173.5
	NOR	4(2- NMOS, 2-PMOS)	109.30	1.249	135.5
	XOR	8(4- NMOS, 4-PMOS)	336.36	1.263	424.8
	XNOR	8(4- NMOS, 4-PMOS)	144.91	1.265	183.2
RL	Inverter	4(2- NMOS, 2-PMOS)	59.816	1.246	74.52
	And /NAND	6 (4- NMOS, 2-PMOS)	48.793	1.246	60.49
	OR/NOR	6 (4- NMOS, 2-PMOS)	45.884	1.245	56.89
	XOR/XNOR	10 (8- NMOS, 2-PMOS)	51.590	1.243	64.12
2N-2N2P	Inverter	6 (4- NMOS, 2-PMOS)	75.426	1.250	94.27
	And /NAND	8 (6- NMOS, 2-PMOS)	59.183	1.228	72.19
	OR/NOR	8 (6- NMOS, 2-PMOS)	57.418	1.231	70.67
	XOR/XNOR	12(10- NMOS, 2-PMOS)	65.385	1.233	80.41
PFAL	Inverter	6 (4- NMOS, 2-PMOS)	12.936	1.218	15.75
	And /NAND	8 (6- NMOS, 2-PMOS)	14.774	1.245	18.31
	OR/NOR	8 (6- NMOS, 2-PMOS)	14.514	1.200	17.41
	XOR/XNOR	12 (10- NMOS, 2-PMOS)	29.075	1.200	34.88

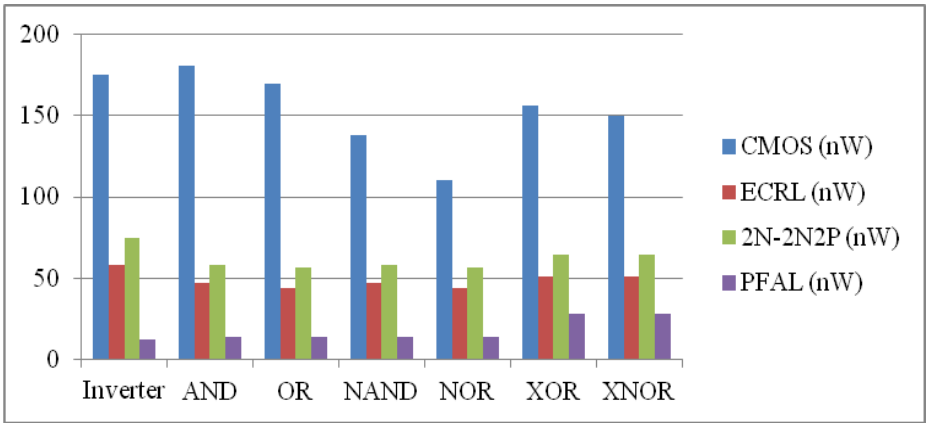

Fig.6: Comparison of Average Power Dissipation for Conventional CMOS and Different Adiabatic Families

IV. CONCLUSION

This paper reviews the adiabatic logic circuits and some important adiabatic logic families have been described and compared for their effectiveness in terms of reduced power dissipation as compared to conventional CMOS logic circuits.

Of all the adiabatic logic families compared, positive feedback adiabatic logic (PFAL) shows least power consumption as opposed to 2N-2N2P logic family and ECRL logic family. In order to reduce power dissipation, we observed that the logic switching should not be instantaneous but must be gradual instead. As the quest for ultra-low power circuit designs keeps on increasing, these improved circuit technologies would prove to be very useful in serving

the need. Also by observing the readings from different tables, it is observed that for a particular logic circuit, delay remains nearly constant at a particular frequency as dc voltage is varied from 0.1V to 0.3V.

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