Implementation of High Performance Vedic Multiplier Based on Efficient carry select adder

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***Abstract*— *In digital system multiplication is one of the most important function. Vedic maths, one of the ancient mathematics system make this tedious task much simple, efficient and suitable for VLSI implementation. This project implements high performance Vedic multiplier based on efficient square root carry select adder (SCSLA).The heart of a multiplier is adder.In this project the improvement is done on the adder to improve the total performance of the multiplier.In the existing system the first stage of SCSLA is RCA(ripple carry adder) with Cin=0 and second stage is BCE-1(Binary to excess one) converter.In moderrn digital systems parallel prefix adders(PPA) have been considered as the most efficient system for binary addition. Here,the first stage of the square root carry select adder is replaced by efficient and most common parallel prefix adders (PPA) such as Kogg stone adder(KSA),Brent-kung adder(BKA) and the hybrid of these two the Han Carlson adder (HCA). A comparative study is carried out to find out the efficient vedic multiplier with parallel prefix adder based SCLA .The result analysis shows that Vedic multiplier with HCA based squre root carry select adder exhibits efficient performance.The system is coded in Verilog HDL(hardware description language)and simulation,synthesis is carried out by using Model Sim 6.4a,Xilinx 14.5i.The implementation is done on Xilinx Spartan 3E FPGA(field programmable gate array).*

Keywords - *Brent-kung adder(BKA),Han-carlson adder(HCA),Kogg-stone adder(KSA), Parallel prefix adder(PPA), Ripple carry adder(RCA),Square root carry select adder(SCSLA), Vedic multiplier*

I.INTRODUCTION

Technology, which is rapidly growing has raised demands for efficient multiplier architecture. Multiplication is one of the primary arithmetic operation every application demands . Multiplier is the main component of arithmetic and logic unit(alu). [7]Compared to booth, array, wallace tree and dadda multipliers vedic multiplier exhibits efficient performance . Vedic multipliers work on the basis of vedic mathematics sutras. Vedic mathematics one of the ancient indian system of mathematics[9]. The word “vedic” is derived from the sanskrit word “veda” which means the store house of knowledge.the system was reconstructed by “sri bharathi krsna thirthaji”,a mathematician as well as a proficient in sanskrit. Bharathi kṛ ṣ ṇa tīrtha's book, vedic mathematics, is a list of sixteen terse sutras, or "aphorisms", discussing strategies for mental calculation. Bharathi kṛ ṣ ṇa claimed that he found the sutras after years of studying the vedas, a set of sacred ancient hindu scriptures.there are mainly two sutras for multiplication purpose - urdhva tiryagbhyam (vertically crosswise) and nikhilam navatashcarmam dashatah(all from 9 and the last from10).among these two urdhva tiryagbhyam is efficient and gives minimum delay for multiplication for all types of numbers irrespective of their size.here, vedic multiplier is designed on the basis of this sutra.

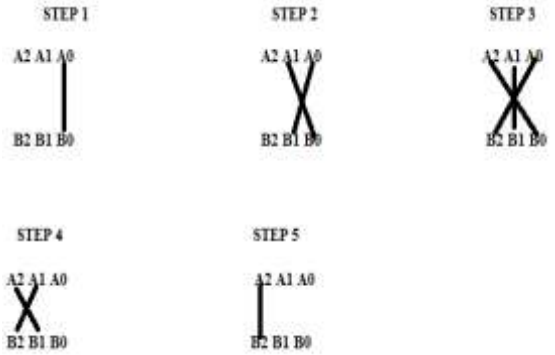
The heart of a multiplier is adder. Ripple carry adder(rca) exhibits area efficient design but the delay is high.the carry look ahead adder(cla)is one of the fastest adder but consume more area.so, as a compromise carry select adder can be used.the carry select adder can be used to obtain better overall performance[4]as it uses multiple pairs of rca(ripple carry adder) the area is not much efficient.the carry propagation delay can be avoided in carry select adder(csla)because multiple carries are generated independently and to generate sum carry is selected by using a mux..the square root carry select adder outperforms the normal csla,it uses different size of adders in each parallel stage.in this article,vedic multiplier is designed on the basis of efficient sqaure root carry select adder with first stage parallel prefix adders(ppa) and second stage with binary to excess one converter. A comparative study is carried out by changing the first stage of the square root csla by common and efficient parallel prefix adders such as kogg stone adder(ksa),brent kung adder(bka), and the hybrid of these two the han carlson adder(hca).

II.VEDIC MULTIPLIER

Vedic mathematics have various simple and efficient multiplication methods.The concept of vedic maths can be easily understood,and calculations can be done without the help of pen and paper. Vedic maths provides two sutras for multiplication purpose : Urdhva Tiryagbhyam (Vertically crosswise) and Nikhilam Navatashcarmam Dashatah(All from 9 and the last from10). Urdhva Tiryagbhyam which is applicable to all case of multiplication iand also for division of large numbers.In this article architecture based on Urdhva -Tiryagbhyam is used.[1]

3-bit vedic multiplication:
A2 A1 A0 x B2B1B0
Considering A2A1A0 and B2B1B0 are input to a 3 bit vedic multiplier.
Here

S0=A0B0
S1=A1B0+B1A0
S2=A1B1+A2B0+A0B2,S3=A2B1+A1B2
S4=A2B2



In this paper 8x8,16x16,32x32 Vedic multipliers are designed by using four type of square root CSLA.The structure is as shown below.2x2basic Vedic multiplier:Here two half adders are cascaded in the manner as shown

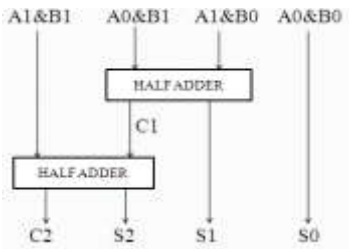


Fig.1:Basic 2x2 vedic multiplier[5]

a)4x4 vedic multiplier:

It uses 2x2 basic multiplier in the first stage for multiplication and three 4-bit CSLA for addition.

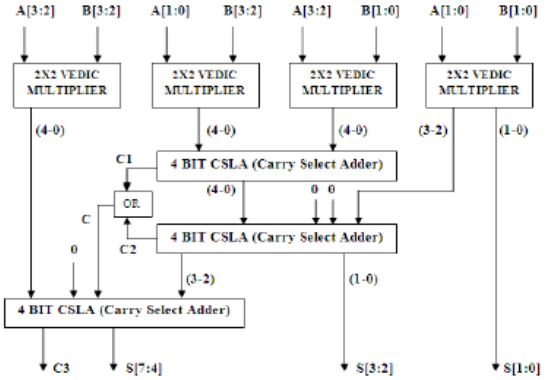


Fig. 2: 4x4 Vedic multiplier[5]

b)8x8 Vedic multiplier

It uses 4x4 Vedic multipliers for first stage multiplication and 8-bit CSLA for partial product addition.

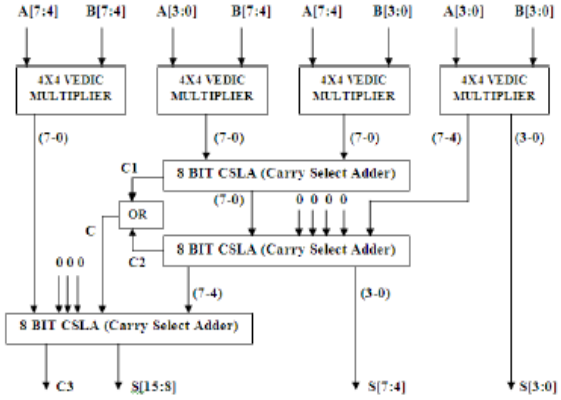


Fig. 3: 8x8 Vedic multiplier[5]

c)16x16 Vedic multiplier

In the first stage 8x8 multipliers are used and 2nd addition stage 16-bit CSLA is used.

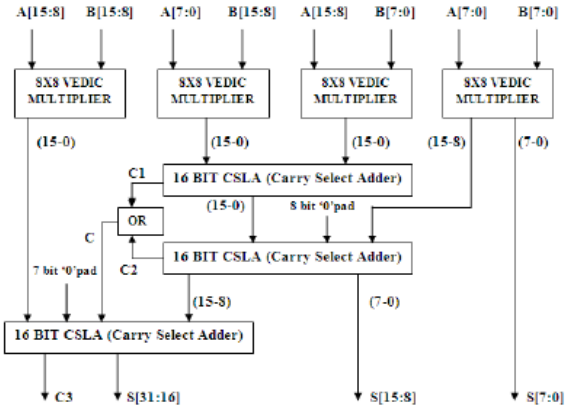


Fig. 4: 16x16 Vedic multiplier[5]

d)32x32 Vedic multiplier

16x16 vedic multipliers are taken in the first step and 32 bit carry select adders are used for further addition.

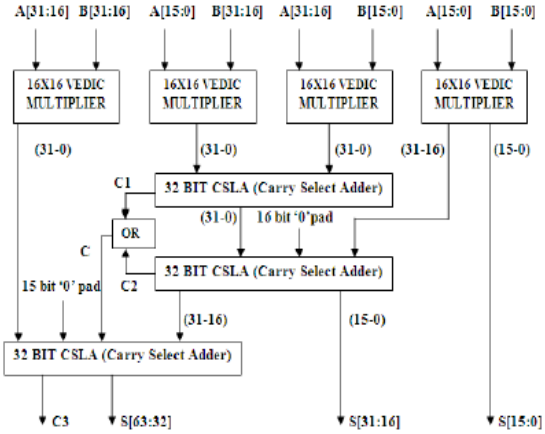


Fig. 5: 32x32 Vedic multiplier[5]

III.CARRY SELECT ADDER

The basic operation of a carry select adder is parallel computation[10].CSLA generates carries and partial sum.The final sum and carry is selected by multiplexers(MUX).In general there exists linear CSLA and squre root CSLA(SCSLA).In the case of linear CSLA the bit length is equally divided but in the case of SCSLA the bit length are unequally divided(variable length adders are used)[11].

a)Sqaure root carry select adder(SCSLA)

In the case of a sqaure root carry select adder, in each parallel stage ,differently sized adders are used.It is also known as variable sized adders.The bit length are unequally divided in each stage. By replacing the second stage by binary to excess one converter(BEC-1) more area efficiency can be obtained.

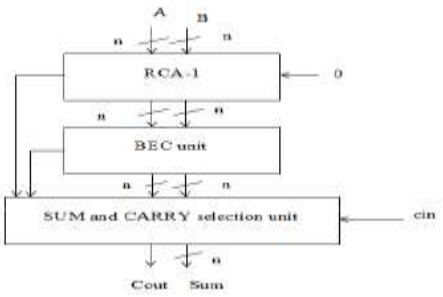


Fig .6:Square root carry select adder with BEC unit.[3]

Example

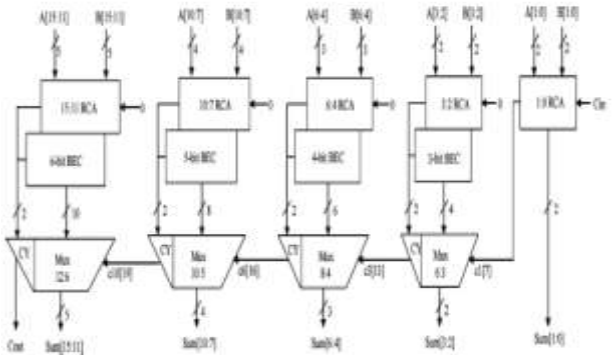


Fig.7: 16-bit square root CSLA

IV.PROPOSED SYSTEM

To further improve the efficiency the first stage of the SCSLA-RCA with Cin=1 is replaced by most common and efficient parallel prefix adders such as Kogg-stone (KSA),Brent-kung adder(BKA),and the hybrid of these two the Han Carlson adder (HCA).

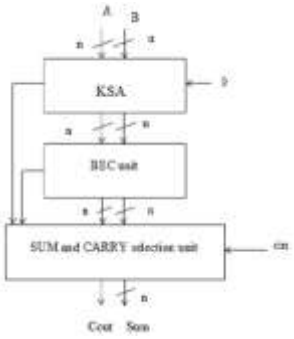


Fig.8:SCSLA-KSA

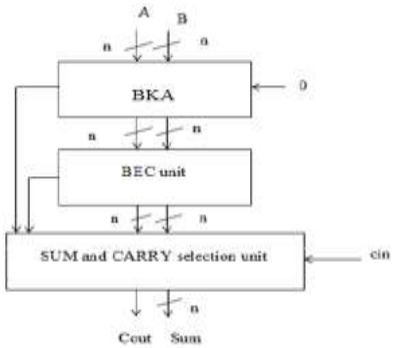


Fig.9:SCSLA-BKA

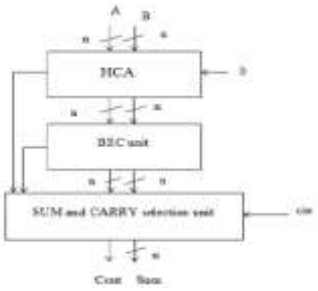


Fig.10:SCSLA-HCA

In this paper a comparative study of vedic multiplier is carried out by using these adders.

V.PARALLEL PREFIX ADDERS

Parallel prefix adders is considered to be one of the fastest type of adder design.It is flexible and well suited for VLSI design.The addition processes involves three stages.

i)Propagate and Generate signal generation. (pre-processing step).
This step involves the computation of generate and propagate signals,corresponding to each pair of bits a and b.The output is generate and propagate signals.
Pi= ai xor bi, Gi=ai and bi.[8]

ii)carry generation stage.(Intermediate signal generation stage)
In this stage carries are computed.It generates carry propagate and generate as intermediate signals.
CPi:j=Pi:k+1 and Pk:j, CGi:j=Gi:k+1 or (Pi:k+1 and G k:j).[8]

iii)sum computation stage.(post-processing stage)
This is the final step in the addition operation.
Ci-1=(Pi and Cin) or Gi. Si=Pi xor Ci-1.[8]

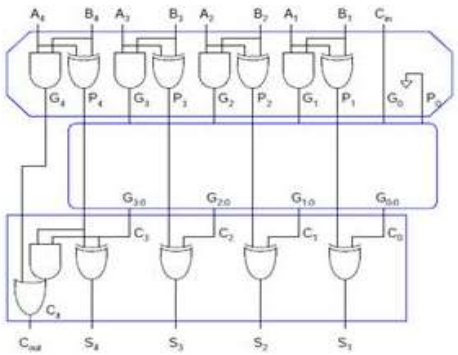
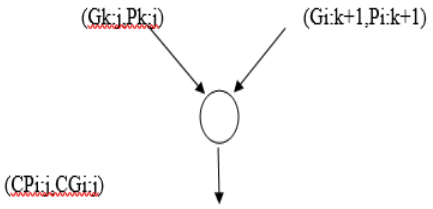


Fig.11:PPA block diagram

The parallel prefix adder is constructed by carry operators or O-operators.



Propagate and generate signals are produced in the first stage.Then these are given to carry generation block.Different structures of these adders are different with respect to carry generation method..

a)kogg-stone adder(ksa): One of the most important parallel prefix adders which is widely used for VLSI applications.The carry signals are generated on the order of logN,where N is the number of inputs.It exhibits high speed,but the major disadvantage is that the area utilization is high.In this project 2,3,4,5,6,7,8 bit KSA'S are needed and used.

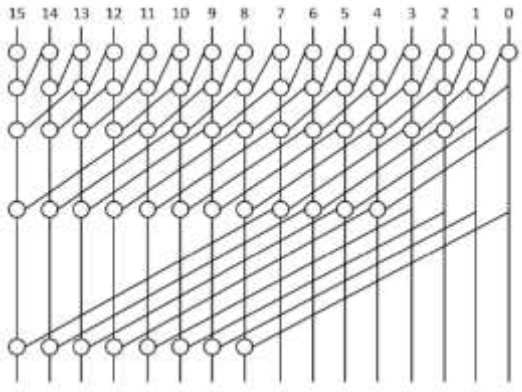


Fig.12:KSA carry generation tree[6]

b)Brent-kung adder(BKA):This kind of adders show less efficiency compared to KSA.But it exhibit better area utilization due to less wiring congestion.

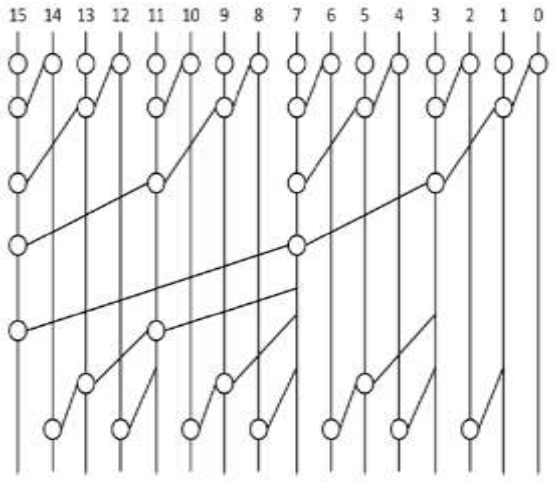


Fig.13:BKA carry generation tree[6]

C)Han Carlson adder(HCA):It is the hybrid of KSA and BKA.This adder uses one Brent-kung Adder in the first stage followed by Kogg-stone adder and one Brent -kung adder in the last stage[

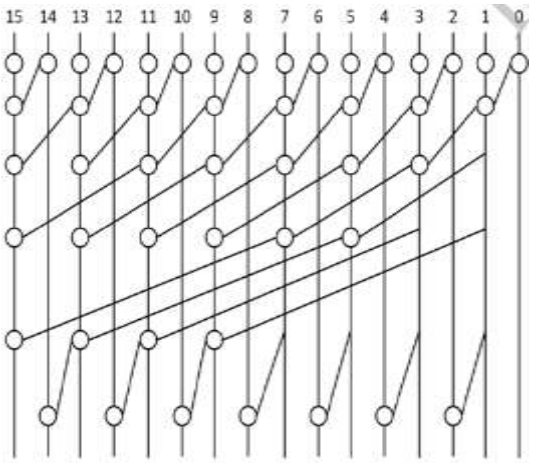


Fig.14:BKA carry generation tree [6]

VI.RESULT AND DISCUSSION

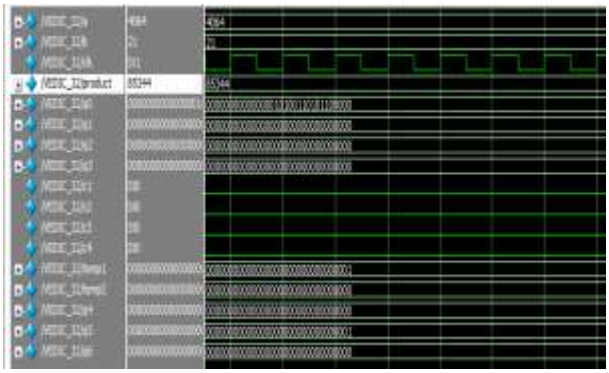
Here a comparitive study between 4 types of Vedic multiplier based on squre root CSLA is carried out.Multipliers are compared in terms of power,delay memory and LUT(look up table).From The result analysis it could understood that HCA-SCSLA based vedic multiplier shows better results.

	8x8 RCA-CSLA	8X8 BK-CSLA	8X8 KS-CSLA	8X8 HCA-CSLA	16X16 RCA-CSLA	16X16 BK-CSLA	16X16 KS-CSLA	16X16 HCA-CSLA	32X32 RCA-CSLA	32X32 BK-CSLA	32X32 KS-CSLA	32X32 HCA-CSLA
Power (KW)	1.48	00.76	00.98	00.76	3.76	1.32	2.74	1.32	9.48	3.80	5.32	3.79
DELAY (nS)	10	10.13	12.00	10.13	13	14	14.13	14	16	27	27.05	27
LUT	164/ 63400	163/ 63400	125/ 63400	163/ 63400	777/ 63400	694/ 63400	743/ 63400	694/ 63400	3391/ 63400	2902/ 63400	3021/ 63400	2858/ 63400
MEMORY (KB)	317032	294536	239936	23453 6	313286	235176	313286	235176	319080	317928	318321	238824

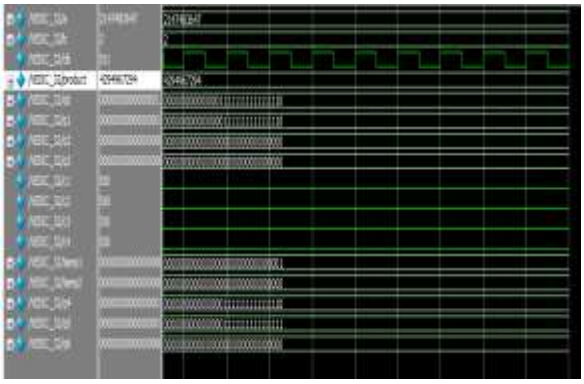
VI. SIMULATION RESULTS

32x 32 vedic multipliers waveforms:

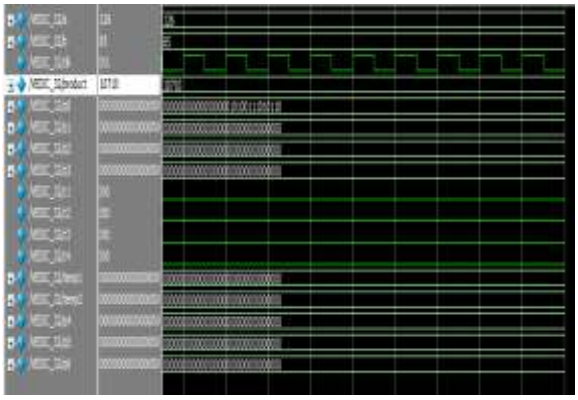
i)vedic multiplier with first stage RCA based CSLA



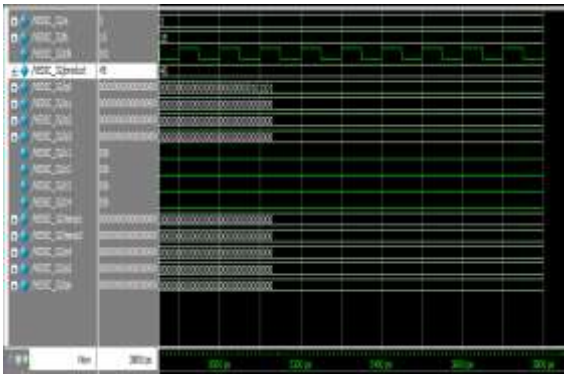
ii)vedic multiplier with first stage KSA based CSLA



iii)vedic multiplier with first stage BKA based CSLA



iv) vedic multiplier with first stage HCA based CSLA



VII.CONCLUSION

In this paper vedic multiplier based on different type of squre root carry select adder is designed and studied.RCA-SCSLA,BKA-SCSLA,KSA-SCSLA,HCA-SCSLA based vedic multipliers are designed and compared.The comparison is done baed on area,power,delay,LUT etc.From the total analysis it could understood that HCA-SCSLA based vedic multiplier shows efficient performance.

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