Variation of Power and Delay in Digital CMOS Circuit Design in DSM Technology

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Abstract- *In Deep Sub-Micron (DSM) technology, more number of gates are to be integrated on a single chip, so as to result in small geometries. But with this power densities and total power are rapidly increasing. Design of low power circuits has become important in a variety of application. However reducing power consumption involves a tradeoff between timing and area at different stages of the design. The successful power sensitive design requires engineers to accurately and efficiently be able to perform these tradeoffs. All the simulations are performed by using HSPICE tool at 45 and 32nm CMOS technology. We have compared Power, delay and PDP on conventional gates at low frequency at 25^0C and 110^0C and analyze the impact of technology scaling with variation of temperature in all conventional gates.*

Keywords: *Energy, Delay, Power consumption, PDP.*

I. INTRODUCTION

The urge of high performance and dynamic functionalities in an integrated circuit has led to aggressive technology scaling over the years. The supply voltage (V_{DD}), device threshold voltage (Vth) and the device geometry are expected to be scaled further with this trend. Which results in reducing the short channel effects and increased transistor OFF- state current (I_{OFF}). Additionally leakage currents, higher operating frequency and on die transistor count will lead to increase in total power dissipation [1-3]. A number of techniques have already been proposed for reducing power dissipation. The two important types of power dissipation in VLSI circuits are 1) Static power dissipation and 2) Dynamic power dissipation. While static power dissipation is due to internal leakages in devices during the off state of a circuit [1], dynamic power dissipation is because of the energy loss during charging and discharging of the output node capacitance of a transistor when switching takes place.

The propagation delay of the circuit is used to determine the speed of the circuit. It vary according to the size of transistor, the transistor count per stack, the parasitic capacitance and intrinsic capacitances including the capacitive effects of inter-cell and intra-cell routing and the logic depth [3][5]. The propagation delay is not only a function of circuit technology, but also depends upon various other factors. Most importantly, delay is a function of the input and output signal slopes of the gate. The propagation delay times, t_{PHL} and t_{PLH} determines the signal delay from input to output during the output transitions from high to low value and low to high value. t_{PHL} is the time delay between the transition $V_{50\%}$ of rising input voltage and the $V_{50\%}$ of the falling output voltage [6-8]. Similarly, t_{PLH} is defined as the time delay between the transition $V_{50\%}$ of the falling input voltage and the transition $V_{50\%}$ of the rising output voltage. In breaking the transistor into two half increases the resistance of the transistor which reduces the performance in terms of speed of the circuit and saves the power consumption of the conventional gates.

$$T_p = \frac{T_{PHL}+T_{PLH}}{2} \quad \text{eq… (1)}$$

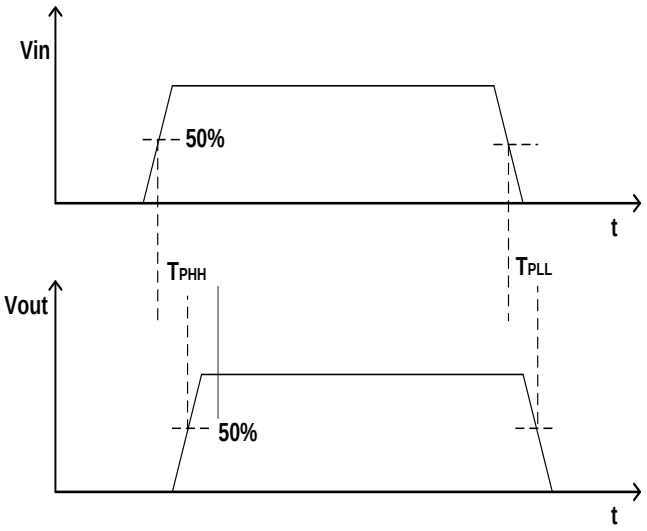

Fig.1: Propagation Delay Characteristic.

Power Delay Product

The term Power Delay Product (PDP) is the energy required by the circuit to perform the logical task. The energy consumption or power-delay product is a fundamental parameter, often used in measuring the performance and the quality of a CMOS process and gate design. As a physical quantity, power delay product can be interpreted as the average energy consumed by a gate while switching its output from low to high and high to low [9-10].

$$PDP = C\,VDD^2$$

eq…(2)

The module area depends upon the size and number of transistors and routing complexity. The main objective in the design of VLSI circuits is to minimize silicon chip area per logic gate so as to have large number of gates per chip. Area reduction can take place in three different ways, first through advancements in processing technology that enables the reduction of the device size, second through advancements in circuit designing techniques, and third through carefully designed chip layout. Comparatively smaller devices, however, possess lower current-driving capability, which tend to increase the delay [11-13].

III. Literature review

Today CMOS (Complementary Metal Oxide Semiconductor) is the primary technology in the semiconductor industry. In general, CMOS gate has an nMOS pull-down network to connect the output to '0' (GND) and pMOS pull-up network to connect the output to '1' (V_{dd}). The pull-up and pull-down networks are constructed in a mutually exclusive manner so that only one of the networks is conducting in steady-state.

Paper	Techniques	Objective	Outcomes
LECTOR: A Technique for Leakage Reduction in CMOS Circuits [9]	Leakage Reduction Narender Hanchate, IEEE Tran. -2004	Reduction of the threshold voltage due to voltage scaling leads to increase in subthreshold leakage current	Resulting in better leakage reduction compared to other techniques Provides a proper threshold voltage for ultrathin body MOSFET
Leakage Power and Delay Analysis of LECTOR Based CMOS Circuits [11]	Leakage Reduction, Preeti Verma, IEEE Conferance. 2011,	Analysis for leakage current and propagation delay of the basic CMOS gates viz. NOT, NAND and NOR gates implementing LECTOR technique	From the experimental results it can be verified that we get an average saving of 66% for leakage power reduction with 16% increase in delay. Propagation delay may be further reduced by sizing the transistors but this will increase the area overhead of the circuit.
A Review on Leakage Power Reduction Techniques at 45nm Technology [6]	Leakage Power Reduction Techniques N.Praveen Kumara, IEEE Paper, 2015	We presented various techniques to reduce the standby power at 45nm technology.	Presented various stand-by current reduction mechanisms. Simulations were carried out at 45nm technology using cadence tool. Simulations results show that these techniques reduce the stand-by current nearly to 60% at optimum performance.

Impact of technology scaling on leakage power in nano-scale bulk CMOS digital standard cells [11]	Leakage estimation in nano-scale technology, Zia Abbas , Microelectronics Journal 45 (2014)	Whole analysis are reported for use in further research on leakage aware digital design.	In This paper presented the characterization of the effect of technology scaling on different leakage current components in a complete standard cell set, referring to 45 nm, 32 nm and 22 nm traditional bulk CMOS process.
Estimation of leakage power and delay inCMOS circuits using parametric variation [14]	Leakage power dissipation is amajor concern for scaling down portable devices , Preeti Verma , Perspectives in Science (2016)	In this paper leakage reduction technique HTLCT (High Threshold Leakage Control Transistor)is discussed. Using high threshold transistors at the place of low threshold leakage control transistors, result in more leakage power reduction as compared to LCT (leakage control transistor) technique but at the scarifies of area and delay.	It is found that the leakage power dissipation increases with increasing temperature, supply voltage and aspect ratio. We get an average saving of 34.17% increases of LCT NAND gate and 41.50% for HTLCT NAND gate as compared to standard two input NAND gate. It is also seen that LCT based circuits have less power consumption but more delay as compared to conventional design.

In this section, we first explain target focusing on generic logic to evaluate our sleepy stack technique. Then we explain low-leakage techniques we consider for purposes of comparison. Although the basic ideas behind for the comparison of this techniques have been seen in this section will give detailed structure with transistor sizing for each prior technique to be compared to our proposed approach. Finally, we explain experimental methodology that we used to compare our technique to the previous techniques we consider.

IV. Results and Dissuasion

This now work on Conventional gate circuits designing has been carried out with the sole purpose of achieving even better performance of devices. And that performance is being evaluated based on certain performance evaluation parameters.

In over work we have calculated various parameters on conventional and proposed techniques on various gates, from simulation results proposed circuit saved dynamic power, static power, delay and PDP than other existing techniques.

Delay is calculated for all fourteen circuits, goes minimum for input vector variants V1 and V2 for all circuits. Here PMOS transistor is split into two, with lesser widths on same technology. The width of the split transistors can be reduced further for getting lesser delays as compared to the original circuit. The W/L ratio variations and corresponding delays for 2 input NAND gate. Leakage power of conventional gate is compared with technique implemented in with all the input vector combination at 25^0 C.

Table I. Design Parameters for CMOS Logic Families

TYPE	CMOS	CMOS
PMOS (width)	260 nm	260 nm
NMOS (width)	130 nm	130 nm
Power supply	1 V DC supply voltage	0.9V power clock
Frequency	100MHz, 500MHz, 1GHz	

Transient analysis at 45nm and 32nm technology

The figures below show the transient analysis of based proposed circuits at 45nm and 32nm technology with

operating frequencies viz. 100 MHz, each figure consist of the waveforms of the 2 inputs namely A, B and one outputs namely basic gates circuit. As the figure reveals the circuit provides full output voltage swing for all the input combinations and no voltage degradation occurs in both the output waveforms namely hence the voltage degradation problem that existed in case of most of the low power reference circuits is been successfully eliminated.

Power analysis at 45nm technology

The Table 1, below show the power consumption obtained during the simulation of the proposed circuits at 45nm technology at different operating frequencies viz. 100 MHz, 0.9V and 0.8V supply voltage as shown in Table II and III.

Delay analysis

Delay in any circuit basically depends on the Input path in a basic circuit that is also called the critical path of an adder circuit. The Table below show the results of the delay obtained during the simulation of the proposed circuit at various input frequencies.

Table .II: Dynamic Power at 45nm 25^0C

Gates	Average Power(µW)	Delay(pS)			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.315	5.947	6.281	6.116	1.926
AND	0.426	11.96	6.524	9.244	3.937
NAND	0.372	9.515	4.452	6.983	2.597
NOR	0.346	10.38	4.194	7.287	2.521
EXOR	0.469	7.447	7.672	7.559	3.545

Table.III: Dynamic Power at 32nm 25^0C

Gates	Average Power	Delay			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.4440	5.382	5.612	5.497	2.440
AND	0.5708	11.19	5.658	8.424	4.808
NAND	0.4862	9.422	2.694	6.058	2.945
NOR	0.4661	10.73	3.571	7.150	3.332
EXOR	0.5875	11.96	12.83	12.39	7.279

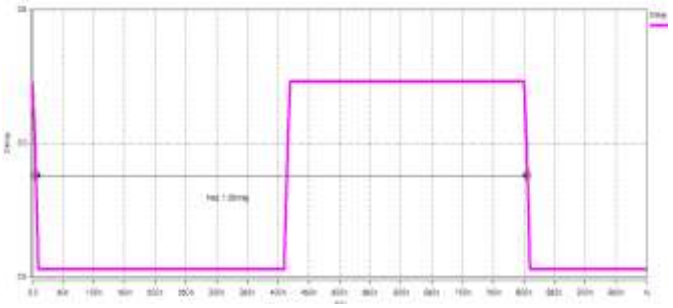

Fig.6: Calculation of frequency of operation Delay V/S time graph

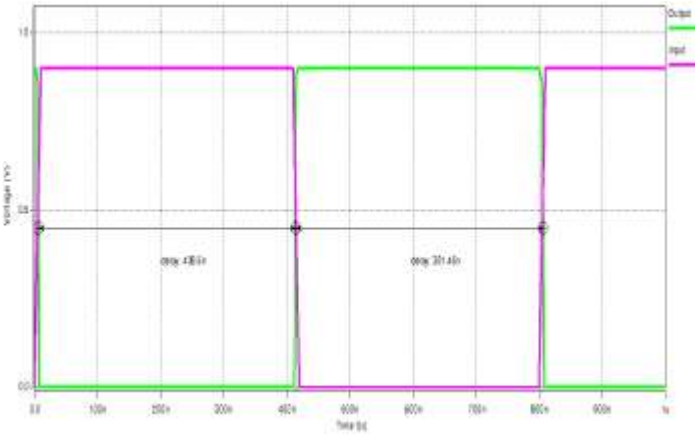

Fig.7: Calculation of Delay Voltage V/S Time graph

DC analysis results for two input logic gates at 45nm technology

In this section, Table IV and Table V shows results Comparison between standard circuit & proposed circuit of leakage power dissipation for two input logic gate at 45nm technology at 25^0C and 100^0C temperature.

Table.IV: Leakage Power Consumption at 45nm at 25^0 C

Gates	Leakage Power Consumption at 45nm			
	00	01	10	11
NOT	22.84	77.12		
AND	62.46	111.4	78.07	174.4
NAND	32.44	153.9	105.7	153.5
NOR	45.62	89.51	76.85	114.8
EXOR	165.1	112.4	113.4	158.9

DC analysis results for two input logic gates at 32nm technology

Comparison between standard circuit & proposed circuit of leakage power dissipation for two input logic gates at 32nm technology at 25^0C and 100^0C

temperature. We observe that from our proposed analysis will be more effective as we scale down in nano-design technology. We have seen observe from our analysis that we have less power consumption as we scale down from 45nm to 32nm technology. From this analysis we say that our proposed hybrid technique is more beneficial for nano scale design circuits.

Table. V: Leakage Power Consumption at 32nm at 25^0 C

Gates	Leakage Power Consumption at 32nm			
	00	01	10	11
NOT	32.14	84.88		
AND	73.34	148.6	93.00	190.9
NAND	38.92	131.2	112.57	169.73
NOR	55.26	94.97	84.33	142.90
EXOR	174.2	143.70	133.70	169.28

DC analysis has been done for calculating I_{Leak} and P_{ST}. For this purpose 45nm 32nm technology by using BPTM file is used at 1V and 0.9V and temperature sets at. Width to Length (W/L) ratio for the PMOS and NMOS transistors is '3' and '1.5' respectively. For DSM circuits mainly I_{SUB} is the dominating component of power dissipation in CMOS IC. Hence I_{SUB} of all the test bench circuits is represent graphically also. This file contains every physical design details of a CMOS transistor, where 45nm and 32nm is the effective length of CMOS transistor. All kind of analysis with mapping of this file is shown through the flow of HSPICE design flow.

V. Conclusion

Leakage reduction solution as compared with the other conventional and relevant techniques and there is no need of technology modification, no change of fan-out logic state of WLS gates during idle mode and needs no additional power supply. Trade–off between area, delay and power requirements can be obtained by the use of specific variant in a given circuitAnd every variants suitable for specific performance parameter like V1, and V2 is better when speed is our main concern, it reduces 14.58% of the average delay for these circuits, but in this case W/L ration of PMOS must be adjust. Table.3 and 4 shows overall optimum result for leakage reduction and power.

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