Comparative Analysis of Low power, high speed based Level shifters

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Abstract:- *Since the last two decades, the trend of device miniaturization has increased to get better performance with a smaller area of the logic functions. In deep submicron regime, the demand of fabrication of nanoscale Complementary metal oxide semiconductor (CMOS) VLSI circuits has increased due to evaluation of modern successful portable systems. Leakage power dissipation and reliability issues are major concerns in deep submicron regime for VLSI chip designers. Multi-VDD design reduces the power consumption in Systems-On-Chips(SoCs). As the level shifter in multi-VDD system imposes additional power consumption and propagation delay, it is necessary to optimize the level shifter circuit for minimum power-delay product (PDP) to obtain the potential benefit of using multiple power supply. Carbon nanotube FET(CNT-FET) is one of the novel devices that could replace conventional silicon MOSFET for low power applications due to its superior electrical properties. In this paper, the power and speed of CNT-FET based level shifters in 32-nm technology node are optimized by choosing chirality, diameter, number of nano tubes and substrate (back gate) bias for both feedback-based and multi-VTH based level shifters.*

Keywords - *Leakage Power, CNTFET, Chirality, DCVS-LS, SI-LS, PDP, EDP.*

I. INTRODUCTION

Efficiency of implementation of arithmetic circuits in the execution of dedicated algorithms such as digital filtering, correlation and convolution largely affects the performance of application specific integrated circuits and digital signal processors. The increasing density of transistors hence complexity in the integrated circuits demands for high speed, power efficient designs. The researchers over the time have developed numerous CMOS Logic styles to meet the requirement of the rapidly growing industry. Lowering the supply voltage is a means of reducing the power consumption of the circuit in ultra deep submicron technology but it results in degraded driving capability and increased circuit delay of the designed cells.

Today, electronic devices play a very important role in every one's day to day life. Devices such as mobile phone, ipad, laptop, pocket calculator become necessity to live a comfortable life. Consumer prefers portable and battery powered electronic devices. Earlier in 1990's, performance and speed was the important parameters to design any system but now with the growing trend towards portable computing and wireless communication, power dissipation has become one of the most critical factor in the continued development of microelectronics technology [1].

In very large scale integration circuit power consumption play important role in CMOS circuit. In a CMOS circuit there are mainly two types of power consumption static and dynamic power consumption. Static power consumption is due to leakage current and dynamic power consumption is due to charging and discharging of capacitor and third power consumption is due to short circuit. For the decade getting high performance, high packing density and low power reducing the transistor size scaling is required. Using such type of methodology the leakage power of transistor has increase exponentially. In CMOS circuit reduction of threshold voltage due to voltage scaling leads to increase in sub-threshold leakage current and hence static power dissipation. When the technology is scaled supply and threshold voltage also scaled. Due to reducing transistor size, the channel length also become short which increase the leakage current through a transistor in off condition. Leakage power is a very serious problem in mobile application so resolving this, different type of technique are used at circuit level and process level.

A Differential Cascaded Voltage Switch is called basic Level Shifter (DCVS-LS), and it is facing a problem of contention current for short duration due to charging and discharging of pull up network (PUN) and pull down network (PDN) and short circuit power consumption take place [1]. Other technique for reducing the contention current which imbalance for reducing driving capacity of PMOS transistor in DCVS-LS by reducing supply voltage of PMOS transistor [2, 8]. Contention current is reduce by dynamic current generator that ON only small period of time and OFF for rest period of time for reducing the static power dissipation [9, 10]. So multi-threshold voltage technique is used with pass transistor and simple inverter that is alternative to differential cascade type of structure [11]. Other improvised in circuit are wide range level shifter that shift low or subthreshold input voltage [12, 13] to higher voltage i.e. supply voltage [14].

In this paper a low power design for a single Level Shifter. The existing design gives very good

performance at high speeds with satisfactory voltage swing at the output. The rest of the paper is organized as follows. The section II consist of the description of the previous work with their advantages and disadvantages. The sections III and conclusion respectively.

II. CNTFET

Survey includes the different power optimization methods at various level of digital circuit design process from system level to physical level. Different sources responsible for power dissipation in CMOS circuits are also reviewed. This work present comparison of CNTFET with CMOS is performing in domino logic circuit for calculation average power, delay and PDP. The transistors made up with 32nm channel length are used for both CNTFET and CMOS. The HSPICE circuit simulation uses 32 nm Stanford University CNTFET models [8] for CNTFET and the 32 nm PTM (Predictive Technology Model) for CMOS [9].

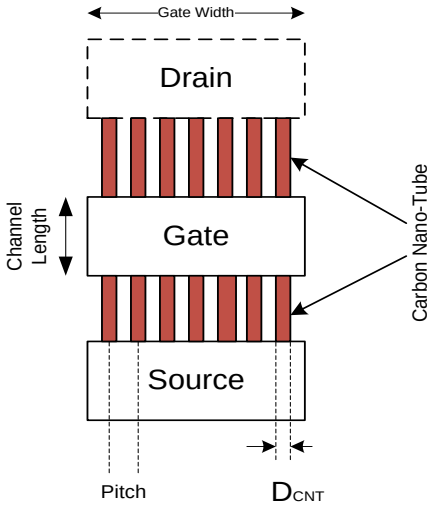

Fig.1 Top view of CNTFET

2.2.1. Differential cascade voltage switch based level shifters (DCVS-LS)

This is the schematics of DCVS-LS based level shifter shown in Fig.2. DCVS-LS has two PMOS transistor that comprises half-latch and two NMOS transistor that are connected two low level voltage (V_{DDL}) and one of them are complemented form of input signal (Q and $\bar{Q}$) and shifted output V_{DDH} is taken from node P and it's transient analysis is shown in Fig.4. Which give two complementary output (P and $\bar{P}$) which is shifted version of (V_{DDL}) that is V_{DDH}. The output node of PMOS transistor make cross-couple through feedback to avoiding any static leakage current from V_{DDH} to ground terminal.

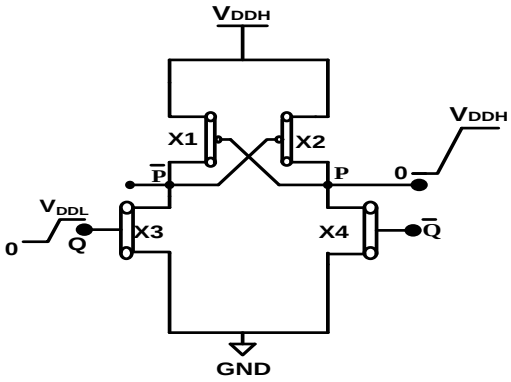

Fig.2 Differential cascade voltage switch based level shifter

Initially assume that one of output node $\bar{P}$ to be V_{DDH} and another P is to 0, thus transistor X1 is ON and X2 is OFF. And low input signal applied at node Q of the X3 transistor that makes it ON and pull-down at 0 to node $\bar{P}$. When voltage at node Q is decrease below the threshold voltage of X2 transistor, then it became ON. Due to this node P will charge through the supply voltage V_{DDH} and due charging of node P, X1 transistor will turned OFF and node $\bar{P}$ will be pulling down by X3 transistor. Finally at total transitions are completed and $\bar{P}$ will be 0 and P will be at V_{DDH}. During total transition X1 and X3 will simultaneously turn ON for short period of time due to this flow of short circuit current or contention current from V_{DDH} to GND. Hence the differential-cascade type of circuit will permit contention current at node Q and $\bar{Q}$.

Another issue with this circuit is that if strength of PDN is not analogous to the PUN due to low level input voltage and modest width of X3 and X4, delay of circuit increase and in worst case it provide non-functional of circuit.

In this paper main aim is reducing delay, power consumption and study of problem arises due to contention current.

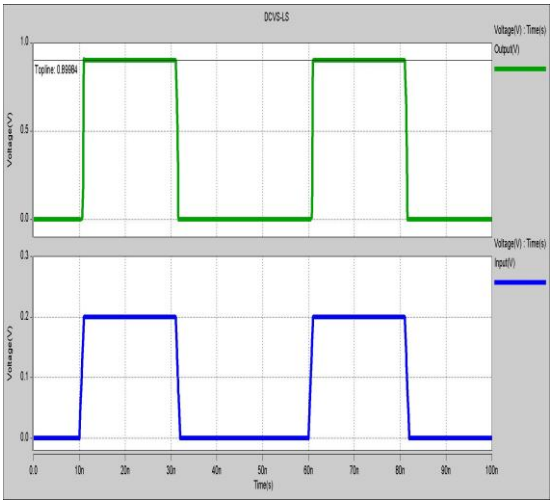

Fig.3 Transient analysis of DCVS-Level shifter

2.2.2 Simple Inverter based Level Shifters (SI-LS)

The schematic diagram of SI-LS is shown in Fig.4. This circuit contain multi-V_{TH} technique that has two stage of cascaded inverter i.e. inverter-I followed inverter-II. In inverter-I the PMOS X1 has shown by narrow tube indicate smaller diameter for higher threshold voltage. The working of SI-LS is as low swing input voltage (0 to V_{DDL}) is given to inverter-I that give high swing inverted output voltage at node A (V_{DDH} to 0). Then it act as input for inverter-II which output is proper up-converted form of input voltage i.e. 0 to V_{DDH}. Here important things is that threshold voltage PMOS X1 should be higher than the difference of (V_{DDH}- V_{DDL}) to reduce static leakage current and inverter-II need have proper sized to reduce loading effect on inverter-I. The important in SI-LS circuit is to proper sizing of all CNTFET to reduce static current.

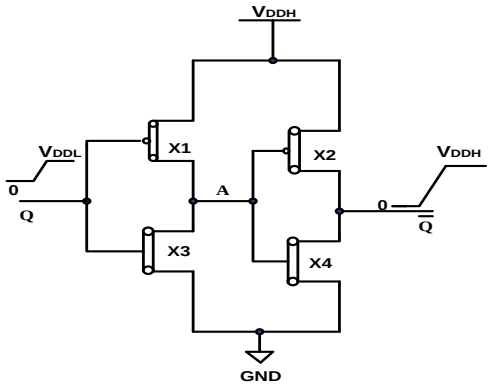

Fig.4 Simple inverter based level shifter

III. Optimization of CNT-FET based LEVEL SHIFTERS

Both chosen circuit DCVS-LS and SI-LS are optimized individually (a) by adjusting the number of nanotube (N) of PUN and PDN and (b) by adjusting the back gate (substrate) bias of CNTFET. Optimization is made for input voltage V_{DDL} of 0.2V that is shifted up to 0.9V. Some of the chirality which use in circuit, their diameter and threshold voltages are listed in Table.I and these are calculated using equation (1) and (3).

3.1 Optimization of DCVS-LS

In DCVS-LS if PUN and PDN are not properly matched this results in heavily contention current or in worst case circuit not function properly. Then output of DCVS-LS is several time lower than the applied input voltage. Hence to improve the driving strength of PUN, the chirality of PUN can be fixed at lower index i.e. (7, 0) that result PUN have high threshold voltage for proper level shifting. The chirality of PDN is fixed at medium value (22, 0) while the number of Nanotubes of PDN is kept at N=30 and analyse driving strength of the DCVS-LS circuit of PUN by varying the number of Nanotube from 1 to 7 as shown in Table-II. The PUN become stronger than PDN by increasing the number of Nanotubes above N=4. If any mismatch between PUN and PDN then output transition are very slow and contention current comes into picture for large duration. The DCVS-LS have lesser PDP by keeping N=7, but circuit is more susceptible by changing the diameter of CNTFET [26]. Reducing this problem due to statistical averaging by using more number of CNTs. Delay and power consumption is large if number of Nanotube is less N=4. So kipping number of Nanotube N=5 in the PDN for enhancing the performance. In next for optimize the PDP and reducing the contention current by varied the number of Nanotube of PDN. The number of Nanotube is varied from 15 to 40 as shown in Table-II. As the PUN is already stronger due to its N=4, and for reducing the contention current by increasing the number of nanotube of PDN at least N=25. Plot the contention current by varying the nanotube of PDN from 15 to 40. But PDP is still high at N=25 and N=40 equal to 0.1768 aJ and 0.3023 aJ respectively.

Because PDN getting stronger due to back gate bias offers stronger channel inversion [23] its large number of Nanotubes. When negative back gate bias voltage is 0.9V and N=25 the minimum PDP 0.0273 aJ is obtained.

IV. RESULTS AND DISCUSSION

All the simulation results are obtained by using BISM4, HSPICE model at 32nm by using Predictive Technology Model (PTM) , which requires a spice code (transistor-level net-list) of the desired circuit for the calculation of the parameters. As shown from Fig.4 DCVS level shifter, DCVS-LS circuit input V_{DDL}=0.2V and shifted output is at 0.9V there is amplification of signal take place and when number of Nanotube increase in PUN network power and delay decreases and overall PDP of the circuit also decreases and minimum.

Table.I. V_{DDH}=0.9V, V_{DDL}=0.2V PUN (7, 0) N=4 Pitch=5nm, PDN (22, 0) Pitch=20nm and N=40

Back gate Voltage (V) PUN	Power (nW)	Delay (ps)	PDP of N=40 (aJ)	Back gate Voltage (V) PDN	Power (nW)	Delay (ps)	PDP of N=40 (aJ)
0	0.8614	278.94	0.2402	0	0.8266	365.75	0.3023
0.1	0.8629	286.48	0.2472	- 0.1	0.7230	367.17	0.2654
0.2	0.8836	301.22	0.2661	- 0.2	0.5721	352.25	0.2015
0.3	0.8611	305.38	0.2629	- 0.3	0.4487	352.07	0.1579
0.4	0.8574	325.89	0.2794	- 0.4	0.4046	360.02	0.1456
0.5	0.8393	337.51	0.2832	- 0.5	0.3583	204.86	0.0734
0.6	0.8612	348.35	0.2999	- 0.6	0.3305	210.46	0.0695
0.7	0.9198	365.47	0.3361	- 0.7	0.2685	271.73	0.0729
0.8	0.9263	377.31	0.3495	- 0.8	0.2641	210.32	0.0555
0.9	0.9274	389.45	0.3611	- 0.9	0.2263	241.41	0.0546

Table.II. Back gate Voltage V_{DDH}=0.9V, V_{DDL}=0.2V PUN (7, 0) N=4 Pitch=5nm, PDN (22, 0) Pitch=20nm and N=25

Back gate Voltage (V) PUN	Power (nW)	Delay (ps)	PDP of N=25 (aJ)	Back gate Voltage (V) PDN	Power (nW)	Delay (ps)	PDP of N=25 (aJ)
0	0.5397	265.97	0.1435	0	0.5202	340.04	0.1768
0.1	0.5264	277.23	0.1459	- 0.1	0.4435	346.20	0.1535
0.2	0.5567	289.51	0.1611	- 0.2	0.2612	357.36	0.0933
0.3	0.5559	301.51	0.1676	- 0.3	0.2934	347.24	0.1018
0.4	0.5616	314.48	0.1766	- 0.4	0.2373	180.24	0.0427
0.5	0.5315	323.73	0.1720	- 0.5	0.2108	196.21	0.0413
0.6	0.5673	341.49	0.1937	- 0.6	0.1810	223.50	0.0404
0.7	0.5686	353.89	0.2012	- 0.7	0.1722	209.09	0.0360
0.8	0.5488	365.49	0.2005	- 0.8	0.1381	268.47	0.0370
0.9	0.5892	377.53	0.2224	- 0.9	0.1125	243.54	0.0273

***Gustavo A. Ruiz*, 1998 [2],** Proposed a new generate signal (*N*) in differential logic to design a ripple carry (RC) adder, carry look ahead (CLA) adder and binary carry look ahead (BCL) adder. Mathematical expression for signal (*N*) has been derived in this paper. The signal is used to enable iterative shared transistor structures in adders. Use of new generate signal in differential cascode voltage switch logic achieves better speed and lower area than a conventional logic. Based on this signal, circuits for above mentioned 32-bit adders have been fabricated in a standard 1.0 µm two level metal CMOS technology.

In SI-LS circuit if tube of PMOS of inverter-I is increases then power consumption rapidly increases and delay also increase and overall PDP also

increases. If the number of tube of NMOS increase in inverter-I, then power, delay and overall PDP increases.

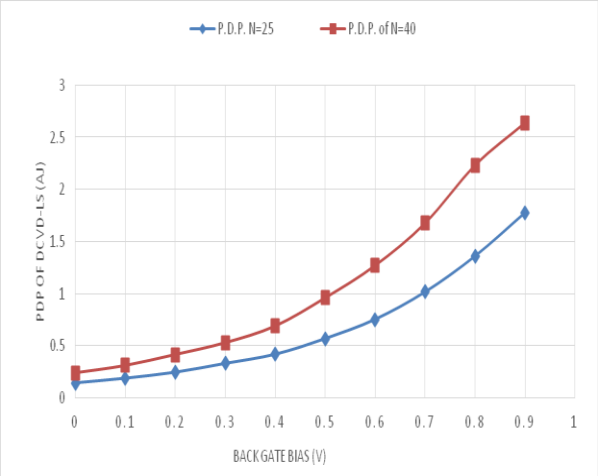

Fig.-5 Back Gate is applied to substrate which act as Second Gate. Plot of PDP for PDN with N=25 and N=40 in DCVS-LS

V. CONCLUSION

In this work, two basic level shifter circuit sviz. differential cascade voltage switch based level shifters and simple-inverter based level shifters are optimized for low power and high speed by using a novel device carbonnano tube FET at 32-nm node. By setting the required chirality, minimum PDP is obtained by varying the number of nanotubes and applying back gate bias. Problems such as contention current (due to current imbalance) in DCVS-LS and the static leakage in both DCVS-LS and SI-LS are addressed carefully by proper selection of chirality and threshold voltage. The obtained minimum power-delay product of the feedback- based level shifter (DCVS-LS) is 0.522aJ and that of multi-VTH based level shifter (SI-LS) is 0.730aJ, for the minimum input voltage of 0.2Vwhen it is unconverted to 0.9V.

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