A Comparative Study on Multi-Level Inverters Using SPWM

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Abstract *— Multilevel inverters are gaining more importance nowadays due to reduced total harmonic distortion (THD) and improved quality of output waveform. As the output voltage level increases, output harmonic content of such inverters decreases, allowing the use of smaller output filters. These multilevel inverters are used for high power applications and also in photovoltaic systems. This paper proposed the simulation models of various five level and seven level inverters. A comparative study based on various parameters like THD, device count, gain etc. are also performed. The simulation is done using MATLAB/Simulink software. The simulation results shows that the enhanced five level and enhanced seven level inverters gives better performance in terms of THD, gain etc. Also the hardware prototype of enhanced five level inverter is implemented.*

Keywords *— Diode-capacitor cell, SPWM, Enhanced five level inverter.*

I. INTRODUCTION

Renewable energy sources such as photovoltaic (PV) based systems are gaining more importance due to the advantages such as less environmental impact and improved economic benefits. With the rapid growth of power electronics technology, various converter topologies have been developed for PV systems. Among these topologies, multilevel inverters have been receiving significant interest. Multilevel inverters consist of series of semiconductor devices and capacitor voltage sources which will produce stepped output voltage waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. The harmonic content in the inverters decreases as the number of output voltage level increases allowing the use of smaller output filters.

For single-phase multilevel inverters, the most common topologies are the neutral-point clamped (NPC), flying capacitor(FC) and the cascaded H-bridges(CHB) types. In recent years, modular multilevel converter(MMC) has become an attractive topology due to its modularity, inherent redundancy, improved power quality and ease of expansion [5]. Nevertheless, the number of components used in MMC is not reduced and also two inductors are added. Various other multilevel topologies are existing with coupled inductors. This will increase the number of output voltage levels without the need for a number of DC sources and bulky capacitors. But the drawback is that coupled inductors are to be carefully designed.

The multilevel topologies mentioned above can only realize the voltage step-down inversion, i.e., the AC voltage amplitude cannot exceed the input DC voltage. A "transformerless" architecture is competent since it reduces the system cost, weight and also realizes the voltage step-up[6],[7]. But the existing architectures requires two DC sources and also more number of switches and diodes[6]. The step-up ratio of the boost converter has some limitations which restrict the step-up capability [7]. A high step-up inverter is discussed in [3] using the diode-capacitor cell and couple inductor. It uses less switches but just implements the two-level inversion.

Here a comparative study of various multilevel inverters using Sinusoidal Pulse Width Modulation(SPWM) are presented. All of them are made of switched-diode capacitor cell, but the gain offered by them are different. Based on the study the Multi Level Inverters (MLI) which provides good performance with reduced input is chosen for hardware implementation.

II. CIRCUIT TOPOLOGY OF MULTI-LEVEL INVERTERS

The various topologies existing for five level and seven level inverters are discussed below.

A. Conventional Cascaded H Bridge Five Level Inverter

Figure 1 shows a circuit of typical arrangement of Conventional Cascaded H Bridge (CCHB) five level inverter. It requires two separate DC voltage sources. Both of them can be of same voltage or of different magnitude. Here we require eight number of switches. Maximum inverter output voltage will be the sum of two input DC voltages.

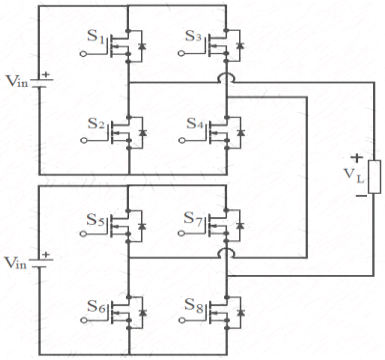

Fig. 1 CCHB Five level inverter

B. Cascaded Boost Five Level Inverter

Figure 2 shows a cascaded boost five level inverter with two diode capacitor cells in parallel. It consist of a switched-capacitor (SC) based boost converter and a two-level inverter connected in cascade. The DC multilevel voltage of the first stage becomes the input voltage of the classical inverter, resulting in a staircase waveform. No additional switches are provided for inductor charging and therefore gain will be less.

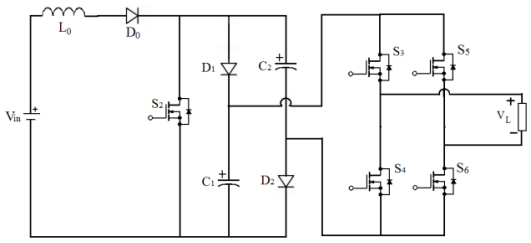

Fig. 2 Cascaded boost five level inverter

C. Enhanced Single Phase Step-up Five Level Inverter

Figure 3 shows single phase step-up five-level inverter. Apart from the conventional CHB inverter it uses only a single DC input voltage source. Its main parts are a conventional boost converter, a switch-diode-capacitor cell and an H-bridge. The diode-capacitor cell (D_1-C_1, D_2-C_2) and the inductor L_1 are used to boost the DC link voltage. The multilevel signal is generated by switch S_2 and the diode-capacitor cell. Here an additional switch S_1 is provided for sufficient charging of inductor. This topology ensures voltage step-up inversion.

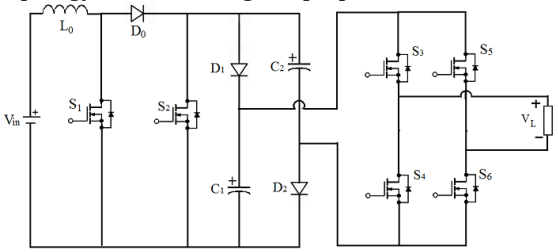

Fig. 3 Step-up five level inverter

D. Enhanced Seven Level Inverter

Enhanced seven level inverter is formed by two boost converters connected in series as shown in Figure 4. Each boost converter consists of two diode capacitor cell. The main disadvantage of this seven level inverter is that it requires two separate DC sources for each boost converter. The number of switches required is eight. The control circuit is complex. Since there are two boost circuits the gain provided is high.

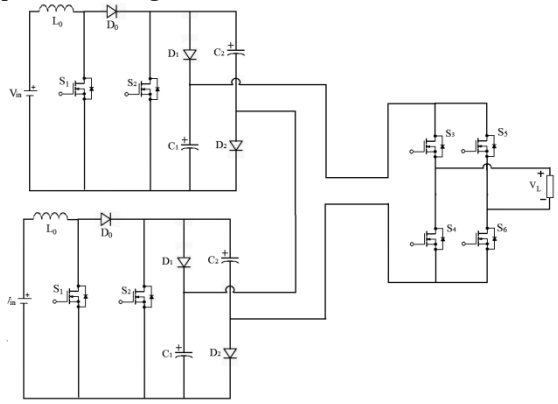

Fig. 4 Enhanced seven level inverter

E. Cascaded Seven Level Inverter

Cascaded seven level inverter is formed by three switched diode capacitor cells in parallel. It has two switches less than the enhanced seven level inverter. The levels are obtained by switching S_1 and S_2. There is no additional switch provided for charging inductor. It provides only low gain compared to enhanced seven level inverter.

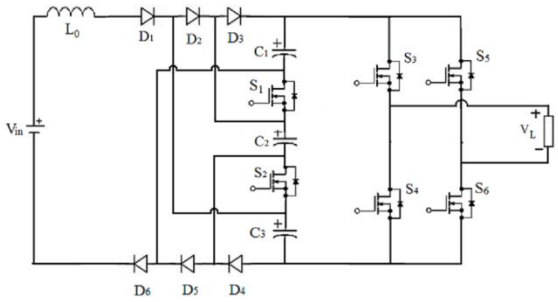

Fig. 5 Cascaded seven level inverter

III. WORKING OF ENHANCED STEP-UP FIVE LEVEL INVERTER

There are mainly 12 modes of operation for this five-level inverter. Six are for positive half cycle and remaining six are for negative half cycle. Depending on the ON and OFF position of switch S_2 capacitors C_1 and C_2 will be connected either in series or in parallel. When switch S_2 is turned on, diodes D_1 and D_2 are turned off, capacitors C_1 and C_2 will discharge in series. When switch S_2 is turned off, diodes D_1 and D_2 are turned on, capacitors C_1 and C_2 get charged in parallel.

The operating modes of the positive half sinusoidal cycle (modes 1-6) are discussed below.

A. Mode 1

S_1 is turned ON in this mode. The inductor L_0 is charged by the input DC source. Meanwhile, the load current flows through switch S_6 and antiparallel diode of S_4.

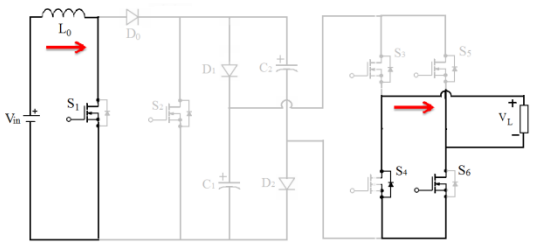

Fig. 6 Mode 1

B. Mode 2

S_1 is turned OFF in this mode. All diodes are in on state. The inductor L_0 is discharging and the input source is charging the diode-capacitor network. The load current flow is same as in mode 1.

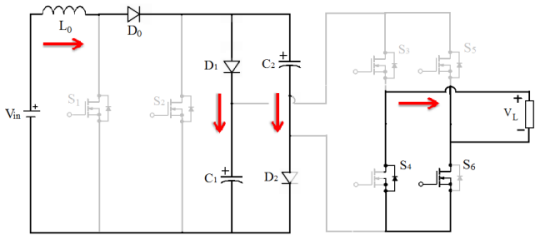

Fig. 7 Mode 2

C. Mode 3

Switch S_3 is made ON in this mode. The input DC source charges the diode-capacitor cell and simultaneously provides the power to the load.

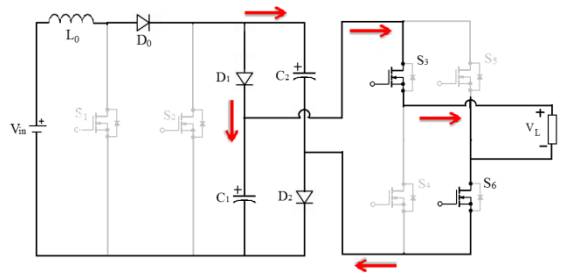

Fig. 8 Mode 3

D. Mode4

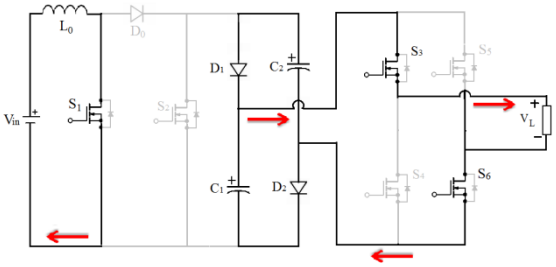

Fig. 9 Mode 4

Switch S_1 is turned ON again. capacitors C_1 and C_2 are working in parallel to feed the load.

E. Mode 5

S_1 stays in ON state and S_2 is turned ON in this mode. The capacitors C_1 and C_2 are connected in series supplying power to the AC load.

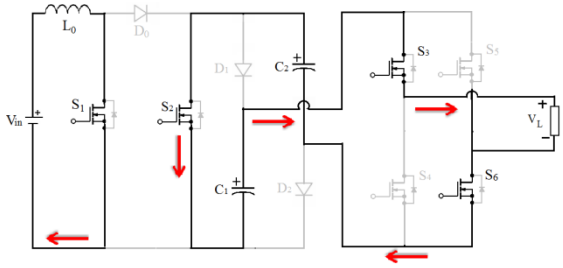

Fig. 10 Mode 5

F. Mode 6

S_2 stays in ON state. Similar to mode 5 operation, the capacitors C_1 and C_2 are connected in series supplying power to the load.

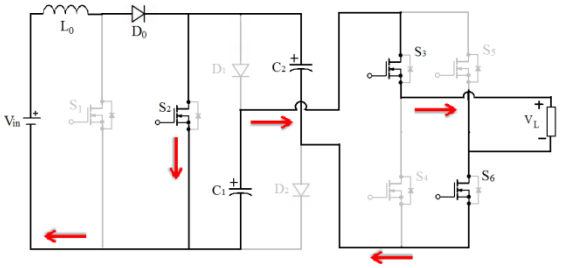

Fig. 11 Mode 6

IV. CONTROL STRATEGY

It make use of Rectified Sinusoidal Pulse Width Modulation(RSPWM) technique with rectified sinusoidal signal of 50Hz frequency as the modulating wave. Two triangular carriers of frequency 15 kHz and of equal magnitude is used and the gate pulses are generated by comparing modulating signal and corresponding triangular carrier. The parameters like gain, stress etc. of the step-up five level inverter circuit can be varied by varying the amplitude of the modulating signal.

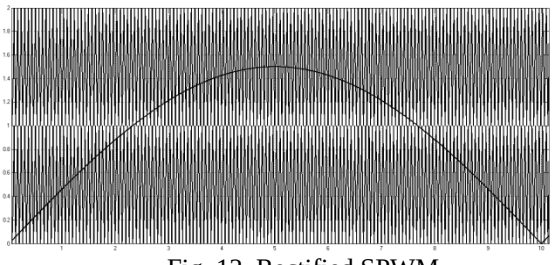

Fig. 12 Rectified SPWM

V. SIMULINK MODEL AND RESULTS

Table 1 describes the simulation parameters for the step-up multilevel inverter. Simulation is carried out using an input of 60V and switching frequency f_s of

15 kHz. Resistance of 200 ohm is used here as load and the voltage across the resistor is also measured.

Table 1 Simulation Parameters

Parameter	Symbol	Specification
Power Switches	S_1-S_6	IRF 540
Diodes	D_0, D_1, D_2	1N5819
Capacitors	C_1, C_2	330µF
Input Inductor	L_1	2mH
Load Resistor	R_L	200Ω

A. Simulink Model of Enhanced Five Level Inverter

The simulation is done using MATLAB/Simulink software. DC supply voltage of 60V is given. The THD is measured using a THD block.

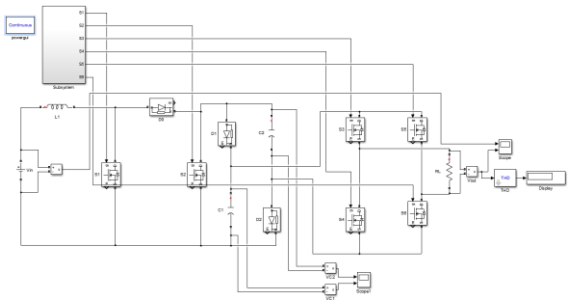

Fig. 13 Simulink model of enhanced five level inverter

B. Simulink Model of Pulse Generation Subsystem

Figure 14 shows the pulse generation subsystem for the sinusoidal pulse width modulation technique used in five level inverter. Two carriers and a single modulating signal is used. The frequency of carrier signals used is 15kHz. The amplitude of modulating signal used is 1.5. The rectified sinusoidal wave is obtained by using absolute block
in simulink library.

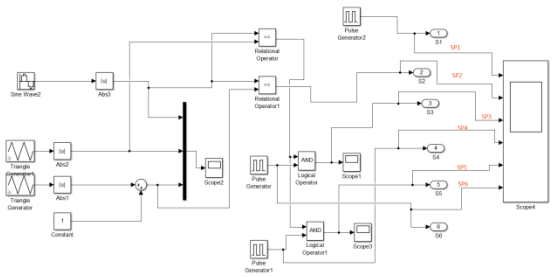

Fig. 14 Subsystem for pulse generation

C. Switching Pulses

Figure 15 shows the switching pulses for each switches in the inverter. Pulses are generated by using relational operators (>= and <=) and logical operators.

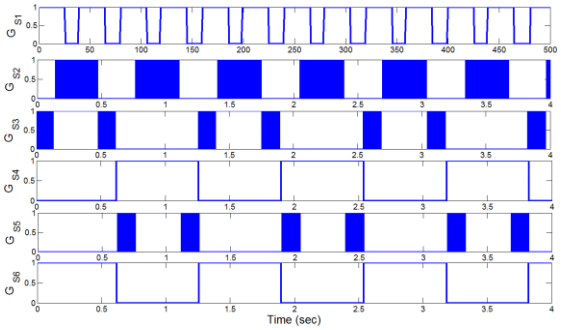

Fig. 15 Switching pulses

D. Output Voltage and Current

Figure 16 shows the output voltage and current of enhanced five level inverter. For an input voltage of 60V and switching frequency of 15kHz output voltage of 600V is obtained.

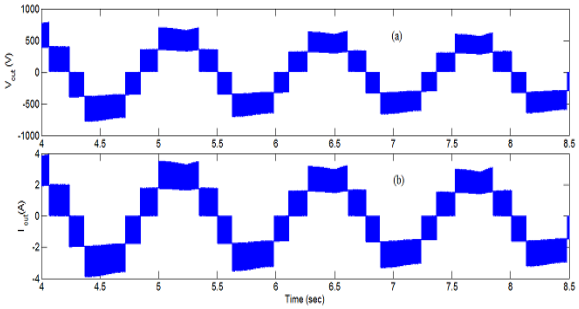

Fig. 16 Output (a) voltage (b) current

VI. COMPARATIVE STUDY

In Table 2 the various five level topologies are compared based on various parameters like THD, device count, gain etc. From the observation the step-up five level inverter gives the best result.

Table 2 Comparison of five level inverters

Five Level Inverters	Main Switches	No. of capacitors	No. of diodes	No. of voltage sources	THD %	Voltage Step-Up	Gain
5 Level cascaded inverter	8	0	8	2	40.23	No	1
Cascaded boost inverter	5	2	8	1	42.23	Yes	3.33
Step-up 5 level inverter	6	2	9	1	40	Yes	10

In the same manner the two topologies for seven level inverter is also compared. Even though the device count is more and number of voltage source required is two for enhanced seven level inverter these can be neglected when the gain and THD are considered.

Table 3 Comparison of seven level inverters

Seven Level Inverters	Main Switches	No. of capacitors	No. of diodes	No. of voltage sources	THD %	Voltage Step-Up	Gain
Enhanced 7 level	8	4	14	2	30.93	Yes	15
Cascaded 7 level	6	3	12	1	32	Yes	8.33

Table 4 shows the output voltage of various multi-level inverters for an input voltage of 30V. The enhanced seven level inverter gives maximum output voltage while cascaded five level inverter gives the least 60V which is the sum of two input voltage sources.

Table 4 Output voltage for 30V input

Inverter	Output voltage
5 Level cascaded inverter	60V
Cascaded boost 5 level	80V
Step-up 5 level inverter	300V
Enhanced 7 level	500V
Cascaded 7 level	200V

The voltage requirement for various multi-level inverters for 230V output is given in the Table 5.

Table 5 Input voltage for 230V output

Inverter	Input voltage
5 Level cascaded inverter	115V
Cascaded boost 5 level	80V
Step-up 5 level inverter	23V
Enhanced 7 level	8V
Cascaded 7 level	30V

VII. EXPERIMENTAL SETUP AND RESULTS

A prototype of enhanced step-up five level inverter is implemented. For the hardware prototype a 330µF capacitor, 100Ω ,5W load resistor and IRF540 switches are used. Control pulses for MOSFET switches are generated using PIC microcontroller. Control pulse is amplified by driver circuit composed of TLP250. It also provides isolation between control and power circuit. The experimental setup is shown in Figure 17.

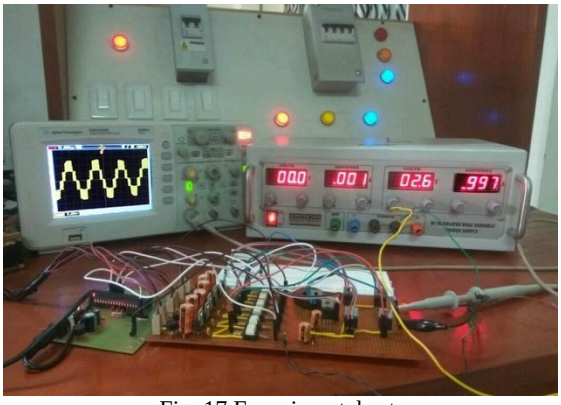

Fig. 17 Experimental setup

For the experimental verification an input voltage of 2.5V is given. The capacitors are charged up to a voltage of 7.5V. The output obtained is 50Hz staircase waveform having maximum output voltage of 15V. The output waveform is shown in Figure 18.

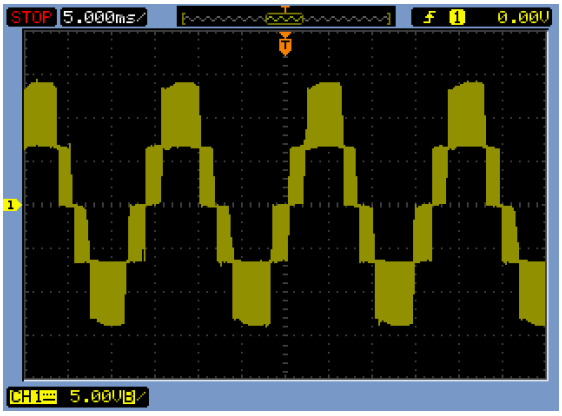

Fig. 18 Output voltage

VIII. CONCLUSION

A comparative study of various multilevel inverters are performed. From the analysis it is found that among five level inverters the step-up five level inverter gives high gain with reduced device count with reduced voltage stress. Similarly among seven level inverters, enhanced seven level inverter gives high gain with reduced THD. Although the device count is more when compared with cascaded seven level inverter the enhanced seven level gives better performance with a gain of 15. Voltage gain increased by 70% for five level inverters and 46% for seven level inverters compared to corresponding cascaded topologies. Prototype of five level inverter is also implemented and the result is verified.

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