Comparative Analysis of Performance in Domino Logic For Wide Fan-in Gates

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Abstract:- *As the in semiconductor industries progress by following Moore's law faithfully from last five decades, and integrating more transistors along with functional circuits on a single chip periodically with every coming process technology. However, this progress help in rapid run towards tiny, circuit design high speed and economical VLSI (Very Large Scale of Integration) circuits has added to excessive power dissipation of numerous circuits used today. Therefore the leakage current and power dissipation becomes increasingly more focused in VLSI circuit design. Carbon Nanotube Field Effect Transistor (CNFETs) is suited best alternatives to the conventional CMOS based devices. During various simulation results, unexpected reduction in process variation, ultra low (nano-scaled) power memory devices and superior improvement of Noise Margin, propagation delay, write-read margin and its stability is found. CNFETs based logic gates are compared with Conventional CMOS and FinFET based logic gates in respect to delay and power consumption.*

Keywords— ***CNT, CNFET, Power Dissipation, Logic Gates.***

I. INTRODUCTION

Continuously progress in the field of nanotechnology rover the world on System on chip (SOC) with the help of novel nanomaterials. The challenges for continued device scaling as well as accepting the Moore's statement is now taken by researchers and they are continuing to scale down the dimensions with new era of technology and novel materials. Scaling from micro to nano dimension, we faces many challenges like short circuit channel effect, increasing the leakage current, severe process variations, high power density and instability of the system performance in the devices. CNFET that has popularly received much attention from past few years as a valuable candidate for accepting all the challenges as mentioned above. The structure of CNFET provides a MOSFET-like (Si based) behavior with yet ballistic or quasi-ballistic transport [1], [2]. The source and drain regions are heavily doped and since the source–drain distances under 100 nm, the carrier concentration transport is ballistic at both high and low voltages. High drivility of current flow through the CNT lies on: a) the features of the ballistic transport and b) the specific electron arrest along the nanotube [3]. The main feature of CNT is that the threshold voltage as well as bandgap energy can be properly varying with the help of chiral vector only (i.e., the diameter). Ultrathin body devices such as FinFETs, CNFET and CNFET based nano memory devices have received an increasing attention in recent years.

Paper is detailed as follows: Section 2 shows the fundamentals of Carbon Nano Tube. Section 3, explores the theory of Domino Circuits. In section 4, we present the Simulation results of CNT based logic gates and Finally Conclusion is offered in section 5.

2. Carbon NanoTube (CNT)

CNT is in hexagonal lattice structure of carbon rolled into a cylindrical form. Carbon belongs same group in the periodic table as silicon with four valence electrons in its outermost shell. S.Iijima in 1991[4] was the father of CNTs who discover large molecular that are unique for their size, shape and superior physical properties. The strength and stability is due to the SP^2-bonds between C-C (carbon-carbon) atoms and this bond in CNT is stronger than SP^3 bonds as in diamond. Single walled and multiwall carbon nanotubes (SWCNT & MWCNT) are its types. The conducting or semiconducting behavior depends on the chirality vector which is defined as the direction angle in which the graphene structure is folded. The structural orientation is geometrically represented by the indices *n* and *m* which are used to calculate the diameter and the helicity angle of the CNT and also determine its fundamental properties [5], [6], [7]. Semiconducting or metallic behavior of carbon nanotube is depends on its indexes (n, m): the tube conducts semiconducting property if $n \neq m$ or $n-m \neq 3i$, where i is an integer. The possible structures are defined as armchair, zigzag and chiral. In this paper, only SWCNT and Zigzag structure (n, 0) is accounted for calculation of all parameters. Three or four SWCNTs are used in parallel with equal spacing (pitch distance) to carry a large amount of current. CNTs exhibit one-dimensional (1D) carrier transport which greatly reduces the scattering probability phenomena and therefore provides to a large mean free path, high current carrying capability and shows excellent thermal, mechanical and electrical properties [8-10].

Rolled-Up vector:

$$C_h = na_1 + ma_2 \quad \text{.....Chiral Vector}$$

$$L = \text{Modulus of } C_h = a\sqrt{(m^2+n^2+mn)} \quad \text{…length of tube}$$

Chirality Vector & Bandgap Energy:

Table 1. Bandgap Energy of CNT with various Chiral Vectors.

Material	Chirality Vector	Bandgap Energy
CNT	10,0	0.98
CNT	11,0	0.95
CNT	13,0	0.76
CNT	14,0	0.74
CNT	16,0	0.62
CNT	17,0	0.61
CNT	19,0	0.52
CNT	20,0	0.51
CNT	22,0	0.45

Threshold Voltage:

It is defined as the voltage required to on the transistor and it is related with inverse of the diameter of the tube. In a CNT, the threshold voltage can be varied by proper selection of chirality vector. V_{th} can be calculated by using equation (3) as:

$$V_{th} = Eg/2e = \frac{\frac{\sqrt{3}}{3}aV\pi}{e*D_{CNT}}$$

Where Eg = Band-gap energy = 0.83/ D_{CNT} e*V*, *a* =is the c-c bond distance= 2.49 °A, $V\pi$ represents the carbon π–π bonding values in electron volts (=3.033 eV.)

Tube Diameter: The diameter of the tube is evaluated with the help of the expression [11-13].

$$D_{CNT} = \frac{C_h}{\pi} = \frac{a}{\pi}\sqrt{(n^2 + nm + m^2)}$$

Field Effect Transistor (CNFET)

The properties represented by the carbon nanotube aggressively replaced Si and Si based devices and hence there is a new revolution in the field very large scale of integration (VLSI) in nano terms. With this revolution, we can accept the challenges of getting the circuit reliability when dimensions reduced further. Now a day, it is nano-fabrication revolution and beyond scaling of conventional bulky CMOS, the CNT based FET (as shown in Fig.1) technology with high thermal stability, superior controlled in process variation, excellent gate controbility and very high drive current is now achieved. CNFET devices are made by growing nanotubes on top of a thick silicon dioxide. The nanotube plays a role of channel between source and drain [14] for conduction. CNFET provides very fast switching speed and shows very low power consumption even at nano sacle design. Hence due its extraordinary properties, a high stability, nanomemory, ultra-low power consumption devices with the replacement of Si is possible. The threshold voltage of CNFET is depends on the chirality vector and diameter of the CNT (D_{CNT}). The threshold voltage of CNFET is uniquely controlled with the variation of D_{CNT}.

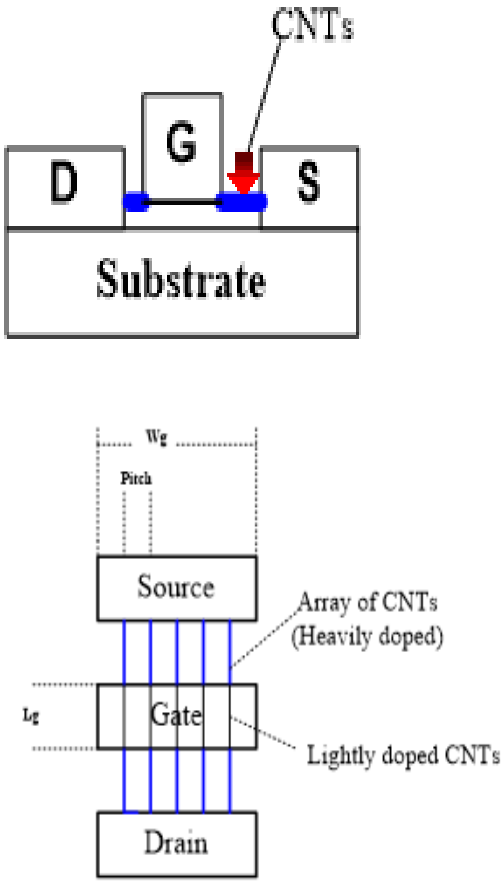

Fig.1: Simple Cross-sectional and Top-view Structure of CNFET

3. Literature review

The basic dynamic logic is Standard Footless Domino Logic (SFLD) circuit as shown in Fig. 2. In domino logic the evaluation phase major concern is reduction of leakage currents through PDN, even all inputs are at low logic level. This leakage current is due to band-to-band tunneling (BTBT) current, gate tunneling current and subthreshold leakage current. In standard domino P-CNT keeper transistor prevent from undesirable discharge of the dynamic node due to leakage current and charge sharing from PDN during evaluation phase. In this way noise immunity of circuit improve.

The keeper ratio *K* is defined as

$$K = \frac{\mu_P\left(\frac{W}{L}\right)_{Keeper-transistor}}{\mu_n\left(\frac{W}{L}\right)_{evaluation-network}}$$

Where *W* and *L* are the transistor size, and μ_n and μ_p are the mobility of electron and hole, respectively. Nowadays traditional keeper is less effective in ultra-deep submicron regime of CMOS technology, to improve noise immunity of dynamic logic by upsizing of the keeper, that increase contention current between keeper transistor and the evaluation network or PDN i.e. wide OR logic gate.

Thus in the SFLD circuit, power and delay increases, this makes critical problem in wide fan-in dynamic gate due to

large number of N-CNTFET transistor are connected at dynamic node [4]. So there is trade-off between noise immunity and performance due to limitation in pull-down legs. Numerous technique are proposed to address these issue. These are divided into two groups, in the first group circuit techniques changes the controlling circuit of the gate voltage of keeper such as conditional-keeper domino (CKD) [11], high-speed domino (HSD) [12], leakage current replica (LCR) keeper domino [13], and controlled keeper by current-comparison domino (CKCCD) [14], as shown in Fig.3(a)-(d)

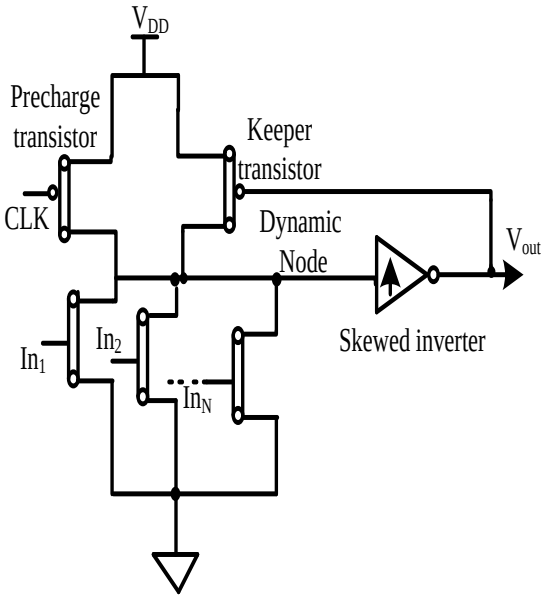

Fig.2 SFLD

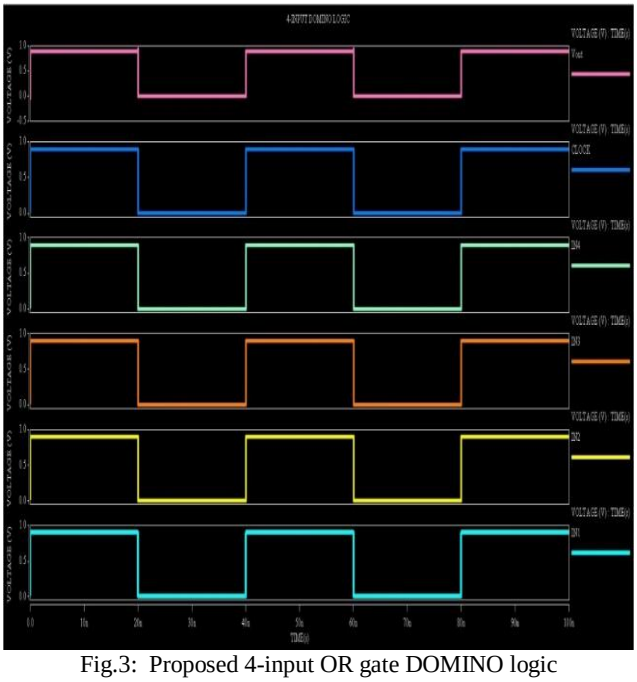

Fig.3: Proposed 4-input OR gate DOMINO logic

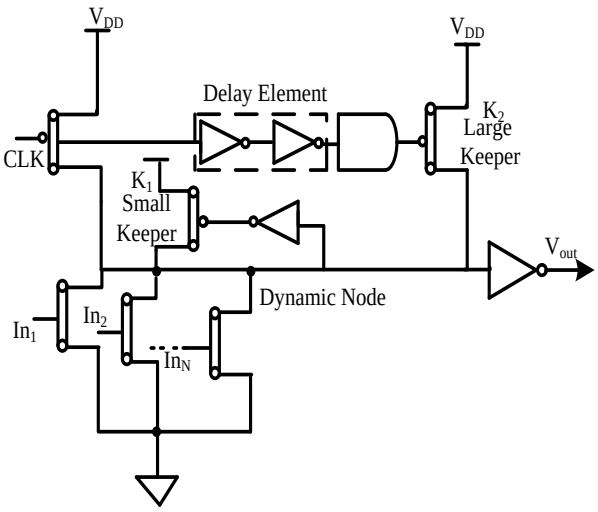

Fig.4: CKD

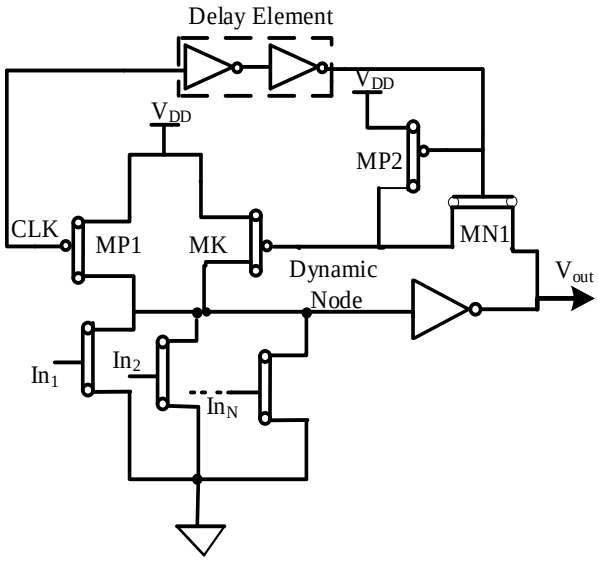

Fig.5: HSDL

4. Simulation Results

BISM 4 device model (PTM) is used for simulating the standard dual-V_t domino logic and proposed technique circuits for accurate estimation of subthreshold and gate oxide leakage currents. Following circuits are simulated in a 32 nm CNTFET technology ($V_{tnlow} = |V_{tplow}| = 0.22$ V, $V_{tnhigh} = |V_{tphigh}| = 0.446$ V, V_{DD}=0.8 V and output capacitance C_{out}=1 fF) 2-input domino AND gate (AND2), 2-input, 4-input and 8-input domino OR gates (OR2, OR4 and OR8 respectively). All these circuits are designed with standard dual-V_t domino and proposed lector dual-V_t technique. To have a reasonable comparison the sizing of NMOS and PMOS are equal in both the technique circuits. For measuring active power consumption clock pulse of 30 ns is applied and measured for low and high inputs at low and high die temperatures.

Table II: Comparison of various domino topologies in CMOS logic on Power, Delay and UNG for 2 and 4 input OR gates

	2 INPUT OR GATE			4 INPUT OR GATE		
Topology	Avg. Power(uW)	Avg. Delay(pS)	UNG	Avg. Power(uW)	Avg. Delay(pS)	UNG
FDL	0.369	28.83	0.382	0.393	30.45	0.525
FLDL	0.371	27.21	0.355	0.382	28.01	0.494
CMFD	0.799	24.46	0.613	0.580	169.5	0.788
HSCD	0.489	34.82	0.397	0.501	36.42	0.532
M-HSCD	0.669	51.18	0.396	0.673	49.95	0.538
CEDL	0.518	34.57	0.394	0.532	36.26	0.532
CSK-DL	0.601	38.44	0.392	0.621	41.32	0.532

Table III: Comparison of various domino topologies in CMOS logic on Power, Delay and UNG for 8 and 16 input OR gates

	8 INPUT OR GATE			16 INPUT OR GATE		
Topology	Avg. Power(uW)	Avg. Delay(pS)	UNG	Avg. Power(uW)	Avg. Delay(pS)	UNG
FDL	0.413	32.21	0.361	0.376	36.41	0.341
FLDL	0.433	31.52	0.312	0.338	32.49	0.312
CMFD	0.581	30.23	0.668	0.560	174.3	0.616
HSCD	0.528	38.15	0.382	0.470	41.75	0.343
M-HSCD	0.694	50.83	0.388	0.620	52.61	0.345
CEDL	0.548	38.11	0.383	0.482	41.76	0.342
CSK-DL	0.645	45.15	0.384	0.604	52.02	0.342

From the results shown in Table II and III, it is seen that proposed domino logic has lesser power consumption and higher unity noise gain at the cost increased delay as compared to other domino logic styles.

In all the topologies discussed above are designed and simulated using FinFET and CNTFET technology in PTM 32nm process for 2,4, 8 and 16 input OR gates.

5. Conclusion

The leakage current of the evaluation network of dynamic node is dramatically increased with scaling of technology, mainly in wide fan-in dynamic-OR gates, reduced noise immunity and increased power consumption. So, new designs is use with CNTFET to obtain desired noise robustness in wide fan-in circuits. Also increasing the fan-in not only reducing the worst case delay, it also increased the contention between the keeper transistor and the evaluation network. Simulation results show that the proposed technique using with CNTFET based domino circuit has much lesser contention current, high noise immunity, less temperature dependence and lowest power consumption for wide fan-in OR gates compared to the conventional designs.
So, that the proposed circuit is especially suitable for wide fan-in OR gates which are mainly used in high performance applications like microprocessors.

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