Design and Analysis of Low Power High Speed 9T SRAM Design in Nanometer Regime

Rahul Baghel[#1], Suresh S Gawande[#2],
[#] PG Student [VLSI], Dept. of ECE, Bhabha Engineering Research Institute, Bhopal, RGPV Bhopal, M.P. India

Abstract:- *Nowadays low power SRAMs have become a critical component of many VLSI chips. This is especially true for microprocessors, where the demands of cache sizes chip are growing with each generation to abridge the increasing divergence in the speeds of the processors and the main memory. In the current scenario, power dissipation is performing an important role while designing integrated circuits and calculating their operating speeds, as well as low power dissipation is also requisite due to the high growth of battery operated applications. In this paper we have compared existing 4T, 6T, 7T, 8T and 9T SRAM cell with proposed 9T at 65nm and 45nm technology and analysed in terms power consumption, delay and PDP with supply voltage of 1V at 100MHz frequency.The proposed circuit reduces power consumption upto 34% when compared with other existing technique.*

Keywords— *SRAM, SNM, Power consumption, PDP*

I.INTRODUCTION

The fast low power SRAMs have become a critical components of many VLSI chips. This is especially true for microprocessors, where the on-chip memory cell sizes are growing with each generation to abridge the increasing divergence in the speeds of the processor and the main memory. The power dissipation has become an important consideration due to the increased integration, operating speeds and the explosive growth of battery operated appliances. The leakage current of the memory will be increased with the increased ICs such that more power will be consumed even in the standby mode. These on-chip memory cells are usually implemented using arrays of densely packed SRAM cells for high performance [1]. A six transistor SRAM cell (6T SRAM cell) is conventionally used as the memory cell [2]. However, the 6T SRAM cell produces a cell size an order of magnitude larger than that of a DRAM cell, which results in a low memory density [2]. Therefore, conventional SRAMs that use the 6T SRAM cell have difficulty meeting the growing demand for a larger memory capacity in mobile applications [2]. The studies show that the power dissipated by the cell is usually a significant part of the total chip power [1]. Cell accessing consumes a significant fraction (30-60%) of total power dissipation in modem microprocessor [3]. A large portion of cell energy is dissipated in driving the bit-lines, which are heavily loaded with multiple storage cells [3]. Clearly, the memory cells are the most attractive targets for power reduction [1]. Besides, in cell accesses an overwhelming majority of the write and read bits are '0'. whereas in the conventional SRAM cell because one of two bit-lines must be discharged to low regardless of written value, the power consumption in both writing '0' and '1' are the generally same [1]. Also in conventional SRAM cell differential read bit-line used during read operation and consequently, one of the two bit-lines must be discharged regardless of the stored data value [3]. Therefore always there are transitions on bit lines in both writing '0' and reading '0' and since in cell accesses an overwhelming majority of the write and read bits are "0" these cause high dynamic power consumption during read/write operation in conventional SRAM cell.

II. Literature Review

Ajoy C A, Arun Kumar, March 2014: The main objective of this paper is to design a power efficient SRAM cell. The traditional SRAM makes use of six transistors that consumes more power and stability for read operation is less. As a substitution by using low power design techniques the power consumption is being reduced. Here the low power logic used is sleepy approach. In the sleep approach, an additional “sleep” PMOS transistor is placed between VDD and the pull-up network of a circuit and an additional “sleep” NMOS transistor is placed between the pull-down network and GND. Also by using dynamic cell supply power is reduced. Pre-charge circuit is used for pre-charging the bit lines. The current mirror sensing amplifier is used for read operation. A. Islam & M. Hasan, March 2012: This paper presents a technique for designing a low-power and variability-aware SRAM cell. The cell achieves low power dissipation due to its series-connected tail transistor and read buffers, which offer a stacking effect. Sushil Bhushan & Shishir Rastogi, Oct. 2011: This paper presents a CMOS four-transistor SRAM cell for very high density and low power embedded SRAM applications as well as for stand-alone SRAM applications. The new cell size is 35.45% smaller than a conventional

six transistor cell using same design rules. Also proposed cell uses two word-lines and one pair bit-line. Shyam AKASHE & Sanjay SHARMA, Number 2012: This paper is based on the observation of a CMOS five-transistor SRAM cell (5T SRAM cell) for very high density and low power applications. This cell retains its data with leakage current and positive feedback without refresh cycle. This 5T SRAM cell uses one word-line and one bit-line and extra read-line control. The new cell size is 21.66% smaller than a conventional six-transistor SRAM cell using same design rules with no performance degradation. Kang S.M. & Leblebici Y., 2003: The electronics industry has achieved a phenomenal growth over the last few decades, mainly due to the rapid advances in integration technologies and large-scale systems design. The use of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been growing at a very fast pace.

2.1 STATIC RANDOM ACCESS MEMORY (SRAM)

Static memory cells [4] basically consist of two back to back connected inverters as seen in Fig.1. The output of the second inverter (Vo2) is connected to the input of the first inverter (Vi1). If we consider the voltage transfer characteristics of the first inverter (Vo1 vs.Vi1) and that of the second consideringVi2=Vo1, there are three possible operating points (A, B and C) obtained by intersection. It may be seen that the operation points A, B are stable as loop gain is less than 1. Point A shows that the output of inverter1 is high and the output of the inverter2 is low. Point B shows that the output of inverter1 is low and the output of inverter2 is high. This shows that the outputs of two inverters are complementary in any stable condition. This property is made use of to realize static random access memory SRAM.

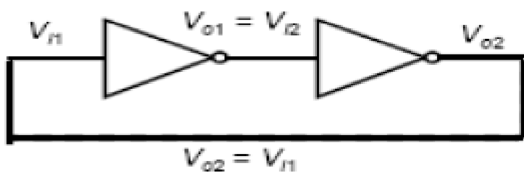

Fig.1. Back to back connected inverters in SRAM

2.2 CONVENTIONAL 6T SRAM CELL

The SRAM cell is used to store the binary information as a key component. A normal SRAM cell forms a latch and access transistor by the utilization of two cross-coupled inverters and these access transistors allow access to the cell during read and write operations and provide cell separation during the not-accessed state [5]. To Provide write stability, data storage (or data retention) and non-destructive read access a SRAM is designed for cell is powered. An analysis and design of different SRAM cells are: Conventional 6T, 7T, 8T, 9T and improved 8T.

A. CONSTRUCTION

They are compared with respect to power, delay and speed. Normally, the cell design must strike a balance between delay, speed, durability, cell area and leakage but power reduction is one of the most important design objectives. However, without compromising the other parameters power cannot be reduced. For the example, low-power can compromise the cell area and also the speed of operations. In Fig.2. a typical six-transistor (6T) CMOS SRAM cell is shown. Figure shows four transistors (M1−M4) comprise cross-coupled CMOS inverters and two NMOS transistors M5 and M6 provide read and write access to the cell. 6T CMOS SRAM cell is very famous due to its superior durability, low-voltage and low power operation [6].

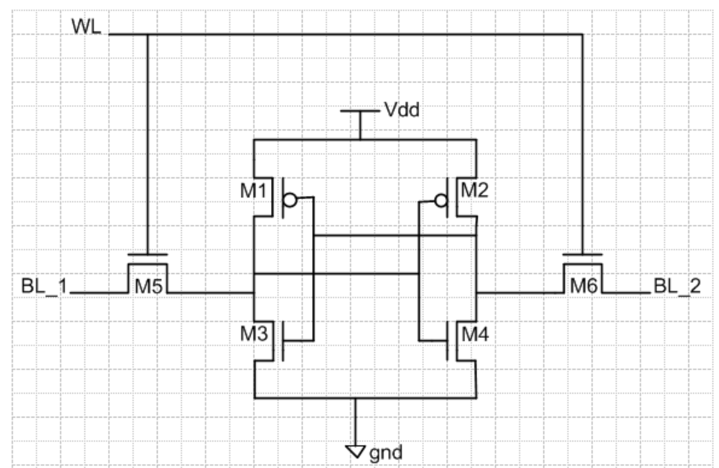

Fig.2. Conventional 6T SRAM cell

B. OPERATION OF SRAM

The Static Random Access memory device can perform the operation which is as follows: hold, read and write.

a. HOLD: The access transistors M5 and M6 disconnect the cell from the bit lines, if the word line is not asserted. The two cross coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply.

b. READ:

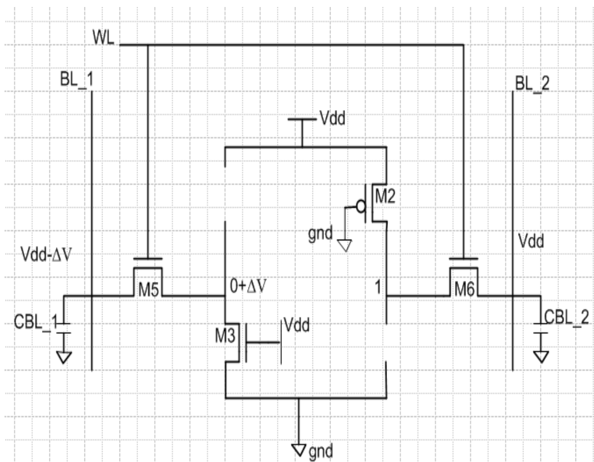

Fig. 3. Read Operation of SRAM Cell.

The bit lines are pre-charged to V_{DD} prior to initiating a read operation. The read operation is started by empowering the word line (WL) and connecting the pre-charged bit lines (BL_1 and BL_2) to the internal nodes of the cell. On read access, the bit line voltage VBL remains at the pre-charge level as shown in Fig. 3. The complementary bit line voltage VBLB is discharged through transistors M1 and M5 connected in series. Conclusively, transistors M1 and M5 form a voltage divider whose output is now no longer at zero volts and is connected to the input of inverter M2−M4 (as in Figure 3.7.1). The sizing of M1 and M5 should ensure that inverter M2−M4 do not switch causing a destructive read [7-8].

c. WRITE:

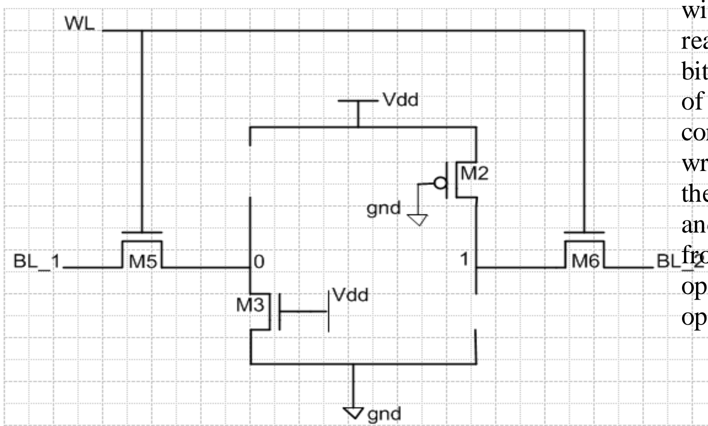

Fig.4. Write Operation of SRAM Cell.

2.3 7T SRAM

While the write operation one of the bit lines i.e. BL in Fig.4. is driven from pre-charged value (V_{DD}) to the ground potential by a write driver through transistor M6. The cell is flipped and its data is effectively overwritten if transistors M4 and M6 are properly sized. A statistical measure of SRAM cell write ability is defined as write margin. The write margin is defined as the minimum bit line voltage required flipping the state of an SRAM cell.The write margin value and variation is a function of the process variation, SRAM array size and cell design. A cell is considered not writeable if the worst-case write margin becomes lower than the ground potential. The write operation is applied to the node storing a '1'. It is necessitated by the non-destructive read constraint that ensures that a '0' node does not exceed the switching threshold of inverter M2–M4. The only function of pull-up transistors is to maintain the high level on the '1' storage node and prevent its discharge by the off-state leakage current of the driver transistor during data retention and to provide the low-to-high transition during overwriting [8].

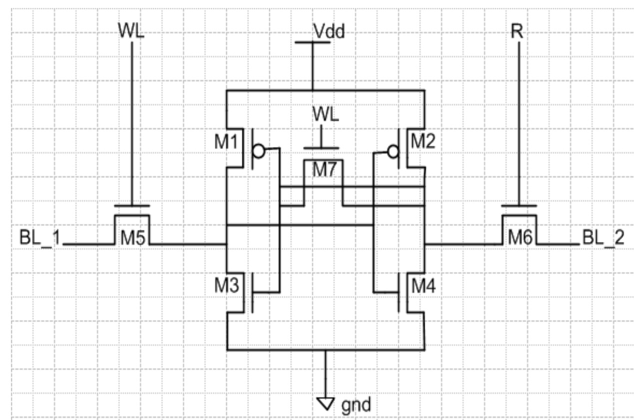

Fig.5. 7T SRAM cell

The circuit of 7T SRAM cell is made of two CMOS inverters that are connected cross coupled to each other with additional NMOS Transistor which is connected to read line and has two pass NMOS transistors connected to bit lines and bit line bar respectively. Fig.5. shows circuit of 7T SRAM Cell, where the access transistors M5 is connected to the word-line (WL) to perform the access write and M6 is connected to the Read-line (R) to perform the read operations thought the column bit-lines (BL_1 and BL_2). The bit-lines act as I/O nodes carrying the data from SRAM cells to a sense amplifier during read operation or from write in the memory cells during write operations [10-12].

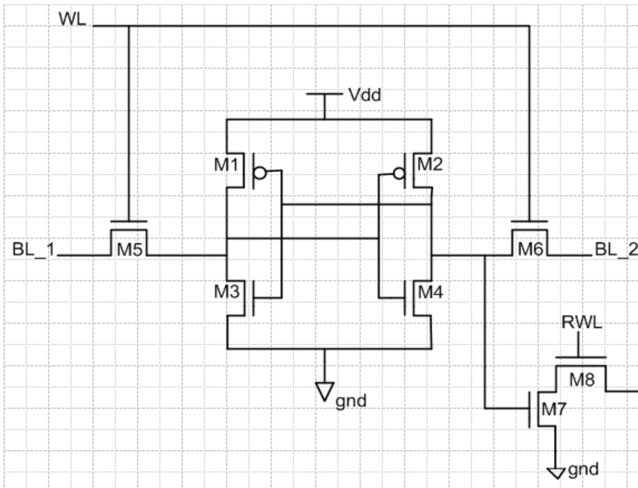

Fig.6. 8T SRAM cell

2.4 8T SRAM cell

The 8T SRAM circuit is presented in this section. The schematic of the 8T SRAM cell sized for a 65nm CMOS technology is shown in Fig.6. The left sub-circuit of the 8T memory cell is a conventional 6T SRAM cell with minimum sized devices (composed of M1, M2, M3, M4, M5, and M6). Two data access transistors (M5 and M6) and two bit lines (BL_1 and BL_2) are used for writing to the SRAM cell. An alternative communication channel (composed of a separate read bit line RBL and the transistor stack formed by M7 and M8) is used for reading the data from the cell [13].

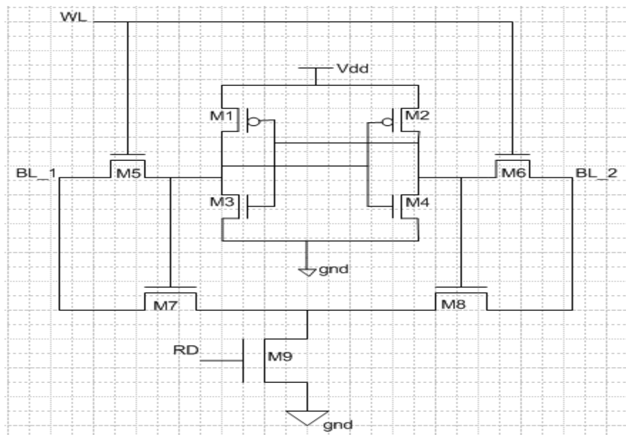

Fig.7. 9T SRAM cell

2.5 9T SRAM Cell

A 9T SRAM cell is presented in Fig.7. The upper sub-circuit of the new memory cell is essentially a 6T SRAM cell with minimum sized devices (composed of M1, M2, M3, M4, M5, and M6). The two write access transistors (M5 and M6) are controlled by a write signal (WL). The data is stored within this upper memory sub-circuit. The lower sub-circuit of the new cell is composed of the bit-line access transistors (M7 and M8) and the read access transistor (M9). The operations of M7 and M8 are controlled by the data stored in the cell. M9 is controlled by a separate read signal (RD). During a write operation, WL signal transitions high while RD is maintained low, M9 is cut-off. The two write access transistors M5 and M6 are turned on. In order to write a "0" to Node1, BL_1 and BL_2 are discharged and charged, respectively. A "0" is forced into the SRAM cell through M5. Alternatively, for writing a "0" to Node2, BL_1 and BL_2 are charged and discharged, respectively.

III. Proposed Work

The Proposed circuit is shown in Fig. 8. Here in this the two extra PMOS transistor M_8 and M_9 have been used in the pull down network. Because of the stacking of these two PMOS transistors in Pull Down network a voltage drop occurs across them. There is an NMOS transistor in parallel of PMOS stack in pull down network which is sometimes called evaluation transistor. Therefore when the pull down network is in standby mode this PMOS stack reduces the leakage current which directly reduces the leakage power consumption of the circuit. The overall power consumption of the circuit is also reduced by using this technique. The modified design uses a stack of PMOS transistor that has been added in the SRAM cell, the schematic and configuration of this approach work in a manner so that it can reduce the leakage power from supply towards ground and indirectly reduces the power dissipation.

The transistors are held in reverse body bias. This reverse body biasing increases their threshold. This increased threshold voltage results in low leakage current and hence low leakage power. Because as result their threshold is high, higher threshold voltage causes low leakage current and therefore low leakage power. If we use minimum size of transistors, i.e. aspect ratio of 1, we yet again get low leakage power due to low leakage current. In Proposed 9T SRAM, write time and Signal to Noise Margin (SNM) improves with smaller penalty of delay by increasing of number of transistors. Fig.9. Shows the transient response of proposed circuit it BL and BLB is the bit line provided from transistor M5 and M6 and W/L is word line to run two back to back inverters which is shown in output waveform, where proposed circuit achieves proper logic level.

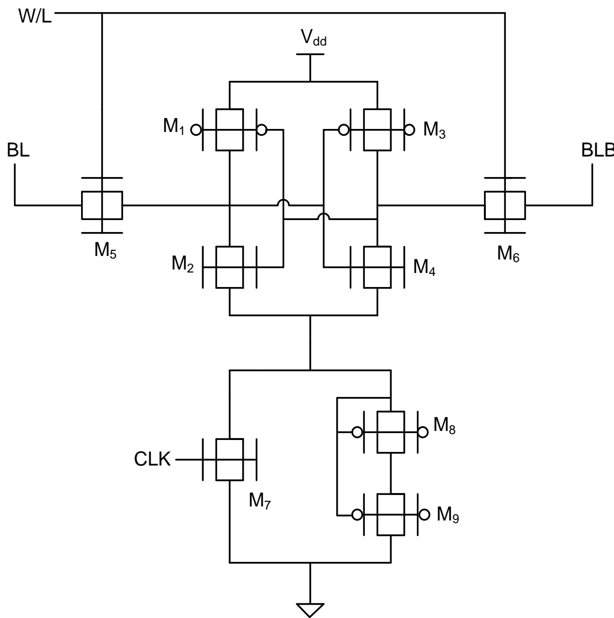

Fig.8. Proposed 9T SRAM

Bit-interleaving and shared word line architectures

Mainly two ways are used to arrange the words in SRAM architecture. Shared word line shown in Fig. 5(a) and bit interleaving shown in Fig. 5(b). A simple SRAM memory architecture as shown in Fig. 5 consists of a matrix of cells made of rows and columns. The rows are selected by the address signal generated by the row decoder. The columns are selected by the address generated by the column decoder. As shown in Fig.6 A3, A4, A5 and A6 are the address signals to select the rows and A0, A1 and A2 are the address signals to select the columns. If M X N is the size of the memory then the number of address lines needed to decode rows is ‘m’ where M is equal to 2m and the number address lines needed to decode columns is ‘n’ where N is equal to 2n [10].

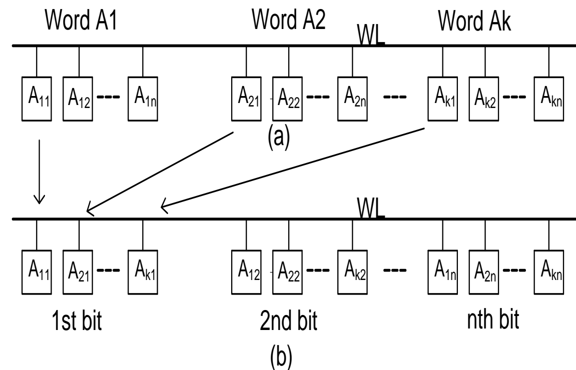

Fig.9: SRAM word organization (a) Shared word line (b) Bit-interleaving

IV. Results and Discussion

In this table the results of 9T, 8T, 7T, 6T and Improved 4T SRAM cells are compared at the basis of parameters Power consumption, Delay and Static Noise Margin. In Table1, The proposed improved 4T SRAM cell shows maximum reduction in power consumption of 24.17% with 6T, of 88.6% with 7T, of 28.21% with 8T and of 35.03% with 9T, maximum reduction in delay of 9.1% with 6T, of 64.26% with 7T, of 9.18% with 8T and of 10.44%.

Table.I. Average Power and Delay of SRAMs Cells

SRAMS	Average Power Consumption(μW)		Delay (pS)			
			65nm		45nm	
			Max	Min	Max	Min
	65nm	45nm				
4T	0.1441	0.2332	19.377	7.8591	15.359	9.6706
6T	13.268	22.357	8.0884	7.7477	6.6294	4.5591
7T	16.718	30.195	7.3579	2.7535	1.5025	0.6312
8T	3.8619	6.1349	10.492	8.5582	3.1342	1.4681
9T	24.551	38.123	8.5957	8.0088	6.0005	3.7416
Proposed 9T	2.8124	3.2671	7.2981	6.9261	4.1872	2.1826

Table.II. PDP of SRAMs Cells

SRAMS	PDP (aJ)			
	65nm		45nm	
	Max	Min	Max	Min
4T	2.792	1.132	3.581	2.255
6T	107.3	102.7	148.2	101.8
7T	122.8	45.97	45.36	19.05
8T	40.51	33.05	19.22	9.005

9T	211.0	196.6	228.7	142.64
Proposed 9T	20.52	22.57	11.77	7.130

Table III: - SNM of existing and proposed SRAM cell at 1.8V

SRAM CELL	HSNM	WSNM	RSNM
6T SRAM	528 mV	460 mV	83 mV
7T SRAM	532 mV	490 mV	89 mV
[illegible]	[illegible] mV	521 mV	93 mV
[illegible]	[illegible] mV	533 mV	71 mV
[illegible]	[illegible] mV	583 mV	107 mV

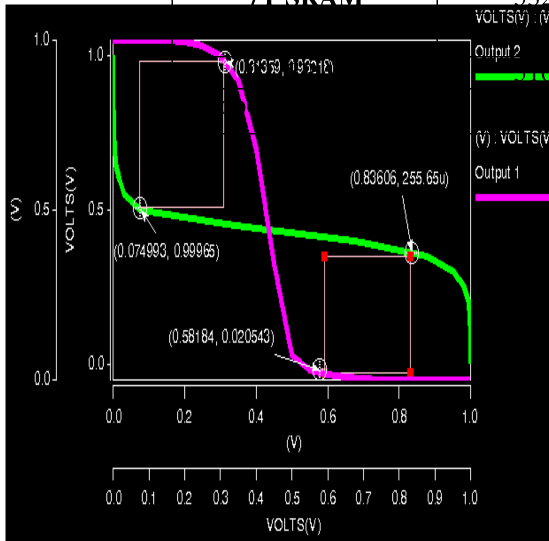

Fig.9. SNM curve of 6T SRAM cell

V. Conclusion

In this paper ,we have simulated and analyzed the performance of various topologies of SRAM cells at 65nm and 45nm technology for parameters like cell power consumption, delay and SNM. By comparative analysis of various topologies of SRAM cells; we can suggest that which SRAM cell topology is better based on various analyzed parameters. The comparative results are given in Table 1 which shows that the power consumption, delay and SNM are minimum for 4T, 9T and 4T SRAM Cells and maximum for 9T, 8T, and 6T SRAM Cells respectively. The results can be used to select SRAM cell topology to design and fabricate memory chips which is best suitable for different type of applications.

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